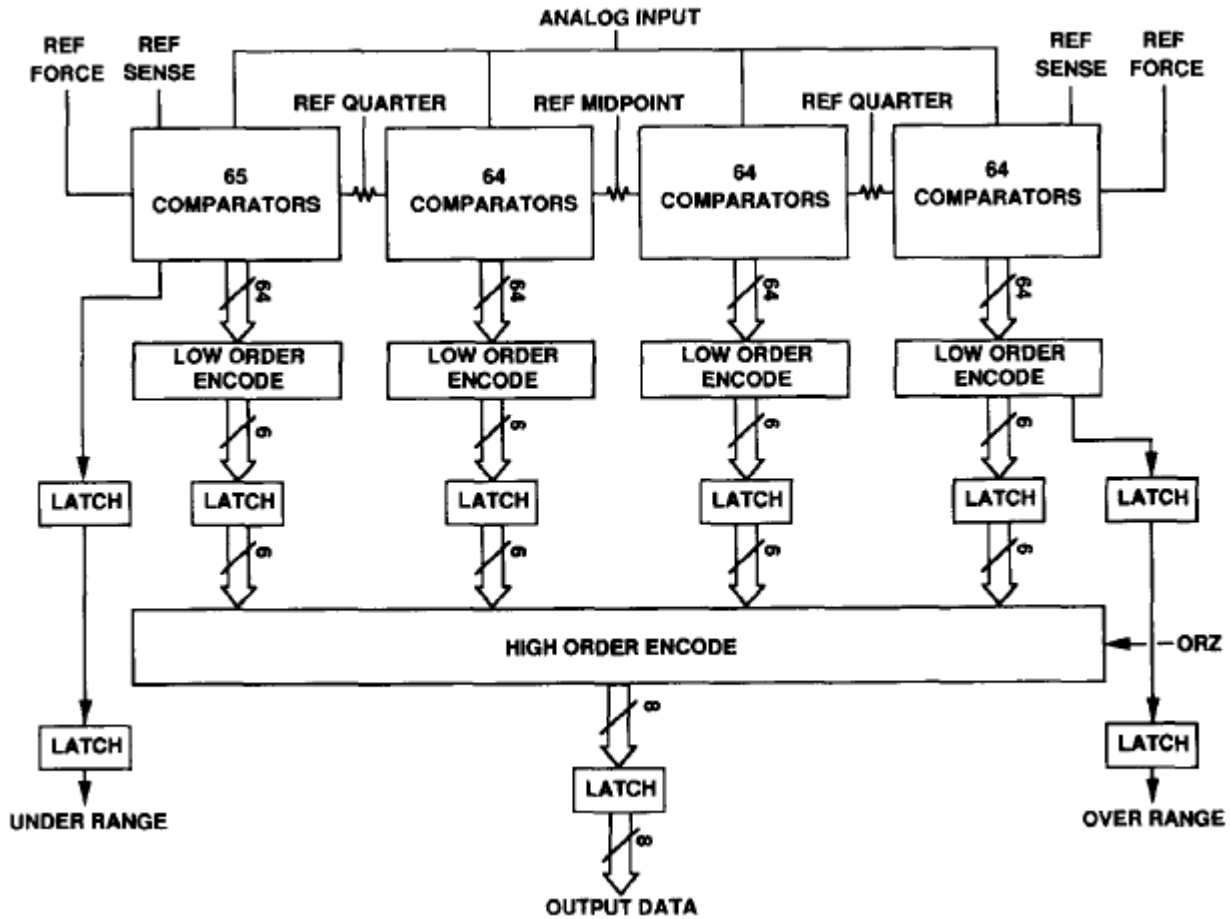
8-bit Flash ADC



C. Mangelsdorf, “A 400-MHz Input Flash Converter with Error Correction,” IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

Pipeline detail

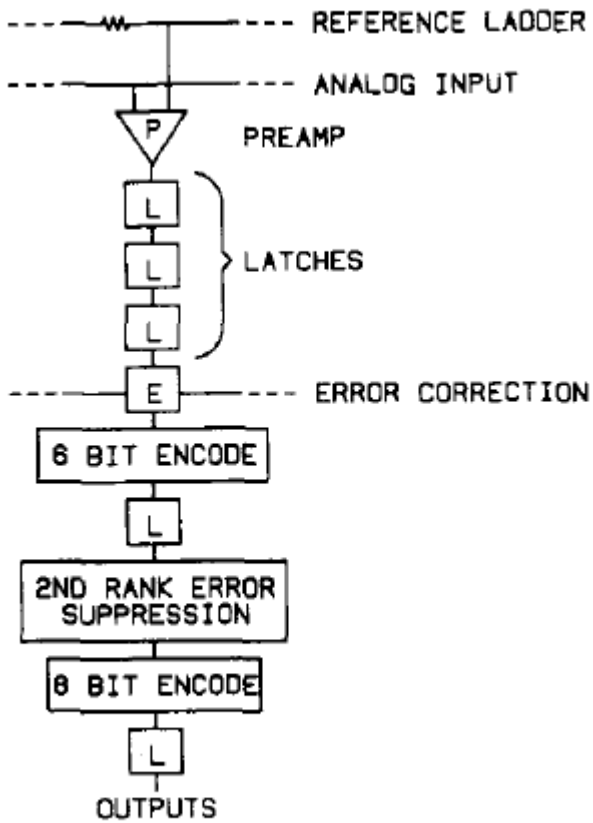
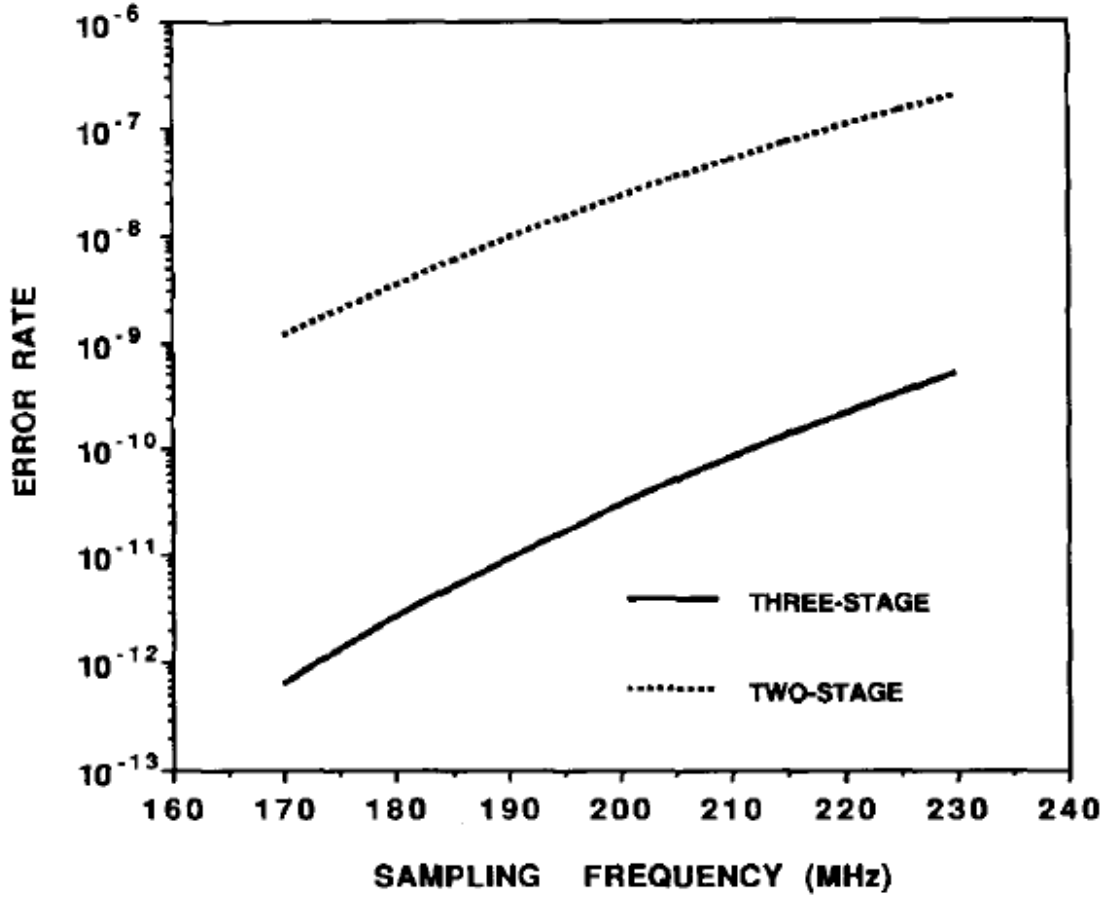


Fig. 2. Pipeline detail.

C. Mangelsdorf, “A 400-MHz Input Flash Converter with Error Correction,” IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

Reduced error rate due to cascaded latches



C. Mangelsdorf, “A 400-MHz Input Flash Converter with Error Correction,” IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

ENOB vs. input amplitude

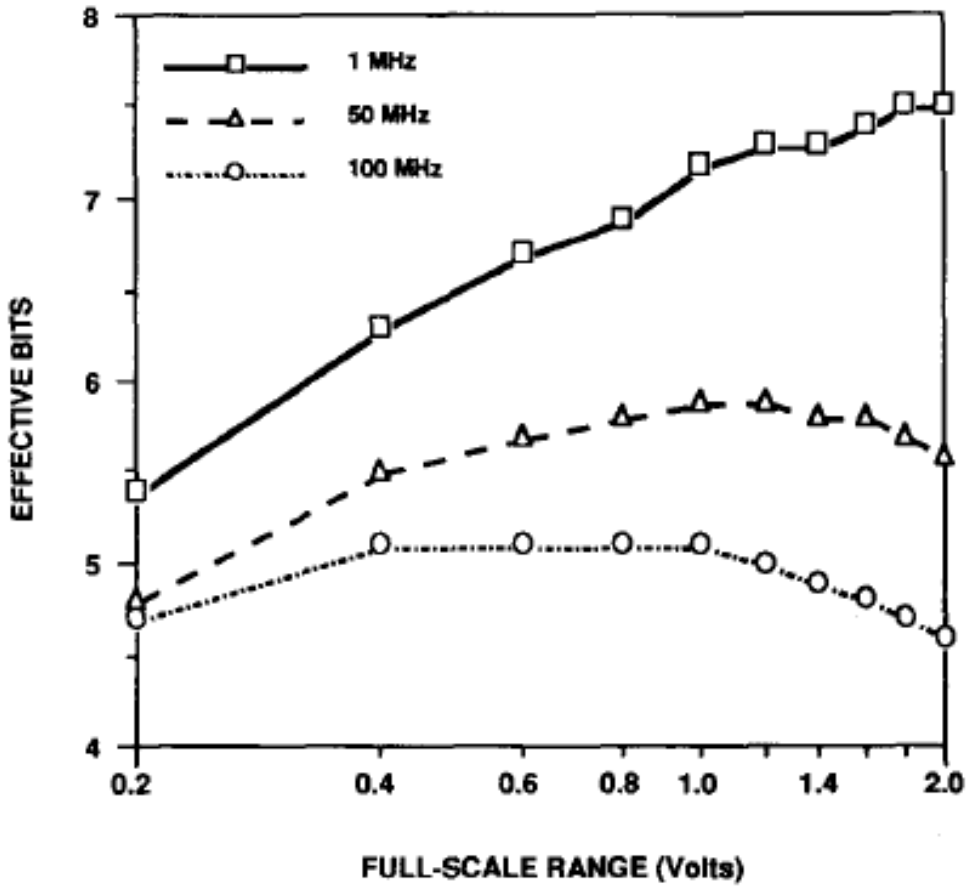


Fig. 10. Effective number of bits versus full-scale range for 1-, 50-, and 100-MHz analog input frequencies, all at 200 Ms/s. Input amplitude was adjusted for each range.

C. Mangelsdorf, “A 400-MHz Input Flash Converter with Error Correction,” IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

2 stage 10 bit ADC

94 comparators instead of 1024

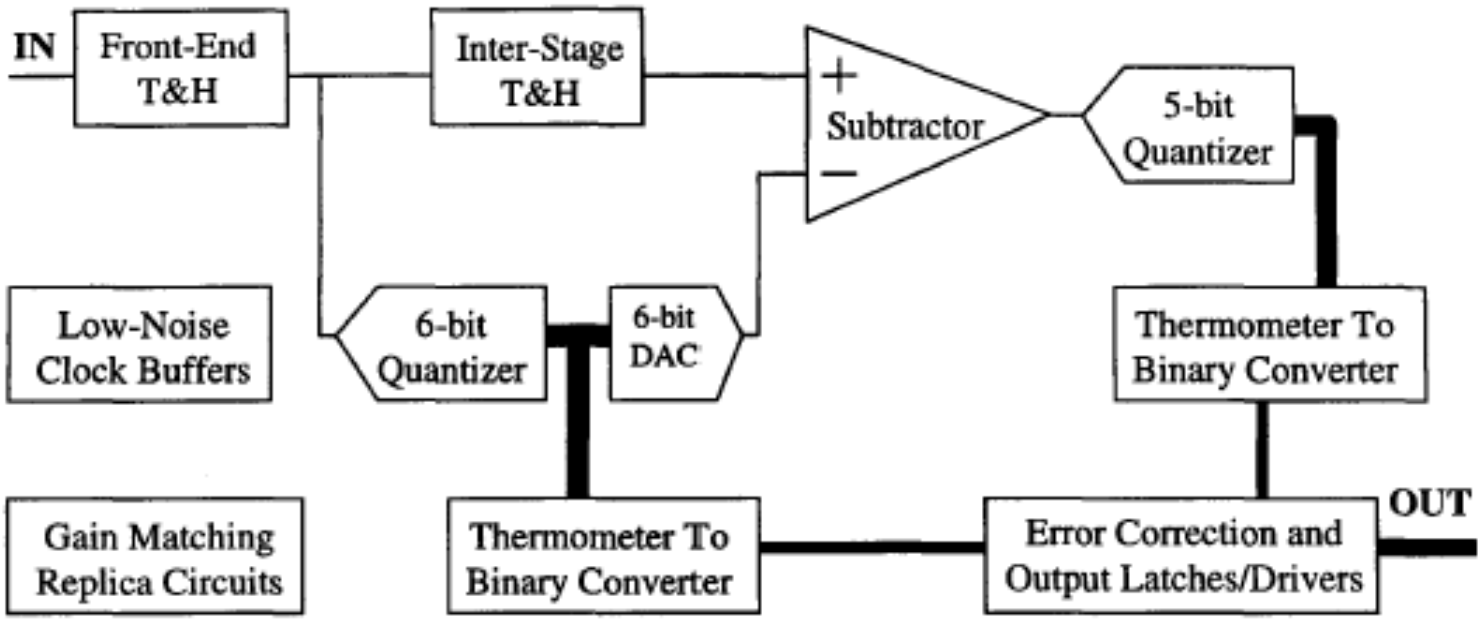


Figure 1: Block diagram of a 10-b, 1GS/s ADC.

N. Sheng, et al,"A 10-bit, 500 MS/s ADC," IEEE IMS, pp. 197-200, 1999.

2 stage ADC dynamic performance

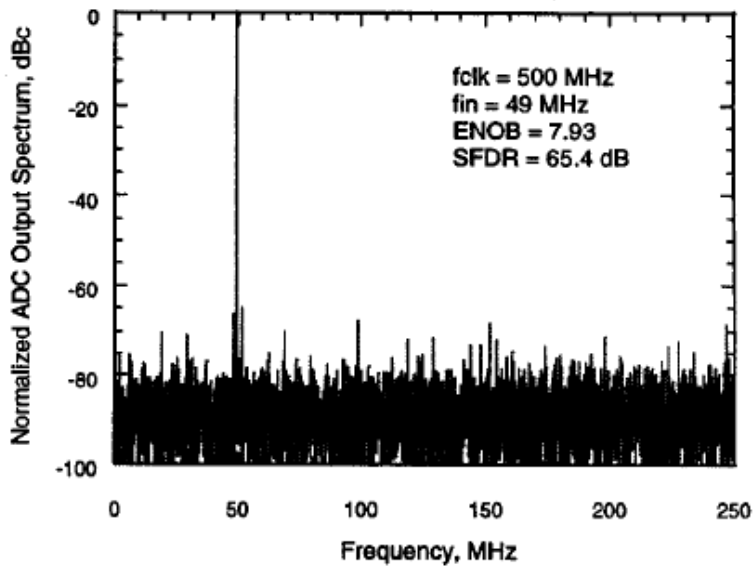


Figure 5: Measured ADC performance at 500 MS/s with 49 MHz input.

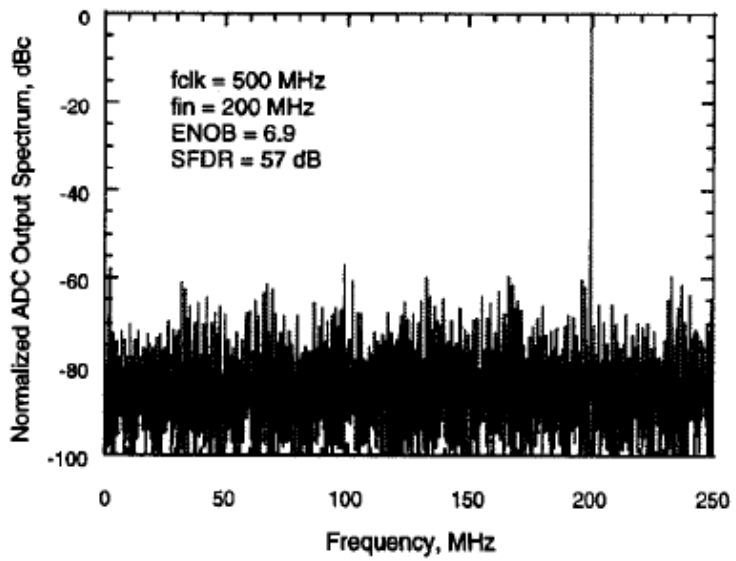


Figure 6: Measured ADC performance at 500 MS/s with 200 MHz input.

N. Sheng, et al,"A 10-bit, 500 MS/s ADC," IEEE IMS, pp. 197-200, 1999.

Subranging ADCs

- Area and power efficient
- Reduced number of comparators
- Suitable for pipelining
  - Increased clock rate but higher latency
  - interpolation, folding also can be used
- Uses simple CMOS diff amps

2 step 8-b subranging ADC

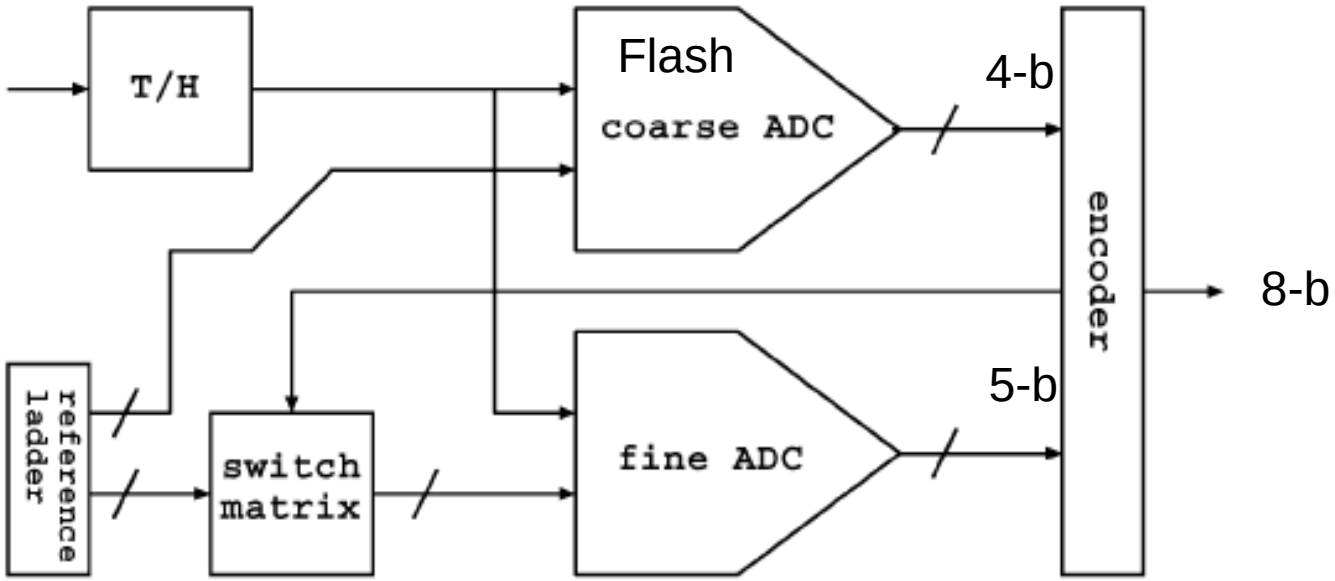


Fig. 1. Two-step subranging ADC architecture.

Output of 4-bit CADC

- selects between 15 reference subranges of 32 LSBs for FADC
- gives 4 MSBs

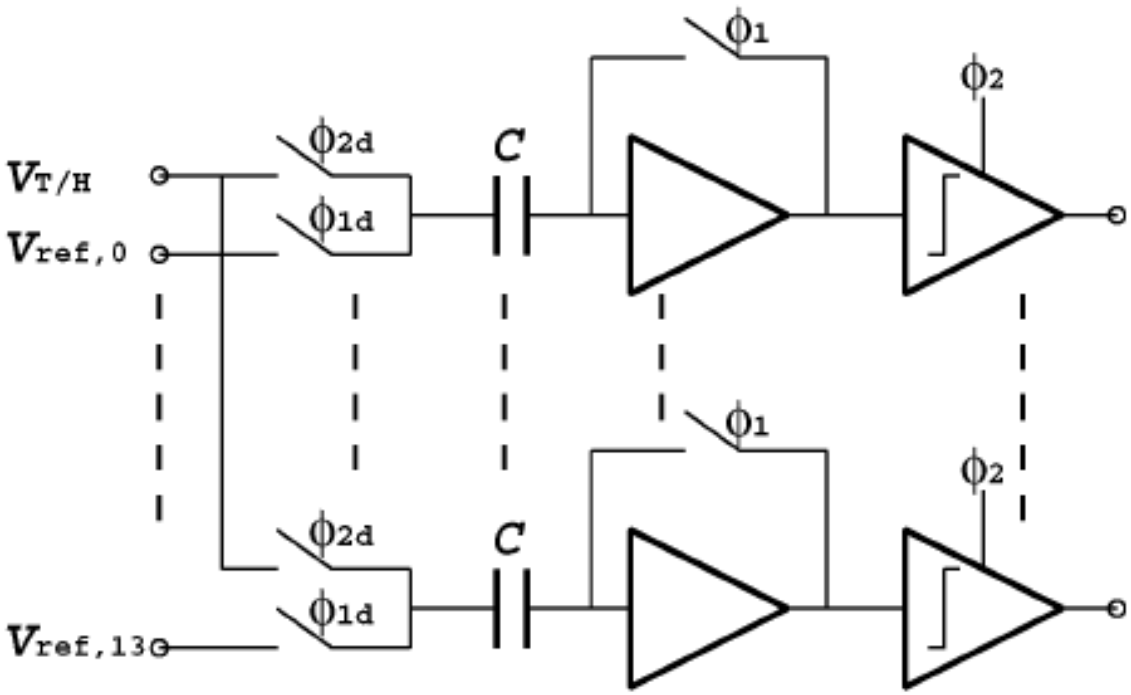
FADC has 5 bits to provide overrange – digitally correct for errors in CADC up to +/- 8 LSBs

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

Coarse ADC Operation: offset compensation

Φ1 reset for ½ clock cycle produces low Z at amplifier input. Store Vref,j + Voffset on C

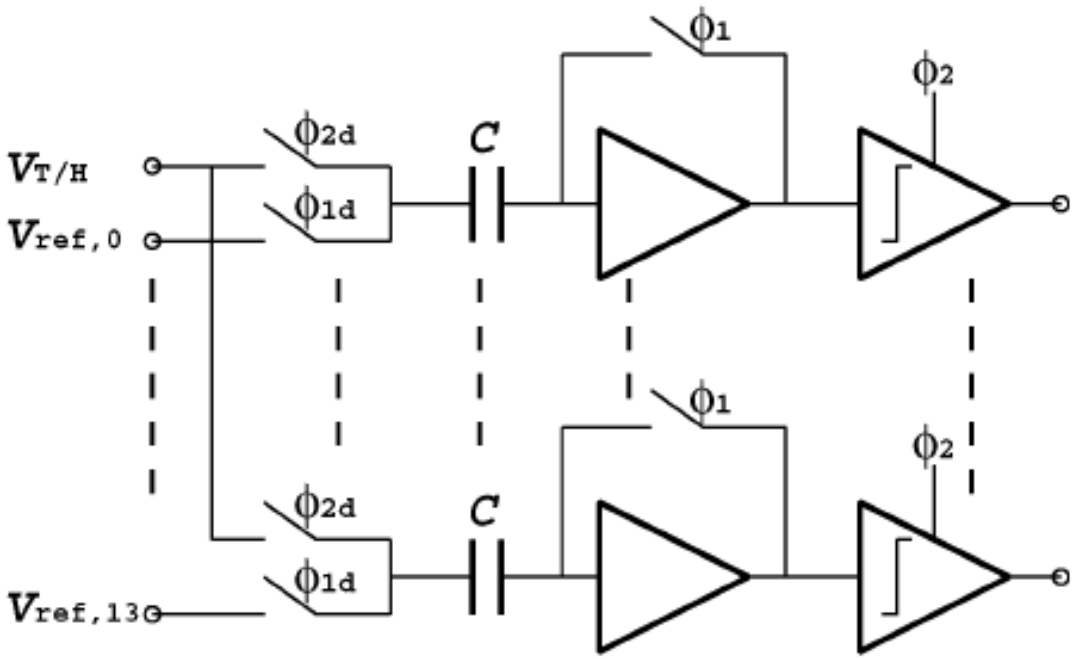
Φ2 then activates amplifier. The difference between $V_{T/H}$ and Vref then is sensed by the amplifier with the same offset.



J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

Switch charge Injection compensation

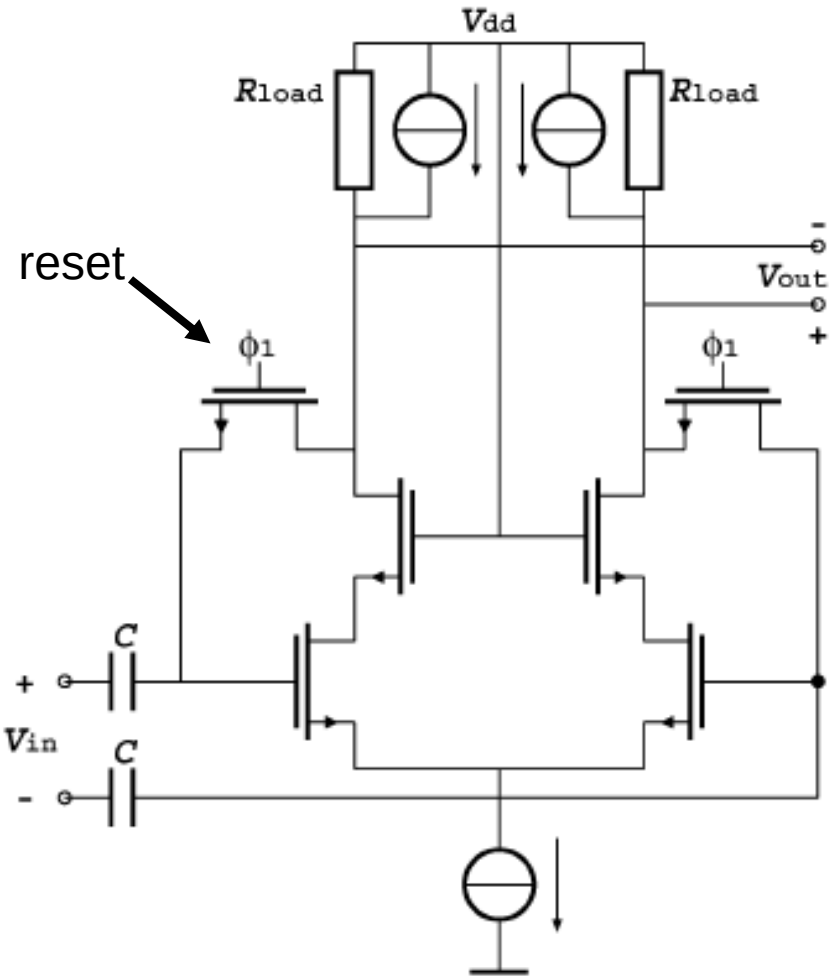
- **Charge injection on reset (ϕ1) is signal-independent**
- **ϕ1 opens slightly before ϕ1d so that signal-dependent charge injection is minimized**



J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

CADC amplifier

- Full differential reduces substrate noise
- Cascode improves speed
- Current sources in parallel with Rload increases gm



J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

Fine ADC operation

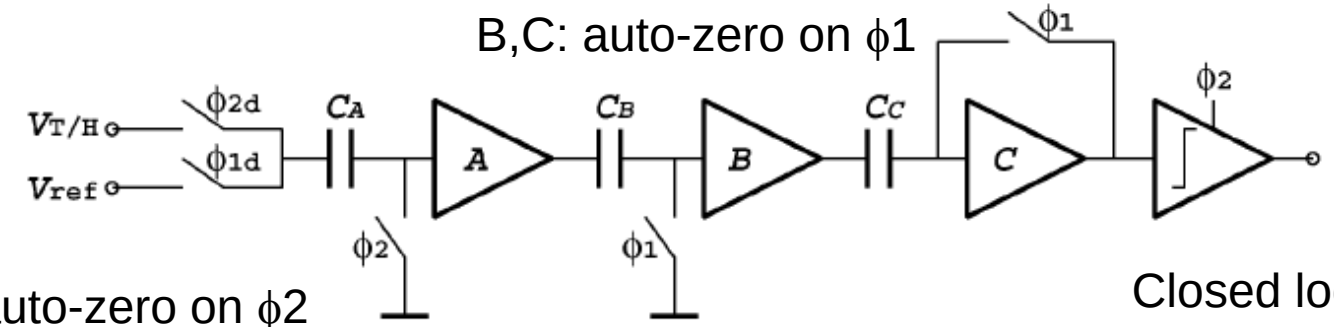
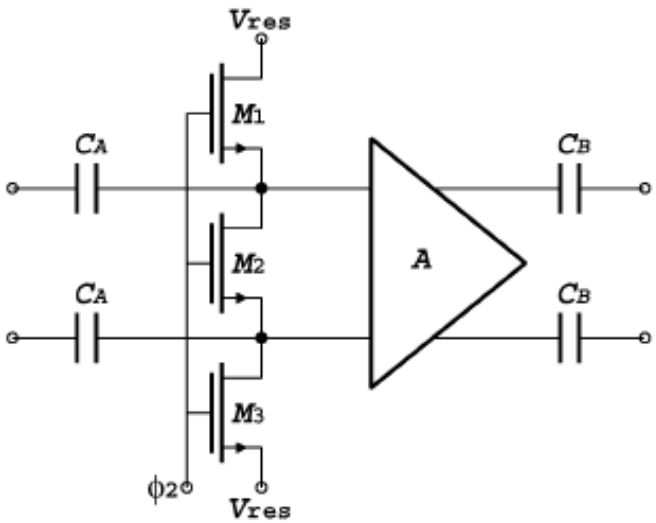


Fig. 5. Operation principle of the FADC.



Reset switch on A, B
Open loop offset comp

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

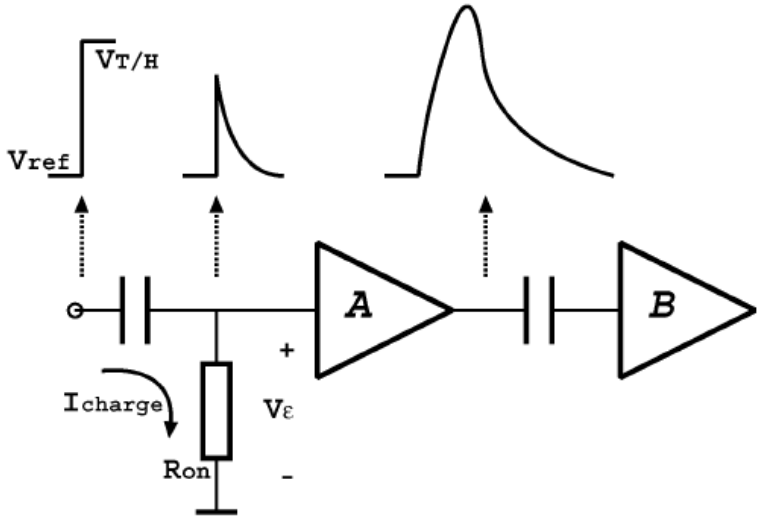


Fig. 7. Effect of finite on-resistance of the reset switches at high conversion rates.

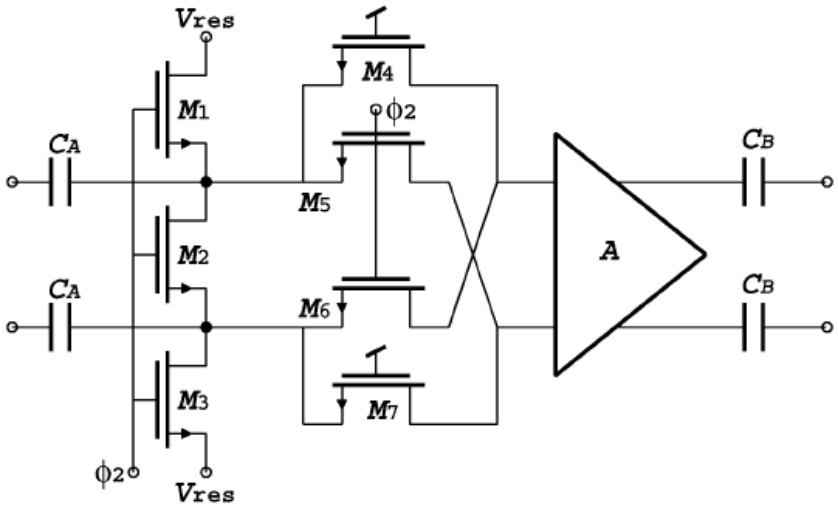


Fig. 8. Implementation of the reset switches in array A and B of the FADC.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

2X Interpolation of ref ladder

Reduces number of comparators, requires fewer ref voltages

Fewer subranging switches needed

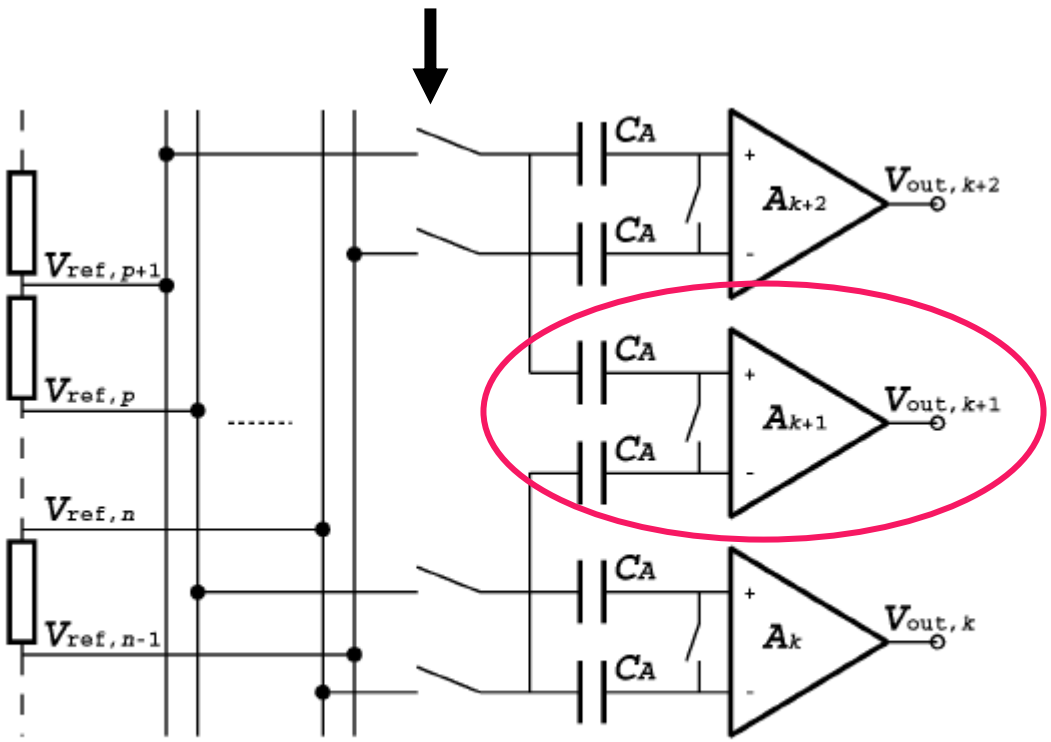


Fig. 9. Implementation of 2× interpolation of the reference ladder voltages.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

Another 2X interpolation

Charge redistribution is used to generate intermediate reference voltage

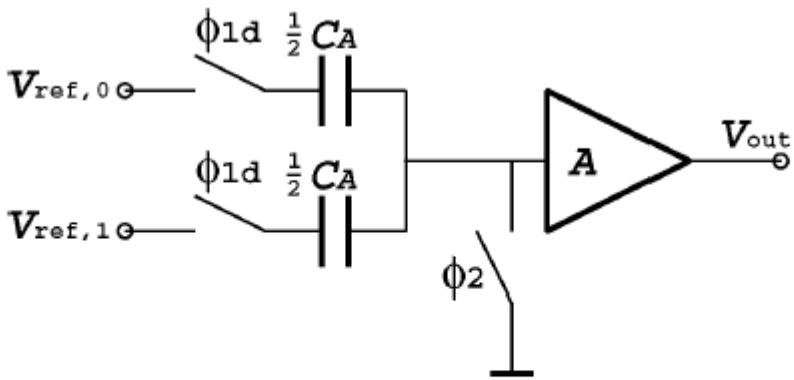


Fig. 10. Implementation of another 2× capacitive interpolation of the reference ladder voltages.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

FADC pipeline

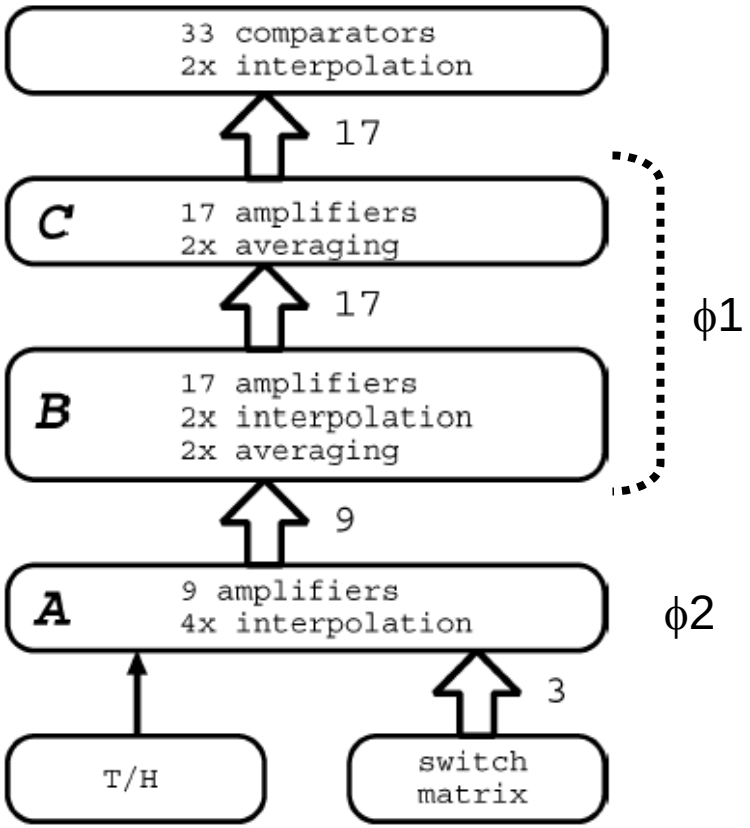


Fig. 4. Block diagram of the FADC.

- Interpolation is introduced at A, B and C
- Only 17 ref voltage taps
- Capacitive loading of switches and amplifiers is reduced proportionally

Active 2X interpolation

2X in row B
2X in comparator

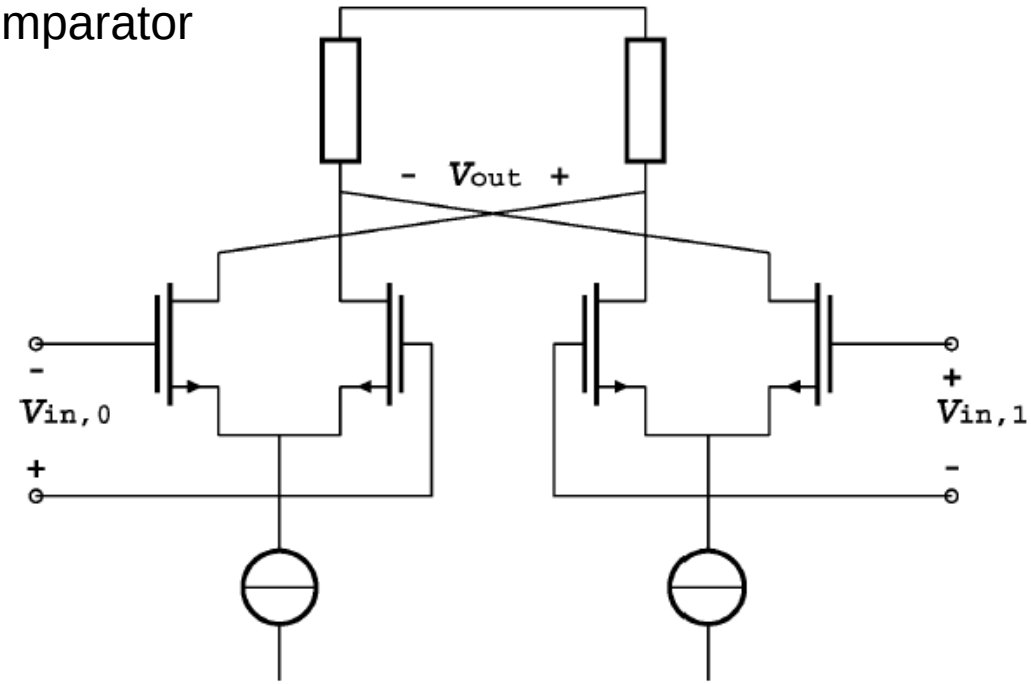


Fig. 11. Simplified schematic of a differential-pair amplifier providing 2× interpolation.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

Capacitive averaging

- RESET:
  - Each cap charged Vin,0 and Vin,1
- AMPLIFY:
  - Charge redistribute
  - Node voltage is the average of Vin,0 ar Vin,1.
- Decreases influence switching noise and random mismatch wl is uncorrelated
- Better SNR

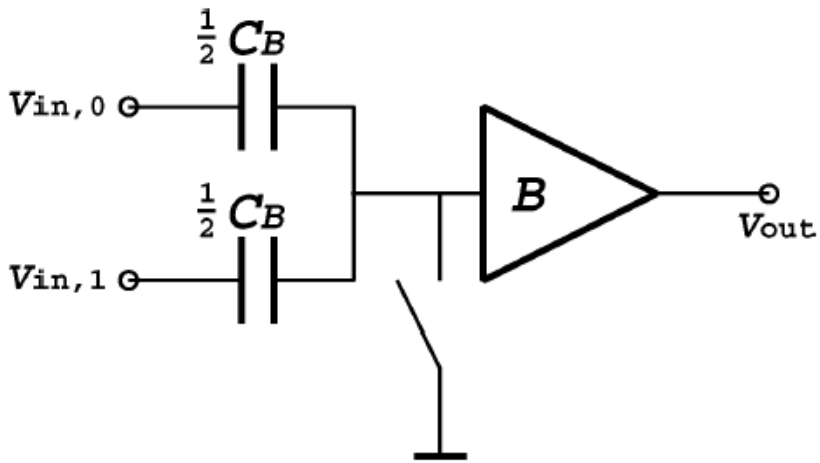


Fig. 12. Implementation of 2× capacitive averaging.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

4X averaging of A stage; 2X averaging of B

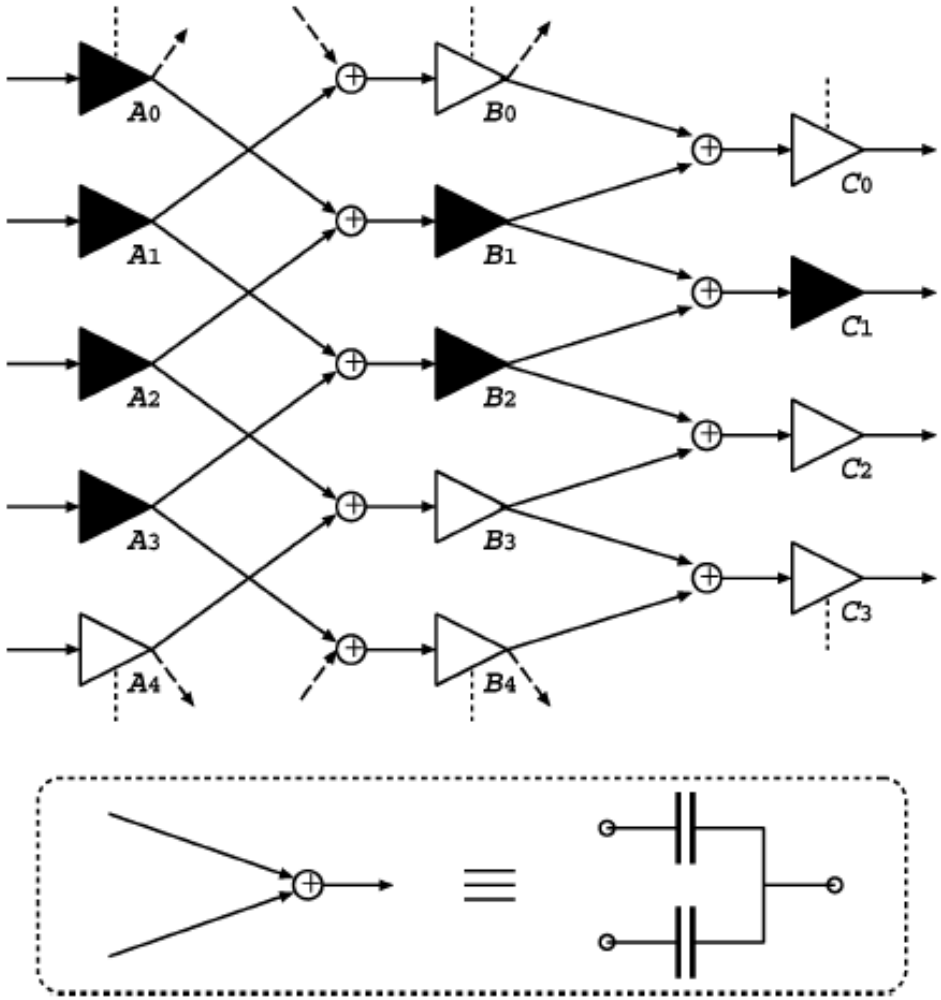


Fig. 13. Distributed averaging topology, providing 4× and 2× averaging of the amplifiers in array A and B, respectively.

J. Mulder, etal.,"A 21mW 8-b 125 MS/s ADC in 0.09 mm^2 0.13 um CMOS," IEEE JSSC, Vol. 39, #12, pp. 2116-2125, Dec. 2004.

CMOS MS Comparator

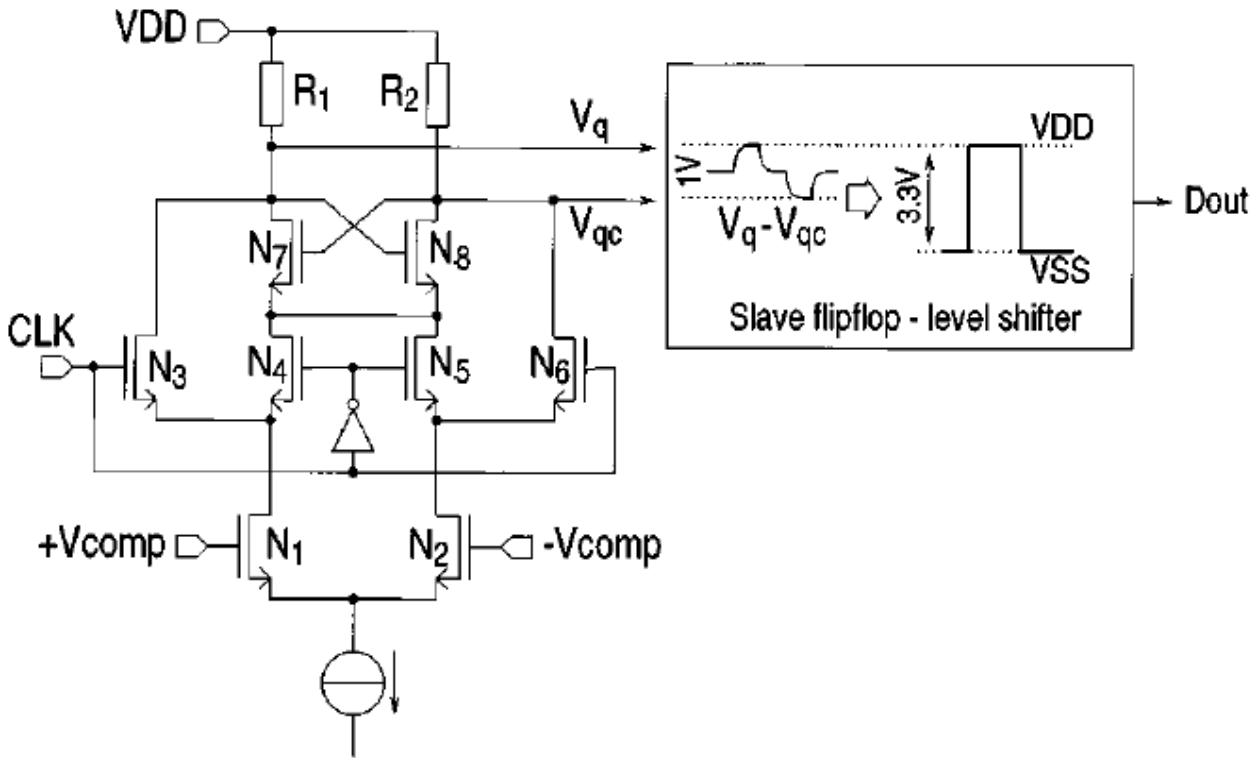


Fig. 10. Implementation of master-slave comparator, optimized for a low bit error rate.

A. Venes, R. Van de Plassche, “An 80 MHz, 80 mW, 8-bit Folding ADC with Distributed Track Hold Preprocessing,” IEEE JSSC, Vol. 31, #12, pp. 1846 – 1853, Dec. 1996.

BJT Comparator

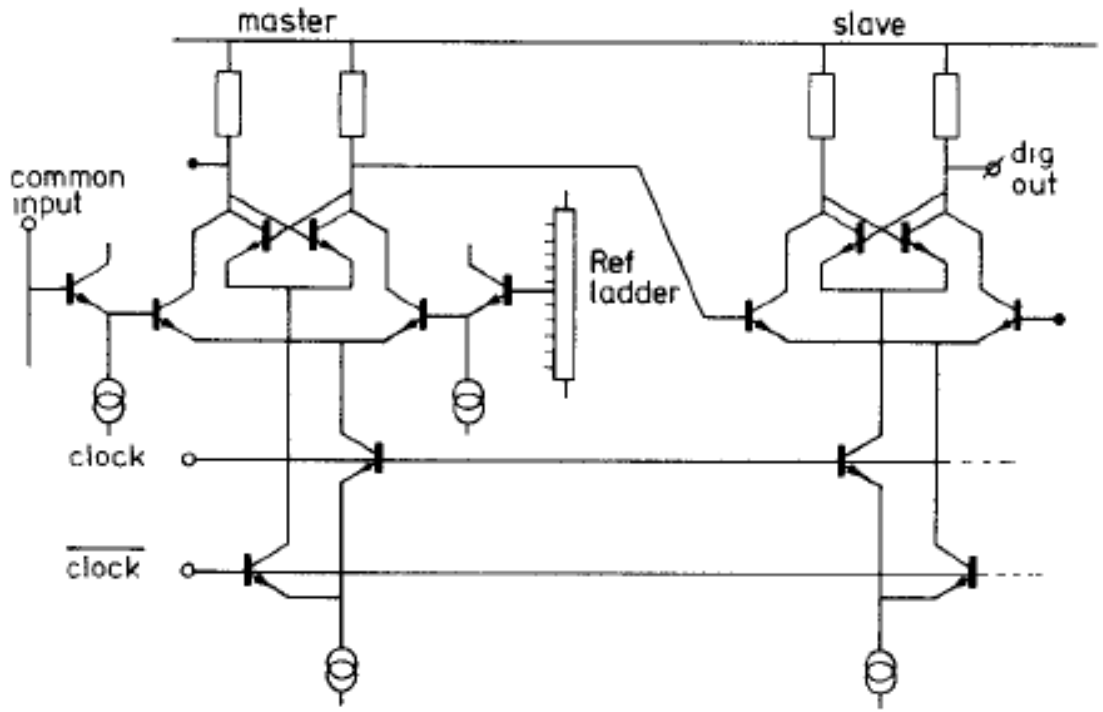


Fig. 2. Standard comparator cell with a master and a slave flip-flop in ECL-miniwatt technique.

Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

Folding ADC

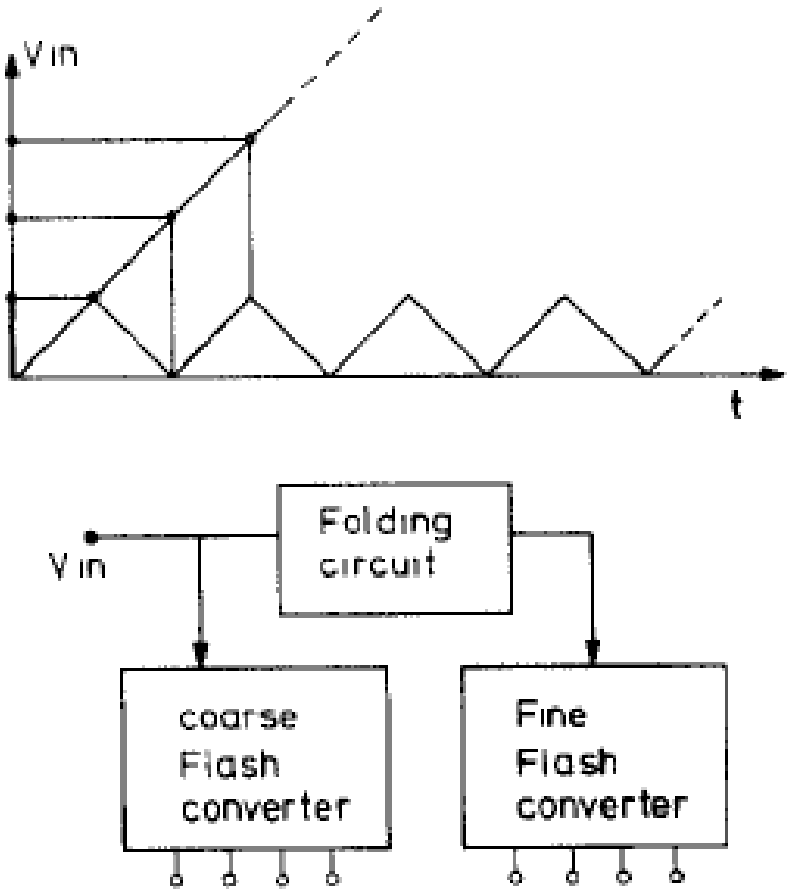


Fig. 4. Block diagram of a single folding system.

Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

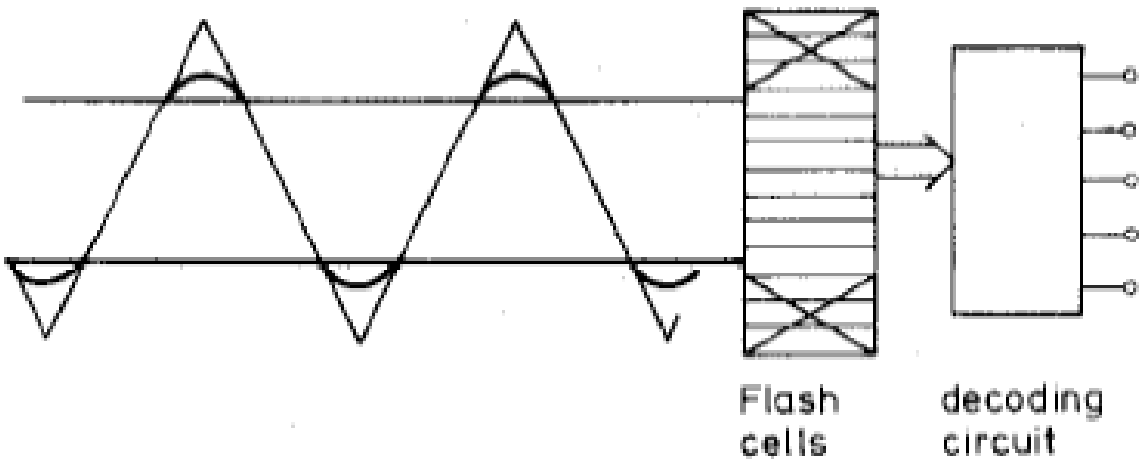


Fig. 8. Triangular waveform with rounding-off effect.

Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

Double Folding ADC

90 degrees out of phase

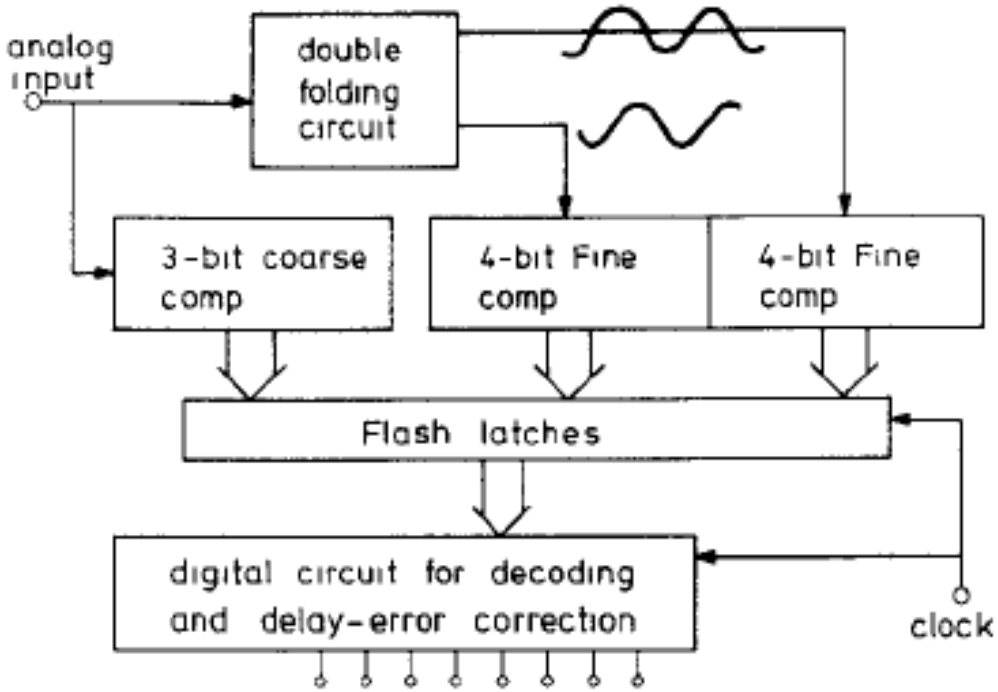


Fig. 5. Block diagram of the double folding system.

Rounding error is corrected in fine ADCs by nonlinear R ladder taps.

Van de Grift and van de Plassche, "Monolithic 8-bit Video ADC," IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

Range overlap reduces nonlinearity due to rounding error

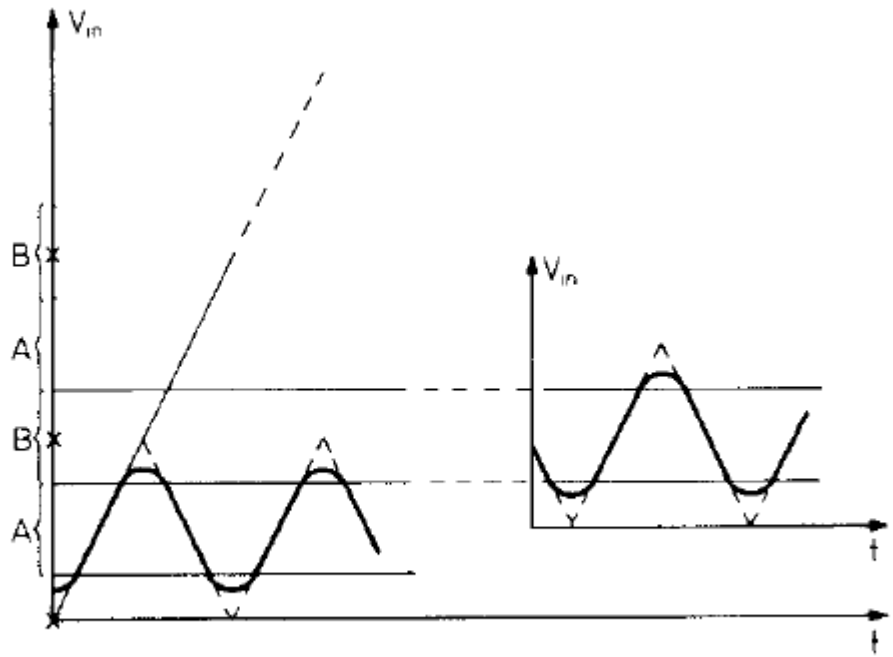


Fig. 6. Signal waveforms of the double folding system.

Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

Double folding circuit

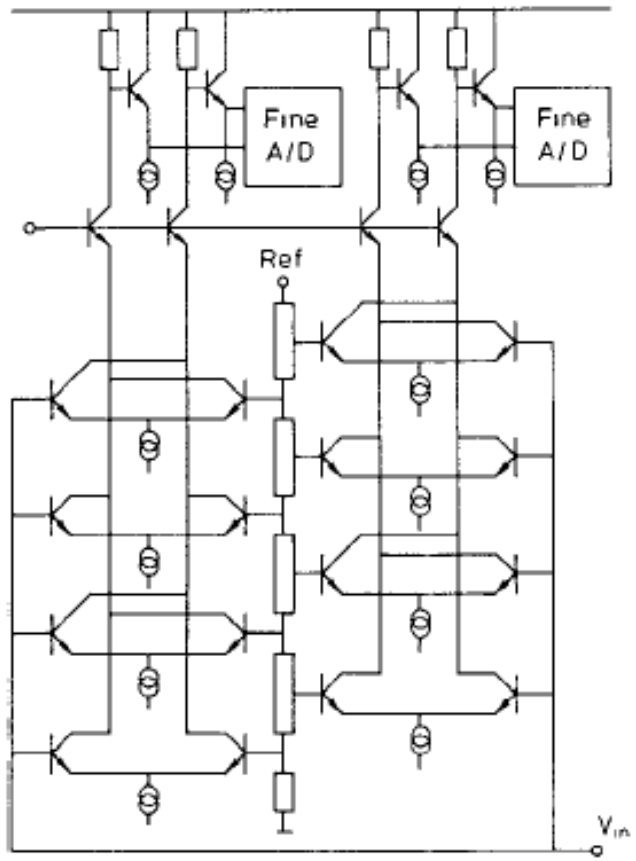
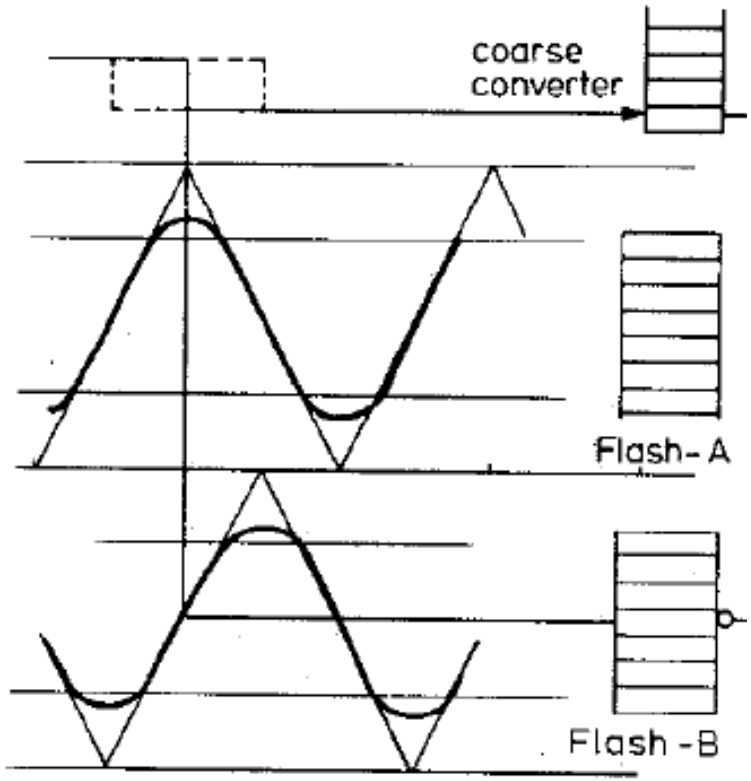


Fig. 7. Simplified circuit diagram of the double folding system.

Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.



Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.

References

- Van de Grift and van de Plassche, “Monolithic 8-bit Video ADC,” IEEE JSSC, vol.19, #3, pp.374-8, June 1984.
- A. Venes, R. Van de Plassche, “An 80 MHz, 80 mW, 8-bit Folding ADC with Distributed Track Hold Preprocessing,” IEEE JSSC, Vol. 31, #12, pp. 1846 – 1853, Dec. 1996.
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- N. Sheng, et al,”A 10-bit, 500 MS/s ADC,” IEEE IMS, pp. 197-200, 1999.
- C. Mangelsdorf, “A 400-MHz Input Flash Converter with Error Correction,” IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.
- J. van Valburg and R. van de Plassche, “An 8-b 650 MHz Folding ADC,” vol 27, #12, pp. 1662-6, Dec 1992
- K. Poulton, et al.”A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS,” ISSCC 2003, paper 18.1.
- K. Poulton, et al.”A 4Gs/s 8b ADC in 0.35 um CMOS,” ISSCC 2002, paper 10.1.