Introduction to Agilent ADS circuit simulation tools

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Introduction

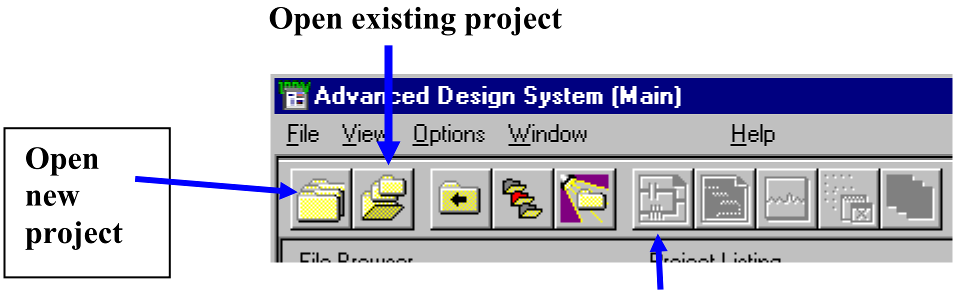
ADS provides a vast array of simulation modes and models. For design of high speed digital circuits, the most useful simulation tools will be DC and transient analysis. Whether to use ADS or HSPICE is a matter of individual preference. Since ADS is oriented toward microwave applications, you will find that it contains a much larger library of transmission line and passive component models that include nonidealities of these components. When dealing with high speed interconnections, this might provide the incentive to learn to use ADS even if you are already an experienced HSPICE user. On the other hand, ADS has yet to handle transistor model libraries in a convenient manner. It is much simpler to switch between process corners in HSPICE using the library commands.

The easiest way to learn ADS is through example files. ADS project files are stored in a compressed format with a .zap file extension.
1. Download the ***ece225_ex1.zap*** file from the course website and locate it in your user directory with write permission. This may require renaming the file since Internet Explorer likes to add a .zip extension to these files. Rename the file by removing the .zip.

2. Open up ADS from the START menu.
Start > Programs > Advanced Design System 2002 > Advanced Design System

There are two ways to begin using ADS.
The first is to import an existing compressed project file. (Simulations are saved in a "project" directory.) Choose: File > Uncompress. Browse to find and select the correct file. When the file is uncompressed, a schematic display panel and a data display panel will open. Simulations are performed from the schematic and outputs read on the data display.

The second method is to open up a new project You must choose a name for the project directory. If the project has already been created, then open it up with the Open icon and selecting the project name.



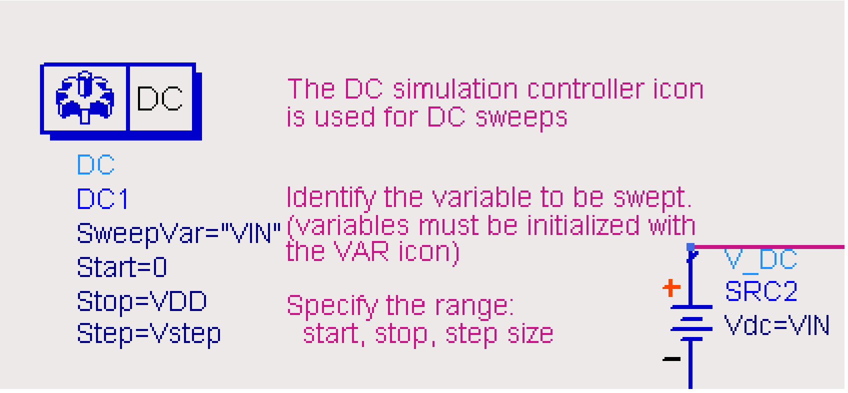
Open existing project

Open new project

If the schematic window doesn't open automatically, open the window with this button.

DC simulation.

Open the CMOS inverter schematic (*inverter_vtc*). Notice that the simulation type is set through a controller icon. These are found in the pulldown menu on the toolbar at the upper left of the window. In this example, a DC sweep of the input voltage is enabled as shown below.



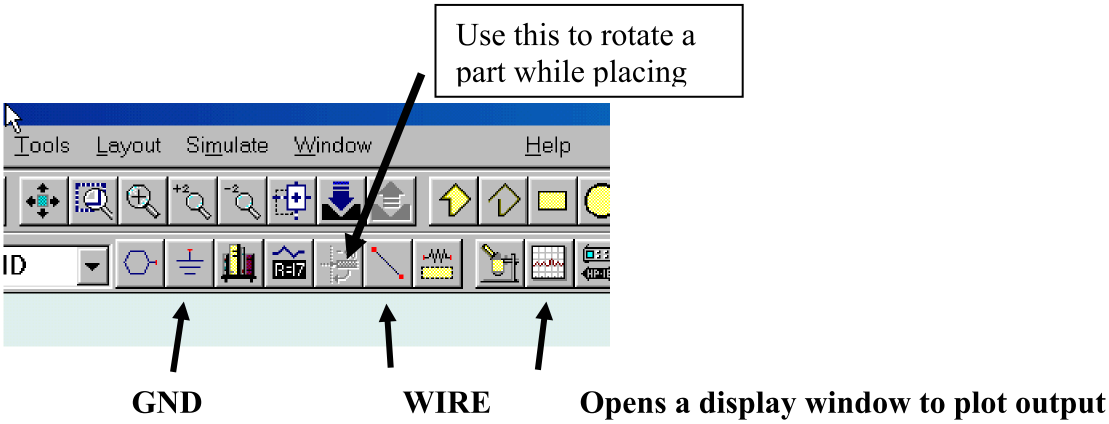
DC
DC1
SweepVar="VIN"
Start=0
Stop=VDD
Step=Vstep

The DC simulation controller icon is used for DC sweeps

Identify the variable to be swept. (variables must be initialized with the VAR icon)

Specify the range: start, stop, step size

Schematics can be constructed by placing components and interconnecting them with wires. Use the drop down menu and associated palette at the left side of the schematic panel to select components.



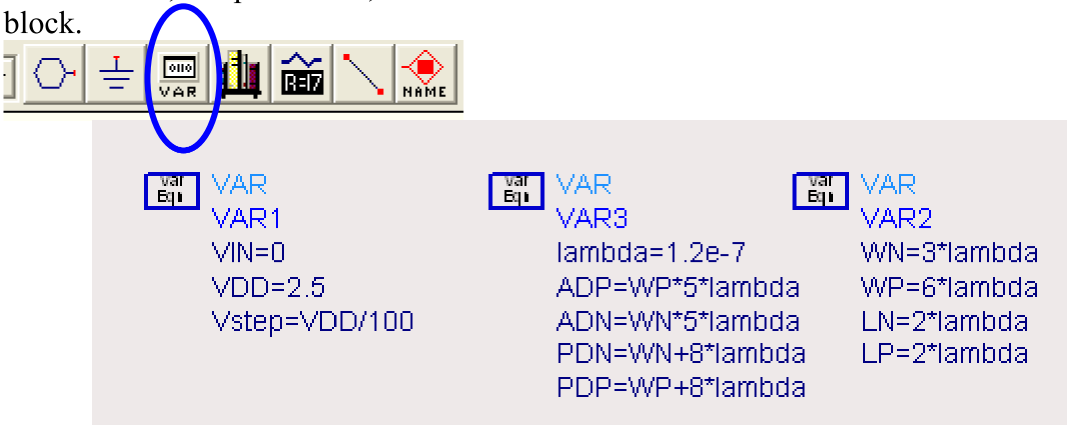
Use this to rotate a part while placing

GND

WIRE

Opens a display window to plot output

All variables, swept or fixed, must be identified and initialized first with a VAR icon block.

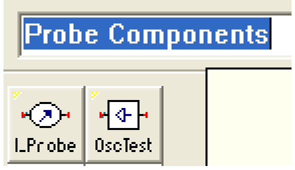


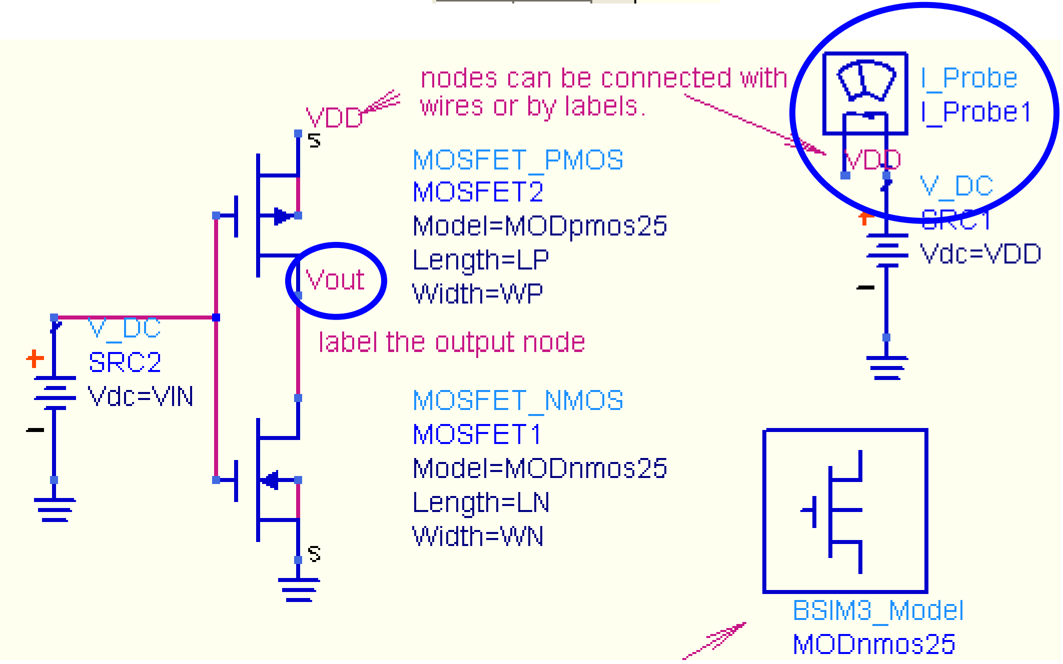
VAR
VAR1
VIN=0
VDD=2.5
Vstep=VDD/100

VAR
VAR3
lambda=1.2e-7
ADP=WP*5*lambda
ADN=WN*5*lambda
PDN=WN+8*lambda
PDP=WP+8*lambda

VAR
VAR2
WN=3*lambda
WP=6*lambda
LN=2*lambda
LP=2*lambda

Output variables are defined by labeling circuit nodes. (Insert > Wire/Pin label) You can also add current probes wherever needed to measure current.




nodes can be connected with wires or by labels.

label the output node

MOSFET_PMOS
MOSFET2
Model=MODpmos25
Length=LP
Width=WP

MOSFET_NMOS
MOSFET1
Model=MODnmos25
Length=LN
Width=WN

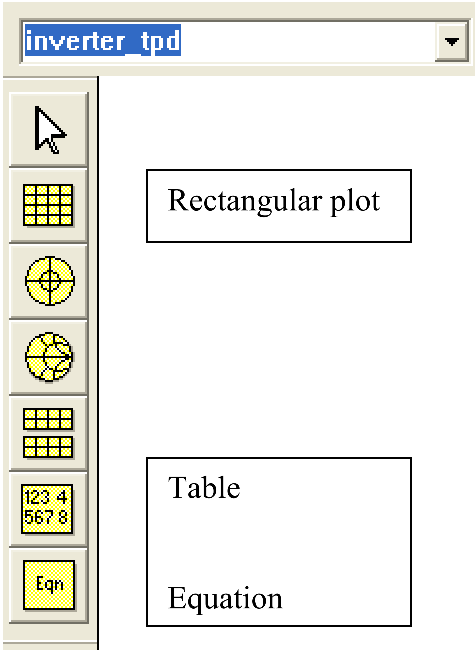
V_DC
SRC2
Vdc=VIN

I_Probe
I_Probe1

V_DC
SRC1
Vdc=VDD

BSIM3_Model
MODnmos25

Run the simulation (F7) then view the data display. Any node voltage can be plotted or read in a table. The palette on the left side of the data display provides several options.



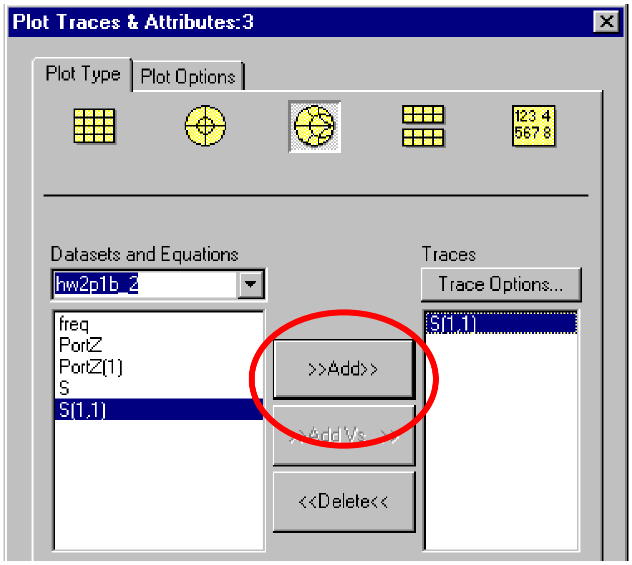
Use pulldown menu to choose correct dataset

Rectangular plot

Table

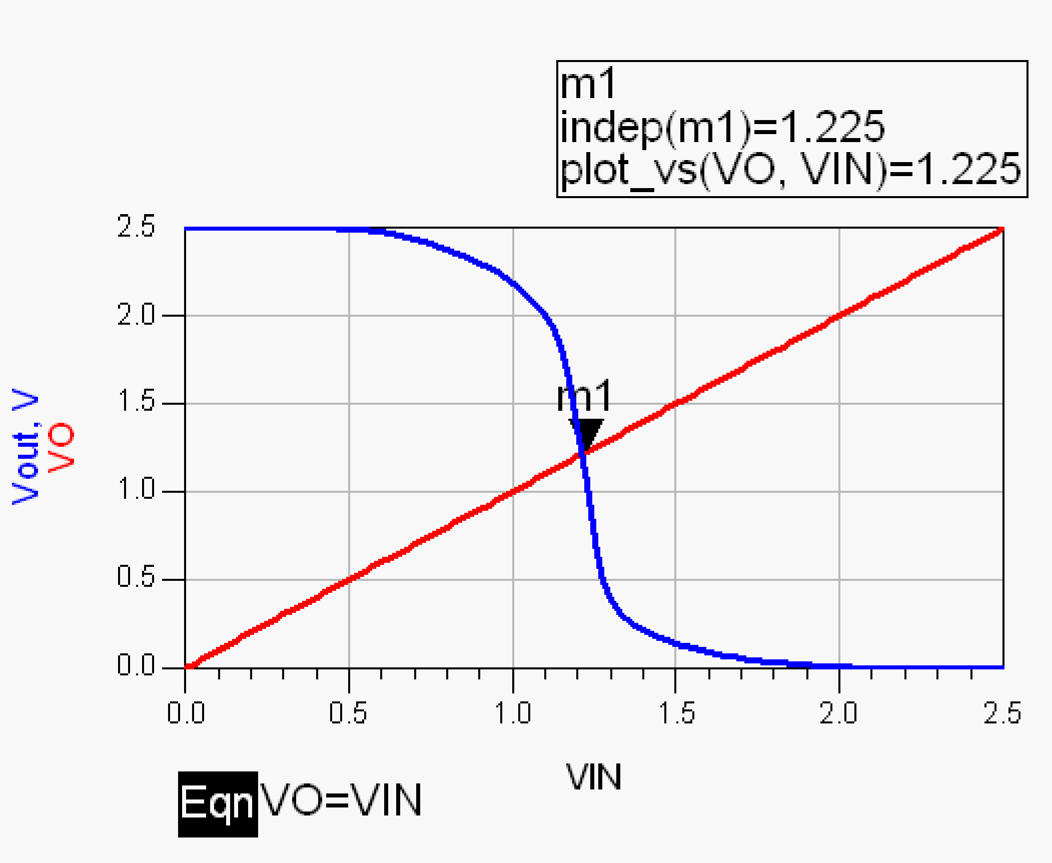
Equation

Plot Traces & Attributes opens up with a menu that you can use to select the desired variable, in this case, S(1,1). Highlight the variable by clicking on it and click on Add.



Datasets and Equations: hw2p1b_2

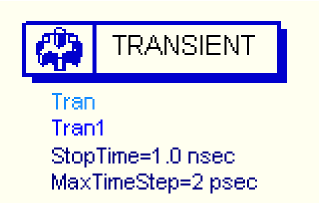
Traces: S(1,1)



Markers can be placed on the plot to measure voltages more precisely. Equations can be defined as needed. In the example above, the equation VO = VIN is used to plot the red line that defines the inverter threshold.

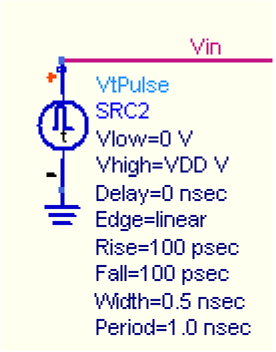
Transient Analysis

You can use the transient analysis simulation mode to predict propagation delays. Find the Simulation – Transient menu and select the transient controller. Then specify the simulation time and the maximum time step size.



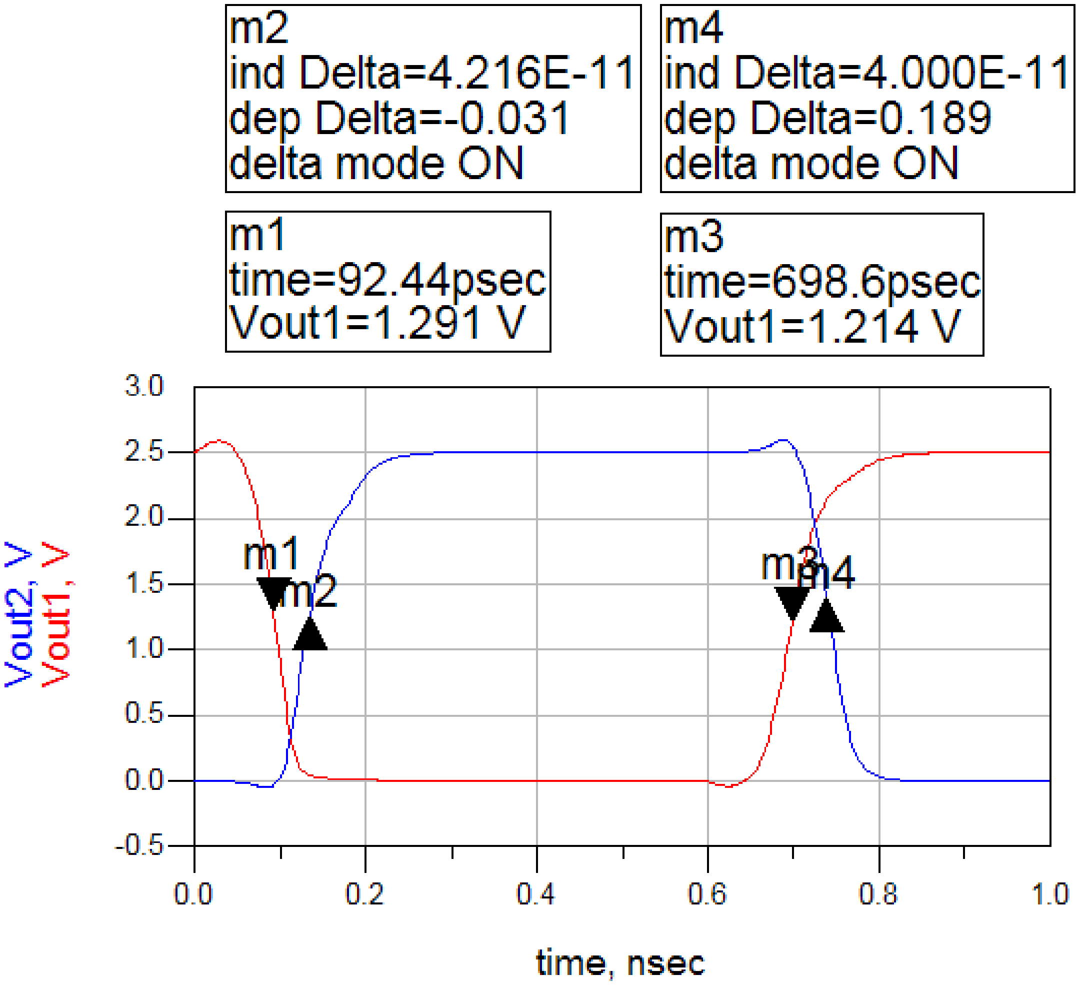
Tran
Tran1
StopTime=1.0 nsec
MaxTimeStep=2 psec

A pulse source can be used for driving the inverter inputs. Choose appropriate voltages and rise/fall times. Refer to inverter_tpd for an example.



VtPulse
SRC2
Vlow=0 V
Vhigh=VDD V
Delay=0 nsec
Edge=linear
Rise=100 psec
Fall=100 psec
Width=0.5 nsec
Period=1.0 nsec

The input and output of the inverter under test is shown below. Markers can be used to measure t_{PHL} and t_{PLH}. Using the delta marker function we find t_{PLH} = 42 ps and t_{PHL} = 40 ps



m2
ind Delta=4.216E-11
dep Delta=-0.031
delta mode ON

m4
ind Delta=4.000E-11
dep Delta=0.189
delta mode ON

m1
time=92.44psec
Vout1=1.291 V

m3
time=698.6psec
Vout1=1.214 V

How do you calculate power dissipation using ADS?

You can include a current probe in the path to measure current. (its in the probe components palette: I_probe. Note that the output from the probe contains a suffix .i

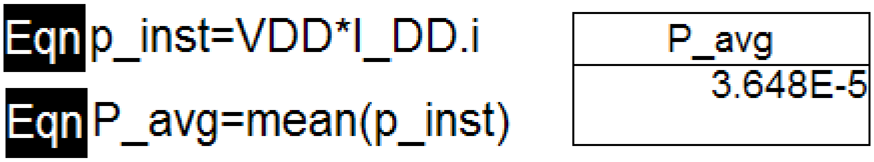
For example, the current value measured by a current probe with an instance I_DD is called I_DD.i)

A measurement equation can be written that includes calculation of the instantaneous power and the average power.

P_inst = VDD * I_DD.i
P_avg = mean(p_inst)

Note that the simulation should include an integral number of cycles in order to calculate the power accurately. Of course if you are averaging over lots of cycles, a small truncation error won't matter much.

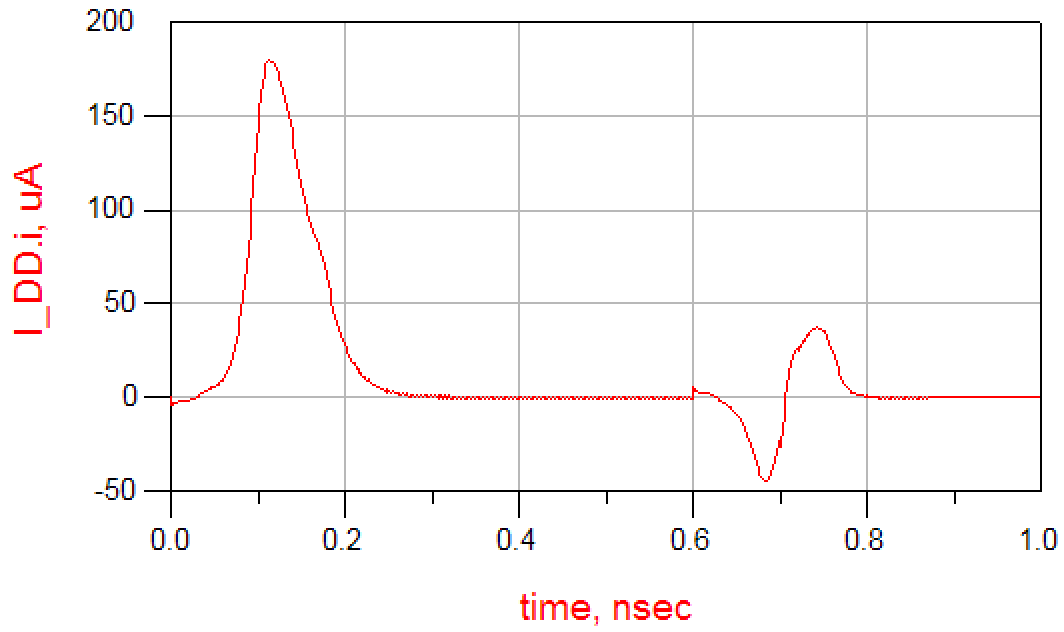
You would look for the output of the measurement equation P_inst or P_avg in the data display as just another variable. If you do calculations with the Eqn in the data display, then you locate that output in another data set called equations. This is found when you are setting up a plot or table by the pulldown menu under datasets and equations.



Eqn p_inst=VDD*I_DD.i

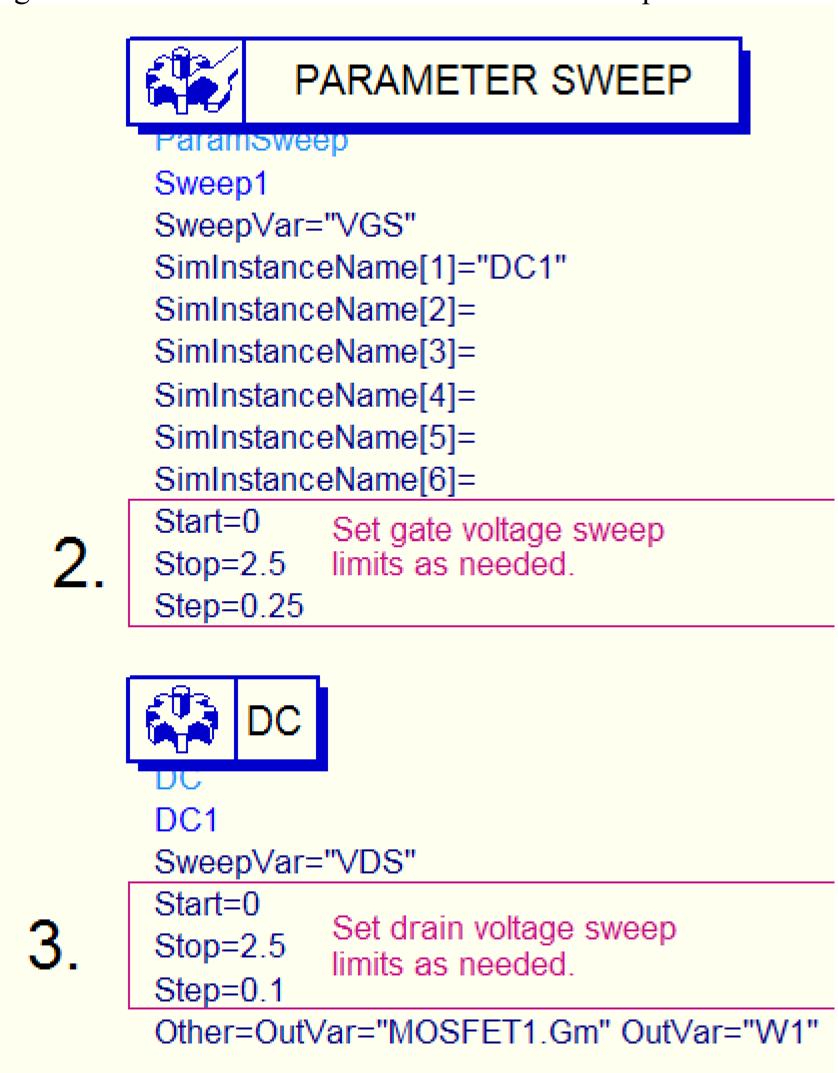
Eqn P_avg=mean(p_inst)

P_avg
3.648E-5



Parameter Sweeps

Parameter sweeps perform a very useful function in simulations. It allow the systematic variation of one or more parameters to find optimum parameter values or to investigate trends in performance or simply to sweep out I – V characteristics of an active device. The latter is illustrated in the ECE225_S03 project by the NMOS and PMOS curve tracer schematics. The parameter sweep controller can be found in the palette that displays for every simulation mode in ADS. In the example below, the DC controller sweeps VDS from 0 to 2.5V first with VGS = 0. VGS is then incremented by 0.25V and VDS is swept again. This continues until VGS = 2.5V at which point the simulation is complete.



ParamSweep
Sweep1
SweepVar="VGS"
SimInstanceName[1]="DC1"
SimInstanceName[2]=
SimInstanceName[3]=
SimInstanceName[4]=
SimInstanceName[5]=
SimInstanceName[6]=

2. Start=0
Stop=2.5
Step=0.25

Set gate voltage sweep limits as needed.

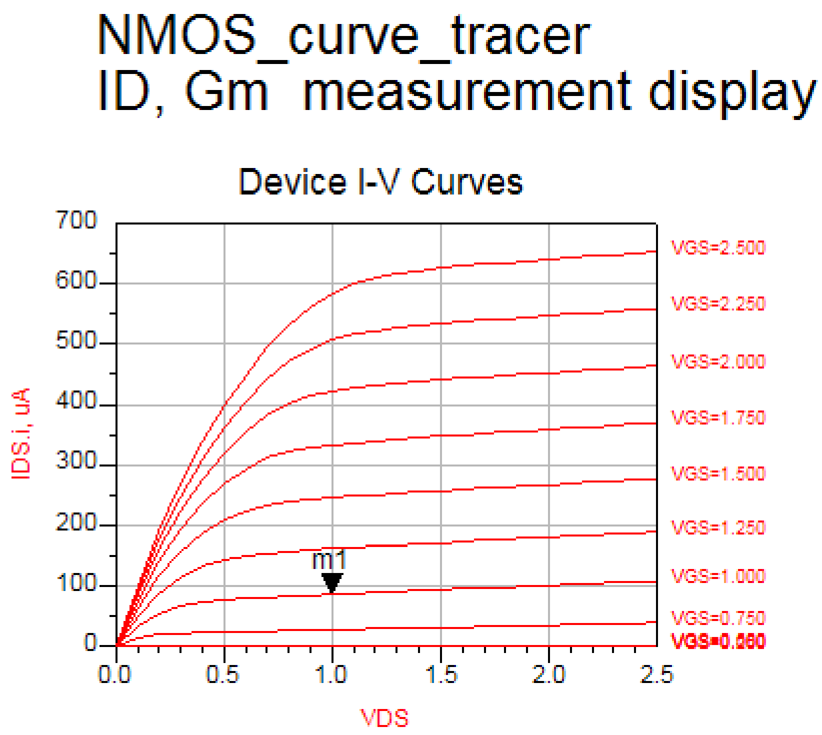
DC
DC1
SweepVar="VDS"

3. Start=0
Stop=2.5
Step=0.1

Set drain voltage sweep limits as needed.

Other=OutVar="MOSFET1.Gm" OutVar="W1"

A curve tracer-like display is plotted in the data display panel:



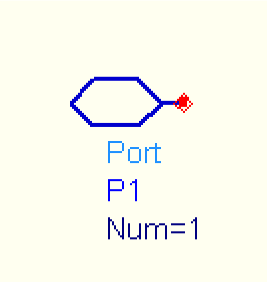
Defining a Subnetwork in ADS:

Subnetworks allow you to take advantage of the heirarchy possible in ADS. You can save circuits or portions of circuits that you plan to reuse as subnetworks which can then be accessed in the Component Library.

Here are the steps:

Begin from your schematic of the circuit that you want to represent as a subnetwork.

1. Insert and label Port connectors from the tool bar. In the example of the inverter subnetwork, Port1 is connected to the input and Port2 to the output.



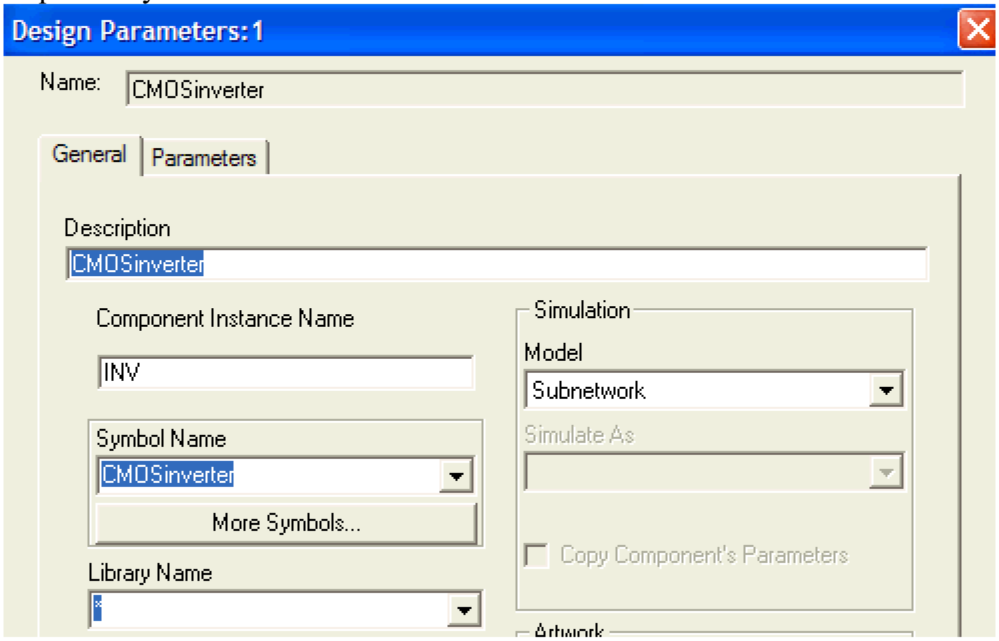
Complete the construction of your schematic for the subnetwork. Note that you will need to include transistor models into the subnetwork if your circuit requires transistors. Name and save the subnetwork.

2. . Create Subnetwork symbol:

View > Create/Edit Schematic Symbol
The Symbol Generator panel opens up. Click on the *Auto Generate* Tab
Unfortunately, there are not logic symbols in the symbol library. Select a dual symbol and Order pins by location.
To return to the schematic, choose *View > Create/Edit Schematic Symbol* (again)
Save the file

3. Name the circuit and set the design parameters
File > Design Parameters

<u>General tab</u>. The component name will be shown, CMOSinverter in this example. Name the component instance. For example: INV When the component is included in a schematic, each instance will be numbered sequentially.



Design Parameters:1

Name: CMOSinverter

Description: CMOSinverter

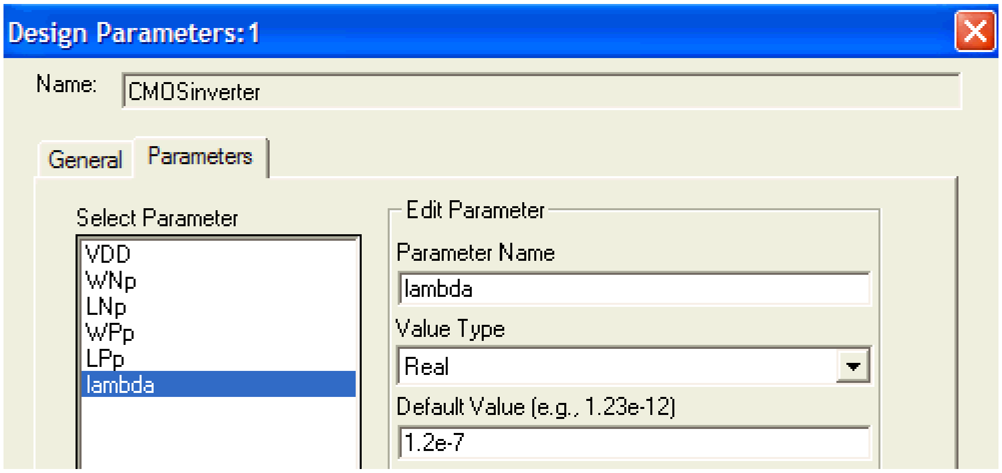
Component Instance Name: INV

Symbol Name: CMOSinverter

Library Name: *

Simulation
Model: Subnetwork
Simulate As:
□ Copy Component's Parameters

5. If you want to allow adjustable parameters from outside the subnetwork, use the Parameters menu tab. This is useful when you want to sweep some parameter that is inside the subnetwork. In this example, 6 parameters are declared to be adjustable. Their values are given a default, but can be specified again outside the model in the schematic where it is being used.



Design Parameters:1

Name: CMOSinverter

Select Parameter

VDD
WNp
LNp
WPp
LPp
lambda

Edit Parameter

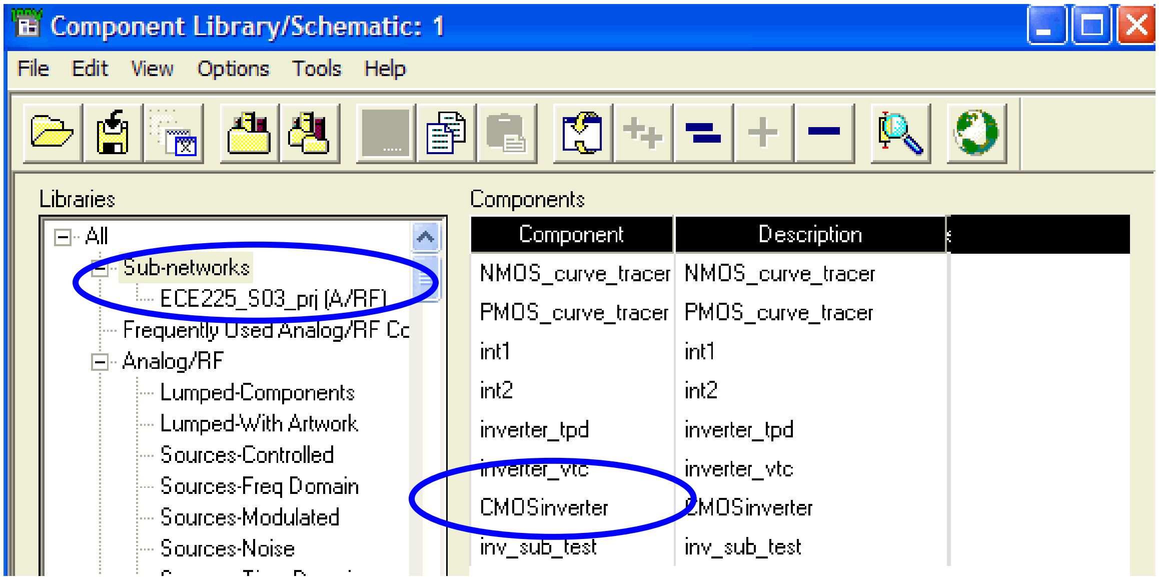
Parameter Name: lambda

Value Type: Real

Default Value (e.g., 1.23e-12): 1.2e-7

6. Save the subnetwork again.

7. To insert your inverter into the schematic, use the component library icon (the bookshelf icon) on the tool bar to open the library. Select your project, then the component you wish to insert. You can then point and click into the schematic.



Component Library/Schematic: 1

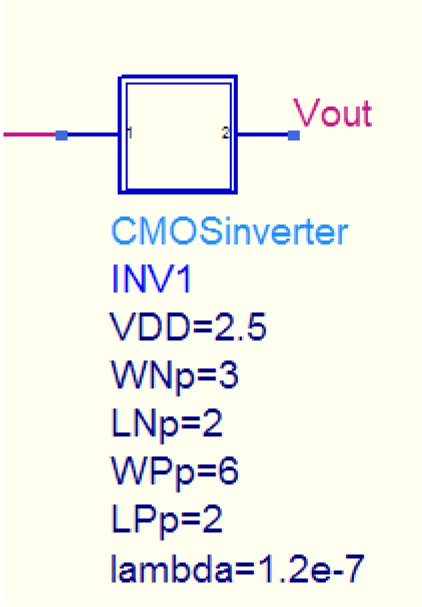
Libraries

- All
  - Sub-networks
    - ECE225_S03_prj (A/RF)
  - Frequently Used Analog/RF Cc
  - Analog/RF
    - Lumped-Components
    - Lumped-With Artwork
    - Sources-Controlled
    - Sources-Freq Domain
    - Sources-Modulated
    - Sources-Noise

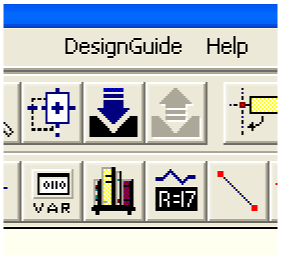
Components

Component	Description
NMOS_curve_tracer	NMOS_curve_tracer
PMOS_curve_tracer	PMOS_curve_tracer
int1	int1
int2	int2
inverter_tpd	inverter_tpd
inverter_vtc	inverter_vtc
CMOSinverter	CMOSinverter
inv_sub_test	inv_sub_test

The symbol appears like this in the schematic:



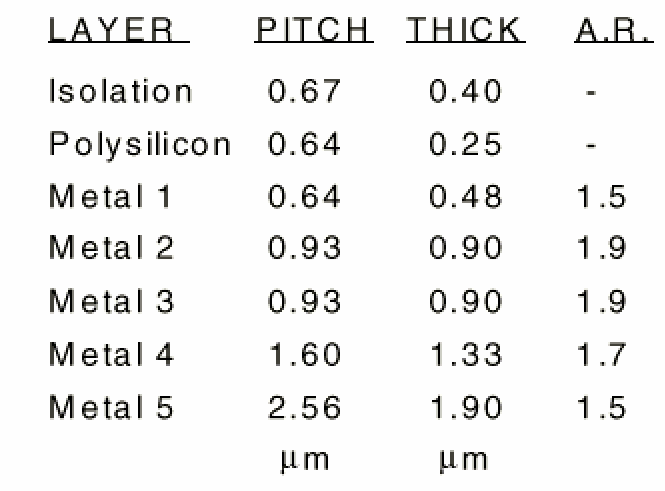
7. You can push into the subnetwork to view or modify it with the down arrow icon on the toolbar.



Interconnect models

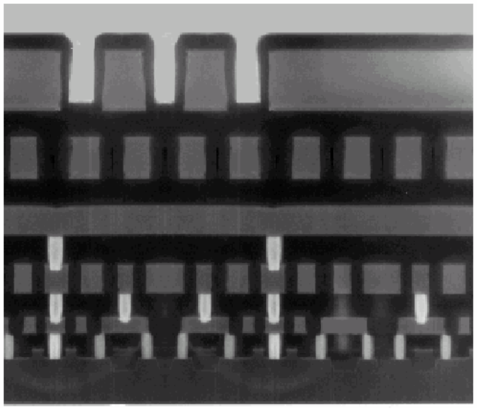
The multilayer substrate model (T-lines – Multilayer) calculates the RLGC relationships between conductors in a multiple metal process. This is a lossy transmission line model that also considers skin effect losses. Using this with the single or coupled lines allows the simulation of interconnect delays and power or ground inductance effects on circuit performance. Refer to the int2 schematic in the ECE225_S03 ADS example file project.

Interconnect metal conductivity and thickness and dielectric constant and thickness must be known and provided as inputs to the MLSUBSTRATEx model specification (where x = number of metal layers + 1). In the example below from Rabaey, Chandrakasan, and Nikolic[1], a cross section of a 5 layer metal process is shown along with a table describing conductor thicknesses. Using the conductor thickness as a scale, one can estimate the dielectric thicknesses. It is assumed that the first dielectric layer is SiO_2 while subsequent ones may have a reduced dielectric constant of about 3 (perhaps polyimide).



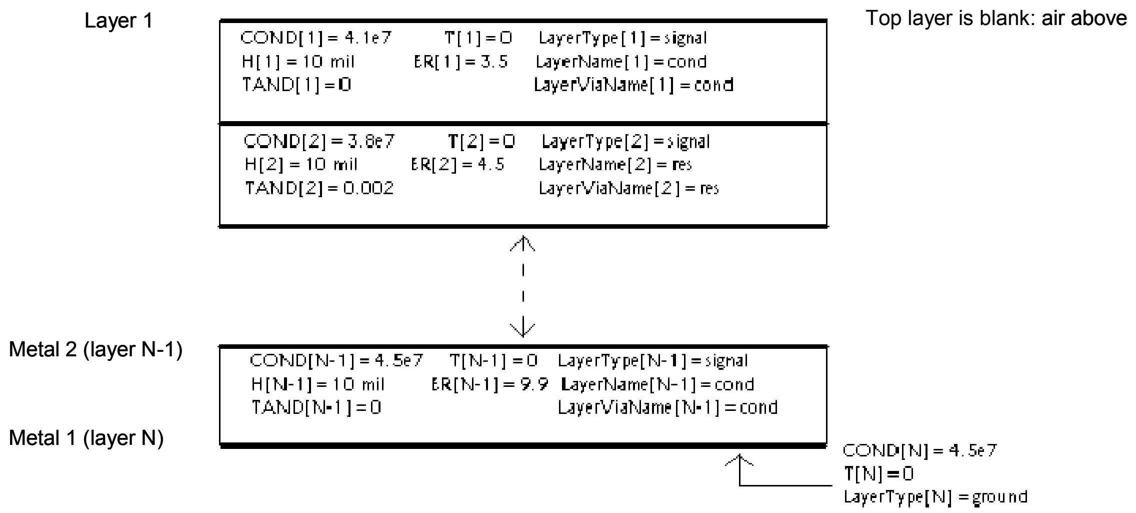
LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

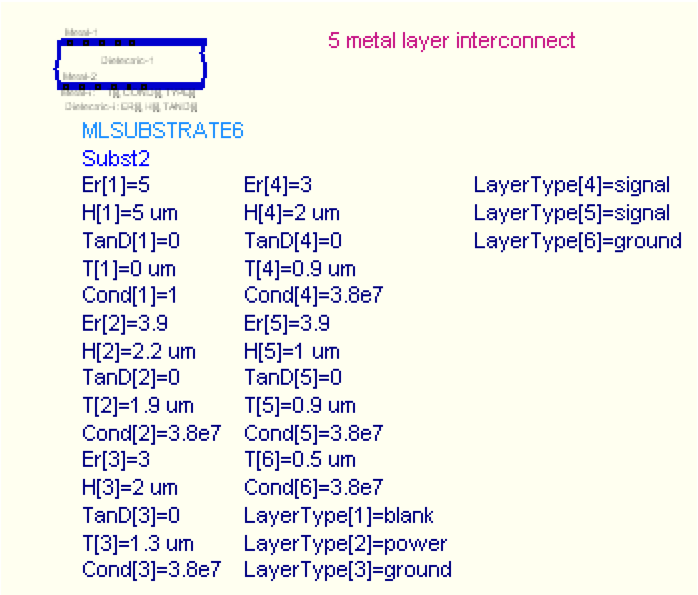
Layer pitch, thickness and aspect ratio



The model parameters assign the highest layer number to the bottom layer. In this example, Metal 1 is assigned as a ground plane for signal conductors on Metals 2 and 3. M4 is assigned as another ground distribution plane and M5 is power. Note that it is possible to route longer interconnects on M4 or M5 if needed using a coplanar strip transmission line topology.

[1] J. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits: A Design Perspective, Second Ed., Prentice-Hall/Pearson, 2003.





MLSUBSTRATE6
Subst2
Er[1]=5
H[1]=5 um
TanD[1]=0
T[1]=0 um
Cond[1]=1
Er[2]=3.9
H[2]=2.2 um
TanD[2]=0
T[2]=1.9 um
Cond[2]=3.8e7
Er[3]=3
H[3]=2 um
TanD[3]=0
T[3]=1.3 um
Cond[3]=3.8e7
Er[4]=3
H[4]=2 um
TanD[4]=0
T[4]=0.9 um
Cond[4]=3.8e7
Er[5]=3.9
H[5]=1 um
TanD[5]=0
T[5]=0.9 um
Cond[5]=3.8e7
T[6]=0.5 um
Cond[6]=3.8e7
LayerType[1]=blank
LayerType[2]=power
LayerType[3]=ground
LayerType[4]=signal
LayerType[5]=signal
LayerType[6]=ground

MLnCTL_C (T-lines – Multilayer) is used to represent single or coupled lines. The parameter n represents the number of lines. Constant width and spacing is assumed and all conductors must be on the same metal layer.

MLnCTL_V allows for variable widths, spacings, and conductors can be on different layers.