A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance

Alex R. Bugeja, *Member, IEEE*, Bang-Sup Song, *Fellow, IEEE*, Patrick L. Rakers, *Member, IEEE*, and Steven F. Gillig, *Member, IEEE*

***Abstract*— A 14-bit, 100-MS/s CMOS digital-to-analog converter (DAC) designed for spectral performance corresponding more closely to the 14-bit specification than current implementations is presented. This DAC utilizes a nonlinearity-reducing output stage to achieve low output harmonic distortion. The output stage implements a return-to-zero (RZ) action, which tracks the DAC once it has settled and then returns to zero. This RZ circuit is designed so that the resulting RZ waveform exhibits high dynamic linearity. It also avoids the use of a hold capacitor and output buffer as in conventional track/hold circuits. At 60 MS/s, DAC spurious-free dynamic range is 80 dB for 5.1-MHz input signals and is down only to 75 dB for 25.5-MHz input signals. The chip is implemented in a 0.8-μm CMOS process, occupies 3.69 $\times$ 3.91 mm^2 of die area, and consumes 750 mW at 5-V power supply and 100-MS/s clock speed.**

***Index Terms*—CMOS analog integrated circuits, digital–analog (D/A) conversion, D/A converters, dynamic linearity.**

I. Introduction

DIGITAL–ANALOG converters (DAC's) are essential components of a large number of modern communications systems, such as wired and wireless transmitters, direct digital synthesis, arbitrary waveform generations, and local oscillators [1], [2]. In such applications, the key performance parameter of the DAC is its spectral purity, i.e., the level of spurious frequency components present in the DAC output signal. Typically, spurs in the output spectrum are harmonically related to the input signal in some way and are generated due to dynamic nonlinearities in the DAC output response. Spectral purity is required in the applications described because of the effect these spurs have on the information content of the DAC output signal. For example, in transmitting a frequency-division-multiplexed signal, the tones within one channel may give rise to harmonic tones in adjacent channels, causing information corruption. The spectral purity of a DAC is typically measured by means of its spurious-free dynamic range (SFDR) for a range of sinusoidal/multitone input signals and for a range of clock update rates.

Manuscript received April 9, 1999; revised July 8, 1999. This work was supported by the National Science Foundation under Grant MIP97-11010.

A. R. Bugeja was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA. He is now with Texas Instruments, Dallas, TX 75243 USA.

B.-S. Song was with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA. He is now with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093 USA.

P. L. Rakers and S. F. Gillig are with Motorola Corp., Schaumburg, IL 60196 USA.

Publisher Item Identifier S 0018-9200(99)09010-1.

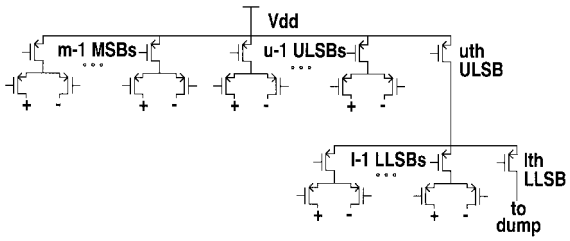


Fig. 1. Conventional DAC architecture.

For high-speed and high-resolution applications (>10 bits, >50 MHz), the current source switching architecture is preferred since it can drive a resistive load directly without the need for a voltage buffer. A conventional high-performance DAC architecture as used in such applications is shown in Fig. 1. As shown in Fig. 1, the DAC consists of $m-1$ thermometer (linearly) decoded most significant bits (MSB's), $u-1$ thermometer decoded upper least significant bits (ULSB's), and $l-1$ binary decoded lower least significant bits (LLSB's). The current sources, which are implemented differentially, are taken directly to a pair of differential resistive loads. Modern high-speed and high-resolution DAC's all use variations of this basic architecture [1], [3]–[7]. The ULSB/LLSB array is sometimes driven by an mth MSB to ensure the sum of the LSB's is one MSB. Also, the ULSB's are sometimes omitted, so that the DAC has an upper array of thermometer decoded bits (MSB's) and a lower array of binary decoded bits (LSB's). Thermometer decoding has the well-known advantages of monotonicity and reduction of glitch at major carries, but full thermometer decoded architectures are impractical to implement for high resolution [3], [5].

The static performance of such DAC's is well characterized by traditional measures such as integral nonlinearity (INL) and differential nonlinearity (DNL), and various techniques have been used to attain full n-bit static linearity for n-bit DAC's. In particular, such techniques have included sizing the devices appropriately for intrinsic matching and utilizing certain layout techniques [4], [7], trimming [3], [6], calibration [8], [9], and dynamic element matching/averaging techniques [10]. The dynamic performance of current-switched DAC's, however, has not scaled in proportion to the number of their bits. In particular, examination of the references will show dynamic performance as measured by SFDR falling off rapidly with increasing signal frequency. Effectively, the larger number of bits only gives lower quantization noise at higher signal frequencies, not higher SFDR. There are several causes for

this behavior; the major ones are summarized below.

1) *Code-dependent settling time constants:* The time constants of the MSB's, ULSB's, and LLSB's are typically not proportional to the currents switched; the problem is worse if $R/2R$ ladders are employed in place of current dividers [11].
2) *Code-dependent switch feedthrough:* This results due to signal feedthrough across switches that are not sized proportionately to the currents they are carrying, and therefore shows up as code-dependent glitches at the output.
3) *Timing skew between current sources:* Imperfect synchronization of the control signals of the switching transistors will cause dynamic nonlinearities [4]. Synchronization problems occur because of both delays across the die and improperly matched switch drivers. Thermometer decoding can make the time skew worse because of the larger number of segments [3].
4) *Major carry glitch:* This can be minimized by thermometer decoding, but in higher resolution designs, where full thermometer decoding is not practical, it cannot be entirely eliminated [5].
5) *Current source switching:* Voltage fluctuations occur at the internal switching node at the sources of the switching devices [4], [12]; since the size of the fluctuation is not proportional to the current's being switched, it again gives rise to a nonlinearity.
6) *On-chip passive analog components:* Drain/source junction capacitances are nonlinear; on-chip analog resistors also exhibit nonlinear voltage transfer characteristics. These devices therefore cause dynamic nonlinearities when they occur in analog signal paths.
7) *Mismatch considerations:* Device mismatch is usually considered in discussions of static linearity, but it also contributes to dynamic nonlinearity because switching behavior is dependent on switch transistor parameters such as threshold voltage and oxide thickness. These differ for devices at different points on the die [13], [14], introducing code dependencies in the switching transients.

Dynamic nonlinearities increase in magnitude with increasing signal frequency since the outputs change value more frequently and a larger proportion of the clock cycles is occupied by nonlinear switching transients. This explains the pronounced frequency degradation of SFDR observed for the DAC's cited above.

Alternatives to the current-mode DAC have been proposed in the literature (for example, [15]), but they are limited by the use of op-amps and/or low-impedance followers as output buffers. Op-amps introduce several dynamic nonlinearities of their own, owing to their nonlinear transconductance transfer functions (slew limiting in the extreme case). High-gain op-amps connected in feedback configurations also require buffers to drive lower impedance resistive loads. Buffers introduce further distortion, due to factors such as signal dependence of the bias current in the buffer devices and nonlinear buffer output resistance.

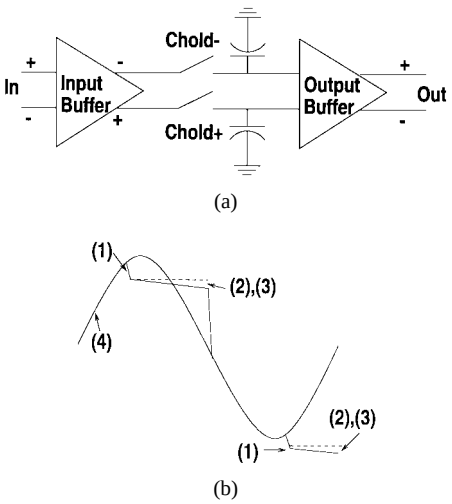


Fig. 2. Problems of classic track/hold circuits.

One conceptual solution to the dynamic linearity problem is to eliminate the dynamic nonlinearities of the DAC, all of which are associated with the switching behavior, by placing a track/hold circuit at the DAC output. The track/hold would hold the output constant while the switching is occurring, and track once the current sources have settled to their dc value. Thus, only the static characteristics of the DAC would show up at the output, and the dynamic ones would be attenuated or eliminated. The problem with this approach is that the track/hold circuit in practice introduces dynamic nonlinearities of its own, which tend to be comparable to or worse than those of the DAC alone. Some of the problems associated with track/hold circuits are now discussed.

Fig. 2(a) shows a classic track/hold architecture composed of an input buffer, a hold capacitor, and an output buffer. The hold capacitor is switched to the input buffer during the track phase and disconnected during the hold. References [16] and [17] are examples of this basic open-loop architecture. The closed-loop implementation involves closing the loop from the outputs of the output buffer to the inputs of the input buffer and is therefore implemented in a pseudodifferential form [18]; in such circuits the hold capacitance is typically the Miller feedback capacitance across the output stage. These circuits suffer from a number of drawbacks with respect to dynamic linearity, as also annotated in Fig. 2(b) (adapted from [16]).

1) *Track-to-hold step [(1) in Fig. 2(b)]:* This involves the pedestal error on the hold capacitor when the switch changes from track to hold, which is nonlinear in some way depending on the switch charge characteristic. The closed-loop approach minimizes this error by keeping the inputs of the output buffer at virtual ground.
2) *Droop rate error (2):* This is a problem if bipolar inputs are used for the output buffer; the signal dependence of the droop rate will cause dynamic nonlinearities.
3) *Hold-mode feedthrough (3):* This involves the feedthrough transfer function in hold mode; it introduces a nonlinearity even if this transfer function is signal independent because of the nonlinear behavior of the DAC during the hold mode. Feedthrough can occur

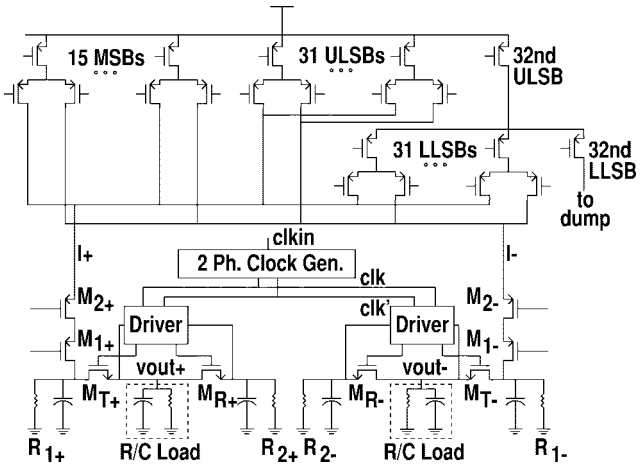


Fig. 3. Return-to-zero high-speed DAC.

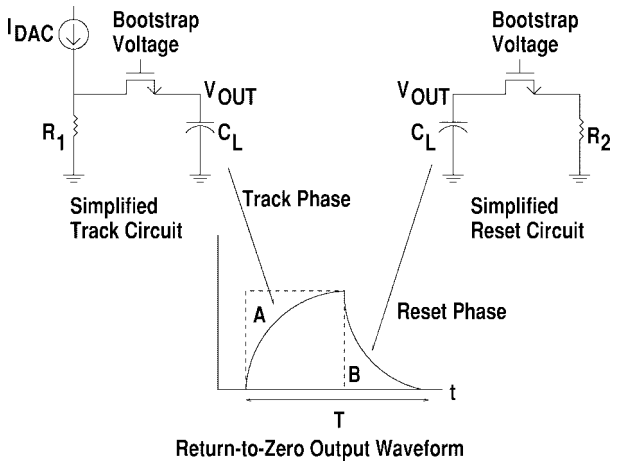


Fig. 4. Return-to-zero action.

across the switch; in closed-loop architectures, this feedthrough also can occur across the input differential pair.

4) *Track mode errors (4):* Typically, these are the largest source of nonlinearities; they mainly involve nonlinear settling behavior of the buffers. In the open-loop case, the distortion is due to signal dependence of the bias current in the buffer devices, nonlinear transconductance transfer functions, nonlinear device output resistance, etc. In the closed-loop case, the buffers are op-amps and suffer from the dynamic nonlinearities associated with op-amps as already described above.

For these reasons, track/hold circuits are not employed at the outputs of modern high-speed and high-resolution DAC's. A different approach, employing a return-to-zero (RZ) circuit at the output, is proposed here. This approach avoids the use of buffers and hold capacitors in the output signal path and is implemented in a form that exhibits unique advantages for dynamic linearity. We discuss the architecture of this circuit in Section II. In Section III, practical details of the circuit implementation are presented. Section IV presents measurement results on the test chip, and Section V presents conclusions.

II. Return-to-Zero Architecture

The architecture of the 14-bit DAC presented here is shown in Fig. 3. The top part of the figure shows that the circuit employs a switched current DAC composed of 15 thermometer decoded MSB's corresponding to the upper four input bits, followed by 31 thermometer decoded ULSB's corresponding to the middle five input bits, and finally five binary decoded LLSB's corresponding to the lower five input bits. The differential outputs of this DAC I_+ and I_- are taken to a differential output stage, which is designed to enhance the DAC dynamic linearity. On either side of the differential circuit, the current is brought down through a double cascode formed by M_{2+}, M_{2-} and M_{1+}, M_{1-} to the on-chip resistive loads R_{1+}, R_{1-}. The circuit operates with two phases in each clock cycle, a track phase and a reset phase, corresponding in timing to the track phase and hold phases of a track/hold circuit. The on-chip resistive loads R_{1+}, R_{1-} are connected to the output R/C loads via the track switches M_{T+}, M_{T-} during the track phase, when the reset switches M_{R+}, M_{R-} are off. During the reset phase, the track switches are off and the reset switches are used to discharge the R/C loads to ground via the on-chip resistive loads R_{2+}, R_{2-}.

The circuit operation is controlled by means of a two-phase clock generator, which feeds the driver circuits shown in Fig. 3. These driver circuits bootstrap the gates of the track and reset switches to their sources during the track and reset phases, respectively, and control the gate-to-source voltage of these switches to maximize the dynamic linearity. The details of this action will be described in the next section.

The RZ action is explained further in Fig. 4, where T denotes the clock period. Simplified circuits for the track and reset phases are shown, with the DAC output current $I_{\rm DAC}$ driving R_1 on the track side. With the switching sequence described, the output waveform shown in Fig. 4 results. The ideal RZ output is of course a square waveform composed of the signal value during the track and zero during the reset. In practice, transient errors are made during both track and hold with respect to this ideal, and are represented in Fig. 4 by the error areas A and B, respectively. These errors do not result in dynamic nonlinearity if they are linear with respect to the signal. For example, if the switches were ideal and nonlinear parasitics were absent, the waveform would be composed of an ideal exponential of time constant determined by R_1, R_2, and C_L. Details of the steps taken to ensure the highest possible dynamic linearity from this circuit are discussed in the next section.

The timing of the clock waveforms driving the switches (through the bootstrap drivers) is important. A nonoverlapping clock driver drives the latches for the current switching DAC, while a complementary clock drives the bootstrap drivers. Care was taken to ensure that 1) the reset-to-track switch occurs only when the current sources have settled sufficiently to give the desired dynamic linearity and 2) the track-to-reset switch precedes the current switching of the next clock cycle, hence avoiding distortion from the transient of the next cycle from spilling into the current cycle.

Fig. 5 compares the time- and frequency-domain characteristics of an ideal conventional full-waveform DAC with

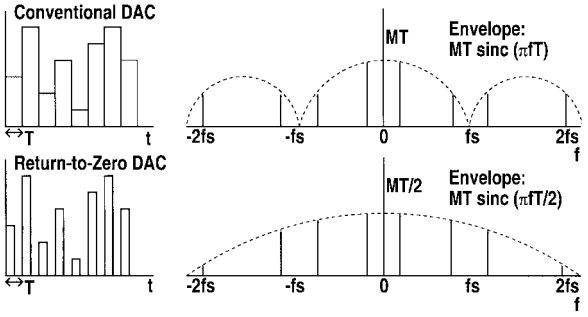


Fig. 5. Spectral comparison.

those of an ideal RZ DAC. The input signal to the DAC's is a sinusoid of frequency $f_{\rm IN}$ and magnitude M. From the time-domain waveforms, it is clear that the conventional DAC outputs each quantized signal for twice as long as the RZ DAC; this shows up in the frequency domain as a halving of the magnitude of the frequency envelope in the case of the RZ DAC. The RZ DAC therefore will have less output signal power. However, as also shown in the figure, the $\sin(x)/x$ distortion is less pronounced in the case of the RZ DAC. In the case of the conventional DAC, the $\sin(x)/x$ envelope has nulls at sampling rate multiples, and the droop is 3.9 dB at half the sampling frequency [19]. In the case of the RZ DAC, the envelope has nulls at multiples of twice the sampling rate, and the droop at half the sampling frequency is only 0.9 dB. In many communication systems, the droop due to the conventional DAC is not acceptable and must be corrected by an inverse sinc filter or equalizer [11]; construction of such a system for high-speed operation is not a trivial task [19]. The flatter envelope of the RZ DAC results in less droop distortion and allows the filter/equalizer to be eliminated entirely in many cases.

Fig. 6 compares an RZ output voltage waveform with a track/hold waveform on the basis of charge injection error at switch turnoff (pedestal error), ignoring all other factors. We assume that in both circuits, this charge is not taken up by a dummy switch (or the reset switch in the case of the RZ circuit); if such switches are present, the argument applies equally well for the uncancelled portion of the charge. The track/hold output can be seen to have effectively twice the signal output of the RZ output, since there is no return of the signal to zero during hold. However, the charge injection also results in an error during the second half of the clock cycle given by (1)

$$\text{Error} = \frac{T \times Q_{\rm INJ}}{2C_L} \tag{1}$$

where C_L is the load capacitance.

In the case of the RZ circuit, the error decays approximately exponentially with the circuit time constant τ, along with the signal itself. From the figure, the signal output is halved with respect to the track/hold circuit, but the error during the second half of the clock cycle due to the charge injection is now given by (2)

$$\text{Error} = \frac{\tau \times Q_{\rm INJ}}{C_L}\left(1 - e^{-T/2\tau}\right). \tag{2}$$

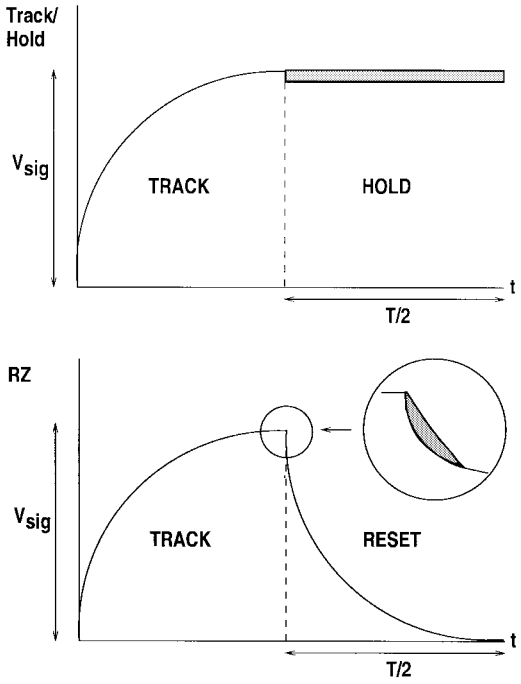


Fig. 6. RZ versus track/hold.

For $\tau \leq (T/2)/2$, we can approximate the error as $\tau \times Q_{\rm INJ}/C_L$. In practice, we design for $\tau \approx (T/2)/10$, so that the charge injection error is about ten times smaller than the track/hold case. Thus, the ratio of the charge injection to the signal is diminished by an overall factor of $5\times$ when we include the halving of the signal output for the RZ case.

III. Circuit Implementation

In this section, we examine the circuit implementation of the DAC in more detail, as well as the advantages that accrue from this particular implementation.

A. Choice of Switch Device

Consider the output circuit schematic shown in Fig. 3. The track and reset switches M_{T+}, M_{T-}, M_{R+}, and M_{R-} are implemented using minimum-length NMOS devices operating in the linear region. The important performance parameters of these switches from the dynamic linearity viewpoint can be summarized as being the on-resistance $R_{\rm ON}$, the channel charge $Q_{\rm CH}$, and the junction capacitance C_J. All of these parameters scale with switch size; in the N-well process used ($K_{\rm NMOS} \approx 3 \times K_{\rm PMOS}, K = \mu_0 C_{\rm OX}$), the use of NMOS devices optimizes the switch size as compared to PMOS devices. For the same device dimensions, the NMOS device will have lower $R_{\rm ON}$ than the PMOS device while exhibiting similar $Q_{\rm CH}$ and C_J to first order. Equivalently, it is possible to attain the same $R_{\rm ON}$ with smaller dimensions in the NMOS case, hence benefitting from smaller $Q_{\rm CH}$ and C_J. The designed switch size of the NMOS switches was 200 μ/0.8 μ.

The use of NMOS devices has an impact on the design of the rest of the DAC. If folding is to be avoided (this gives a simpler implementation, a slight improvement in circuit speed,

and smaller area/power consumption), the current sources then have to be implemented in PMOS, as shown in Fig. 3. This is beneficial because these devices have a lower gm, and spurious fluctuations in their gate bias voltages will thus have less effect than with NMOS current sources. The PMOS devices are also isolated in a well and better shielded from substrate noise.

B. $(V_{\rm GS} - V_{\rm TH})$-Dependent Switch Operation

The $(V_{\rm GS} - V_{\rm TH})$ term has an important bearing on the linearity performance of the MOS switches and the way in which this was controlled is now described. We first consider the threshold voltage $V_{\rm TH}$. Using the first-order model for devices with grounded bulk nodes, we can express this as

$$V_{\rm TH} = V_{\rm TH_0} - \gamma\sqrt{2\phi_f} + \gamma\sqrt{2\phi_f + V_S} \tag{3}$$

where V_S is the source voltage of the NMOS switches and the other symbols have their usual meanings. Expanding (3) in series form, we obtain

$$V_{\rm TH} = V_{\rm TH_0} + \gamma\left[\frac{V_S}{2(2\phi_f)^{1/2}} - \frac{V_S^2}{8(2\phi_f)^{3/2}} + \cdots\right]. \tag{4}$$

The coefficient of the second-order term is approximately five times smaller than that of the first-order term, and for the range of V_S values encountered in the RZ circuit, we can model $V_{\rm TH}$ by the linear approximation

$$V_{\rm TH} = V_{\rm TH_0} + k_1 V_S \tag{5}$$

where $k_1 = \gamma/[2(2\cdot\phi_f)^{1/2}]$ is a constant ($k_1 < 1$).

Consider now the first-order models for $R_{\rm ON}$ and $Q_{\rm CH}$

$$R_{\rm ON} = \frac{1}{\mu_0 C_{\rm OX}(W/L)(V_{\rm GS} - V_{\rm TH})} \tag{6}$$

$$Q_{\rm CH} = -(WLC_{\rm OX})(V_{\rm GS} - V_{\rm TH}). \tag{7}$$

From (6) and (7), we can see that a constant $(V_{\rm GS} - V_{\rm TH})$ will to first-order lead to signal independence of both $R_{\rm ON}$ and $Q_{\rm CH}$ and is therefore desirable. Signal dependence of $R_{\rm ON}$, in particular, leads to signal-dependent time constants and hence signal-dependent settling transients in the output. To solve this problem, bootstrapping is introduced into the switching circuit. The gates of the switches are bootstrapped to retain $V_{\rm GS} = k_2 + k_1 V_S$, where k_2 is the constant component of the overall $V_{\rm GS}$ after bootstrapping. Combining this with the linear model of (5), we therefore obtain that $(V_{\rm GS} - V_{\rm TH})$ is constant.

The bootstrapping circuit is shown in Fig. 7. This bootstrapping circuit is implemented differentially; only one of the two circuits is shown in Fig. 7. The track switch source and the reset switch source each drive buffers to protect the source nodes from the bootstrap transients. The buffers are each composed of a low impedance output differential pair driven by a level-shifting source follower input stage. This simple arrangement gives the required tracking speed at the expense of power consumption. As also shown in Fig. 3, for the track switch, the source node is the output node during the track phase, and for the reset switch, the source node is the node connected to the on-chip resistor R_{2+}, R_{2-} during the reset phase. The buffer gain is close to unity and is set so as to achieve $V_{\rm GS} = k_2 + k_1 V_S$. The buffer gain also includes

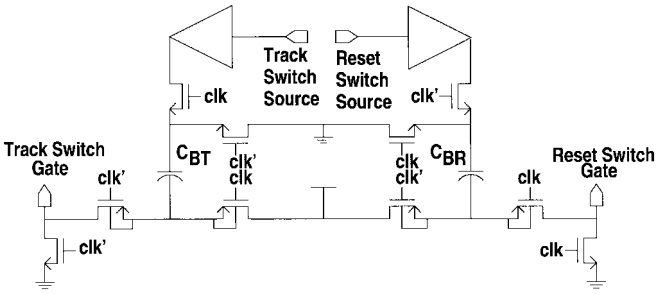


Fig. 7. Bootstrapping circuit.

compensation for the capacitive divider loss, which results in bootstrapping due to the gate capacitance of the switches. When the clk signal is low, the bootstrap capacitor $C_{\rm BT}$ on the track side is precharged to supply voltage. During clk high, the gate of the track switch is driven to the buffer output plus the bootstrapped supply voltage across the capacitor, less the linear gain loss of the capacitive potential divider. The switches on the reset side are driven by complementary clock signals, so that the track and reset switches behave in complementary fashion, as required for proper RZ action.

A simulation of the $(V_{\rm GS} - V_{\rm TH})$ behavior is shown in Fig. 8. In this simulation, which extends over two clock cycles at 60 MS/s, the RZ output stage is run for a minimum output signal in the first clock cycle and for a maximum output signal in the second. Each clock cycle consists of a track phase followed by a reset phase. The value of $(V_{\rm GS} - V_{\rm TH})$ is plotted against time for both the track and reset switches, resulting in the two waveforms shown in Fig. 8. It can be seen that the bootstrapping circuit attains its goal of keeping the value of $(V_{\rm GS} - V_{\rm TH})$ approximately constant independent of the source voltage value. This constant behavior is maintained both between the track and reset clock phases and between the minimum and maximum signal clock cycles.

C. Nonlinearity Cancellation

The effect of the drain-to-source voltage variation on the switch behavior is now considered. We first refine (6) to show that $V_{\rm DS}$ has an effect on the value of $R_{\rm ON}$

$$R_{\rm ON} = \frac{1}{\dfrac{\partial I_D}{\partial V_{\rm DS}}} = \frac{1}{\mu_0 C_{\rm OX}(W/L)(V_{\rm GS} - V_{\rm TH} - V_{\rm DS})}. \tag{8}$$

Thus, although keeping $(V_{\rm GS} - V_{\rm TH})$ constant as just described is necessary to keep $R_{\rm ON}$ constant, the effect of the $V_{\rm DS}$ term must also be accounted for to attain the highest linearity performance. Furthermore, since the switches are implemented using minimum-length devices to minimize the value of the overall switch size for a given $R_{\rm ON}$, the signal-dependent $V_{\rm DS}$ value of the switches is a cause for concern, since any short channel effects that depend on the $V_{\rm DS}$ value could cause nonlinearities. This signal dependence of $V_{\rm DS}$ is a fundamental feature of the switch action, and we cannot design to eliminate it as with $(V_{\rm GS} - V_{\rm TH})$. For any finite switch resistance, some portion of the signal appears across the track switch during the track phase and across the reset switch during the reset phase. This portion

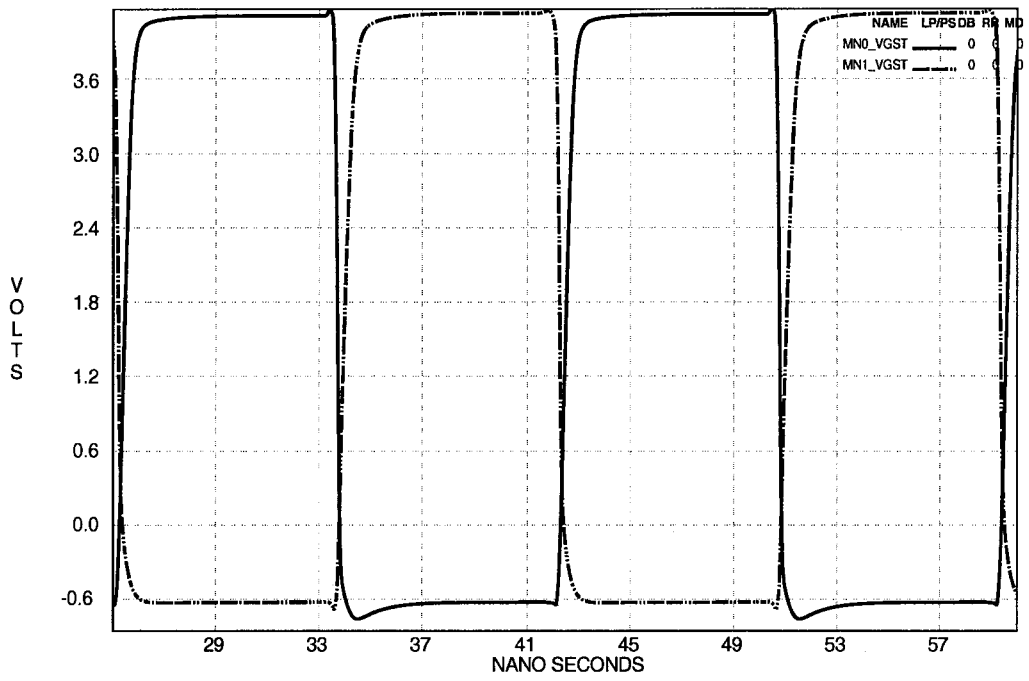


Fig. 8. Bootstrap circuit simulation.

of the signal is minimized by making the switches larger, but very large switches will cause problems with charge injection and source/drain nonlinear junction capacitances, besides providing a larger load for the bootstrap driver circuit.

To solve this problem, the behavior of the $V_{\rm DS}$ waveform during the track phase was made symmetrical to that of the reset phase, within device matching limits. In the output stage circuit shown in Fig. 3, this is done by matching the reset path to the track path, i.e., the track and reset switches are made identical, as well as devices R_{2+} and R_{2-}. The effect of this is now discussed.

With constant $(V_{\rm GS} - V_{\rm TH})$, (8) reduces to

$$R_{\rm ON} = \frac{1}{c_1 + c_2 V_{\rm DS}} \tag{9}$$

where $c_1 = \mu_0 C_{\rm OX}(W/L)(V_{\rm GS} - V_{\rm TH})$ and $c_2 = -\mu_0 C_{\rm OX}(W/L)$ are constants. The signal dependence of the switch has therefore been reduced to the $V_{\rm DS}$ dependence. Consider the track and reset half-circuits shown in Fig. 9, where we are first assuming a purely capacitive load C_L. In these half-circuits, we have used a Thévenin's equivalent circuit to express the DAC current ($I_{\rm DAC}$ in Fig. 4) and the resistance R_1 as the series combination of the voltage source $V = I_{\rm DAC}R_1$ and the resistance $R = R_1 = R_2$. The switch is denoted by its on-resistance value $R_{\rm ON} = R_{\rm ON}(V_{\rm DS})$. In the track half-circuit, this is the on-resistance of the track switch; in the reset half-circuit, this is the on-resistance of the reset switch.

We would like to obtain the $V_{\rm DS}$ value of the track switch during the track phase $(V_{\rm DS_{TRACK}}(t))$ and the $V_{\rm DS}$ value of the reset switch during the reset phase $(V_{\rm DS_{RESET}}(t))$ and compare the two. For the track half-circuit, we can see that $V_{\rm DS_{TRACK}} = C_L(dV_S/dt)R_{\rm ON}$ and also that $V_{\rm DS_{TRACK}} = (V - V_S)(R_{\rm ON}/R + R_{\rm ON})$. Combining these two equations,

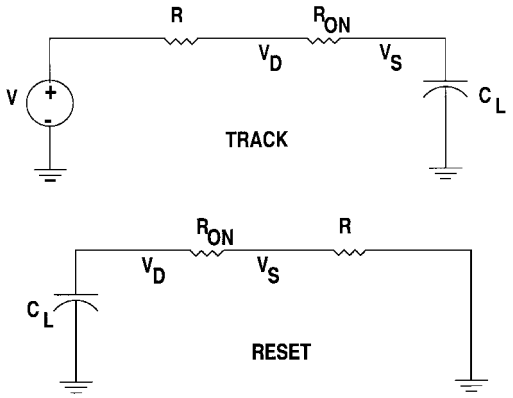


Fig. 9. Track and reset half-circuits.

we obtain the nonlinear differential equation

$$V_{\rm DS_{TRACK}} = -C_L R_{\rm ON}\frac{d}{dt}\left(V_{\rm DS}\left(\frac{R + R_{\rm ON}}{R_{\rm ON}}\right)\right) \tag{10}$$

with the initial condition

$$V_{\rm DS_{TRACK}}|_{t=0} = V\frac{R_{\rm ON}}{R + R_{\rm ON}} \tag{11}$$

where we have taken the time axis independent variable t to be zero at the start of the track phase; at this point $V_S = 0$. It is not necessary to solve (10) explicitly to obtain the $V_{\rm DS_{TRACK}}$ waveform. An equally useful result for our purposes is obtainable by deriving the equivalent equations for the reset case. For the reset half-circuit in Fig. 9, we can see that $V_{\rm DS_{RESET}} = -C_L(dV_D/dt)R_{\rm ON}$ and also that $V_{\rm DS_{RESET}} = V_D(R_{\rm ON}/R + R_{\rm ON})$. (Note that during the reset phase, the drain and source nodes are inverted with respect to the track phase as shown in Fig. 9.) Combining these two

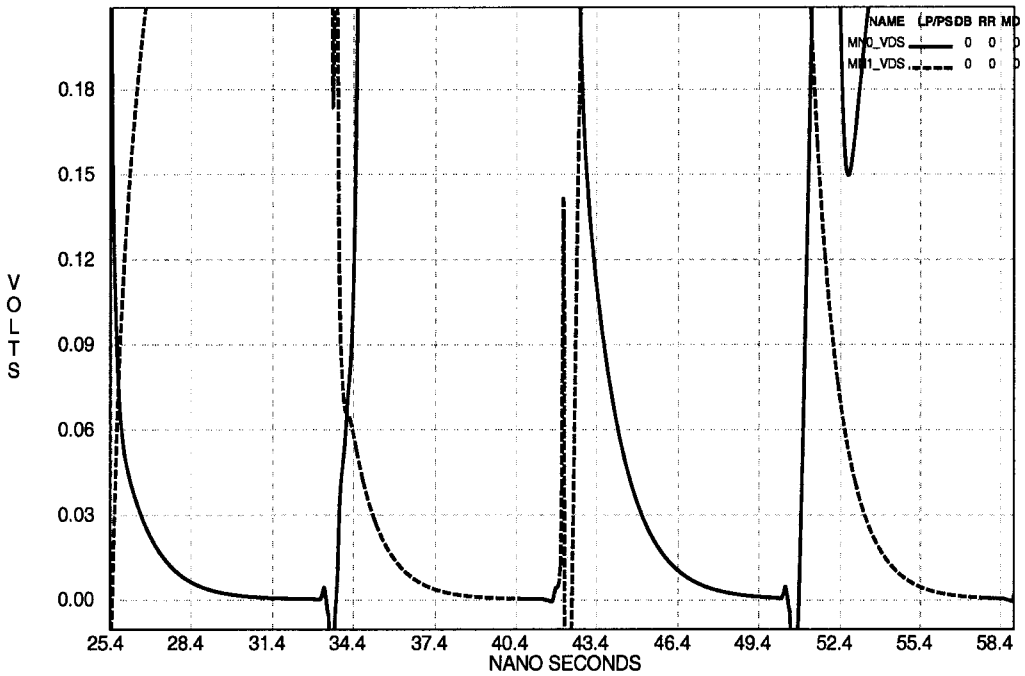


Fig. 10. Simulation of nonlinearity cancellation.

equations, we obtain the nonlinear differential equation

$$V_{\mathrm{DS_{RESET}}} = -C_L R_{\mathrm{ON}} \frac{d}{dt}\left(V_{\mathrm{DS}}\left(\frac{R+R_{\mathrm{ON}}}{R_{\mathrm{ON}}}\right)\right) \tag{12}$$

with the initial condition

$$V_{\mathrm{DS_{RESET}}}|_{t=0} = V\frac{R_{\mathrm{ON}}}{R+R_{\mathrm{ON}}} \tag{13}$$

where we have now taken t to be zero at the start of the reset phase. Comparing (10) with (12) and (11) with (13), we note that $V_{\mathrm{DS_{TRACK}}}(t)$ and $V_{\mathrm{DS_{RESET}}}(t)$ have the same differential equation with the same initial condition, so we conclude that $V_{\mathrm{DS_{TRACK}}}(t)$ and $V_{\mathrm{DS_{RESET}}}(t)$ are identical time functions. This means that the switch drain-to-source voltage behaves in identical ways during track and reset: the V_{DS} value at some point t during track is identical to the V_{DS} value at point $t+(T/2)$ during reset.

Intuitively, we can see from Fig. 9 that the initial values of $V_{\mathrm{DS_{TRACK}}}$ and $V_{\mathrm{DS_{RESET}}}$ are equal, since the initial capacitor voltage is zero in the track phase and V in the reset phase. The initial circuit in both cases is thus a voltage source of value V connected to a potential divider formed by R and R_{ON}. Hence we obtain the initial conditions of (11) and (13). Thereafter, if we consider infinitesimal time increments after the $t=0$ point, we see that in each time increment the circuit is linearized to an R/C circuit, where the capacitance is C_L, and the resistance is the instantaneous value of $R+R_{\mathrm{ON}}$. The change in capacitor value during each time instant is the therefore identical in track and reset intervals spaced $T/2$ apart. This being the case, the value of R_{ON} for corresponding time instants must be equal, and we can extrapolate this argument to see that $V_{\mathrm{DS_{TRACK}}}(t)$ and $V_{\mathrm{DS_{RESET}}}(t)$ have to be identical, as proven above.

A simulation of the V_{DS} behavior is shown in Fig. 10. In this simulation, which extends over two clock cycles at 60 MS/s, the RZ output stage is run for a minimum output signal in the first clock cycle, and for a maximum output signal in the second, as in Fig. 8, and again each clock cycle consists of a track phase followed by a reset phase. The value of V_{DS} is plotted against time for both the track and reset switches, resulting in the two waveforms shown. It can be seen that in this case, the V_{DS} value is not constant. It is changing during both the track and reset phases, and it is also different from the minimum signal clock cycle to the maximum signal clock cycle. However, if we compare values of each track phase to their corresponding values $T/2$ later in the reset phase, we see that they are approximately equal, as predicted above.

Summarizing, in (8), $(V_{\mathrm{GS}}-V_{\mathrm{TH}})$ is kept constant by the bootstrapping circuitry as described in the previous subsection, and V_{DS} is matched point by point from track to reset. Hence R_{ON} itself is matched point by point from track to reset. We call this concept *nonlinearity cancellation*. The reason can be seen from an examination of an RZ waveform, as shown for example in Fig. 4. If the rise and fall characteristics are nonlinear, then the error areas A and B will be individually nonlinear functions of the signal. In a conventional DAC, only A would be present, and this would show up as spectral harmonics. In the RZ circuit presented here, A and B are made equal and cancel out over the entire clock cycle, so they do not result in spectral harmonics in the baseband.

Nonlinearity cancellation is degraded with increasing resistive load and works best for fully capacitive loads as presented above. The reason is that the initial conditions, as well as the endpoints, of the transients are no longer matched for heavy resistive loads, and less benefit is therefore obtained from the nonlinearity cancellation feature. With resistive loading, in the track mode the initial condition is given by $V_{\mathrm{DS}} = V(R_{\mathrm{ON}}/R+R_{\mathrm{ON}})$, and the final condition is given by $V_{\mathrm{DS}} = V(R_{\mathrm{ON}}/R+R_L+R_{\mathrm{ON}})$, where R_L is the resistive load

(the capacitive case considered above is obtained by letting $R_L \to \infty$). In the reset mode, the initial condition is given by $V_{\rm DS} = V(R_{\rm ON}/R + R_{\rm ON})(R_L/R + R_L + R_{\rm SW})$, and the final condition is given by $V_{\rm DS} = 0$. The degradation is graceful because the change $\Delta V_{\rm DS} = V(R_{\rm ON}/R + R_{\rm ON})(R_L/R + R_L + R_{\rm SW})$ for both track and reset; in practice, simulation and measurement on the fabricated test circuit indicate that the performance is not significantly affected for $R_L \geq 4R$.[1]

D. Junction Capacitance Nonlinearities

The effects of junction capacitance nonlinearities become significant for higher resolution designs. Due to the RZ stage at the output of the DAC, we can ignore the junction capacitance associated with the DAC current sources, since these are designed to settle by midcycle. The concern here is with the junction capacitance associated with the devices in the output stage circuit, principally the NMOS switches. Electrostatic discharge devices at the output, if present, would also give rise to junction capacitance nonlinearity.

The junction capacitance behavior can be modeled by the well-known relationship

$$C_J = \frac{C_{J_0}}{\sqrt{1 + \dfrac{V_J}{\Psi_0}}} \tag{14}$$

where V_J is the junction voltage (the bulk is grounded) and the other symbols have their usual meanings. We now proceed to predict the effect of the nonlinear junction capacitance and derive a methodology to deal with it. To do so, we consider our track and reset half-circuits as R/C circuits but with a portion of the capacitive load, which behaves as the junction capacitance

$$C = C_L + \frac{C_{J_0}}{\sqrt{1 + \dfrac{V_{\rm OUT}}{\Psi_0}}} \tag{15}$$

where we now show that the junction voltage is the output voltage $V_{\rm OUT}$ of the DAC and the capacitance has a constant component given by the load capacitance C_L. We now analyze the effect of applying a current input $I_{\rm DAC}$ from the DAC to the R/C circuit with C as in (15). To do so, we first simplify (15) with a linear approximation

$$C = k_1 + k_2 V_{\rm OUT}. \tag{16}$$

The form of solution we obtain for this simplified case will allow us to also make deductions for higher order terms, but as with the threshold voltage, the linear term is the dominant source of nonlinearity for the values of $V_{\rm OUT}$ encountered in the RZ stage circuit. In (16), most of the constant capacitance k_1 is contributed by C_L, but a portion (C_{J_0}) is also due to the junction capacitance. Using (16), the current in the capacitor is given by $I_C = C(dV_{\rm OUT}/dt) + V_{\rm OUT}(dC/dt) = k_1(dV_{\rm OUT}/dt) + 2k_2 V_{\rm OUT}(dV_{\rm OUT}/dt)$. The output voltage is $V_{\rm OUT} = (I_{\rm DAC} - I_C)R$. Combining these two equations, we obtain

$$\frac{V_{\rm OUT}}{R} = I_{\rm DAC} - k_1 \frac{dV_{\rm OUT}}{dt} - 2k_2 V_{\rm OUT} \frac{dV_{\rm OUT}}{dt}. \tag{17}$$

This is a nonlinear differential equation in $V_{\rm OUT}$, and it is not possible to solve explicitly for $V_{\rm OUT}(t)$. However, we can obtain an inverse solution for $t(V_{\rm OUT})$, which is equally useful for our purposes, by separating the variables and integrating. In this way we obtain

$$t = -2k_2 R V_{\rm OUT} + (-k_1 R - 2k_2 I_{\rm DAC} R^2) \cdot \ln\left(1 - \frac{V}{I_{\rm DAC} R}\right) \tag{18}$$

where we see that we cannot invert to obtain an explicit expression for $V_{\rm OUT}(t)$[2] because of the transcendental nature of the expression on the right-hand side. However, we are interested in the error area formed during the transient rise. We can obtain this either by integrating $V_{\rm OUT}(t)$ from $t = 0$ to $t \to \infty$ and subtracting from the ideal $V_{\rm OUT}(t) = I_{\rm DAC} R$ value or directly by integrating $t(V_{\rm OUT})$ from $V_{\rm OUT} = 0$ to $V_{\rm OUT} = I_{\rm DAC} R$. Since we have $t(V_{\rm OUT})$ from (18), we proceed in the second way, to obtain a transient error of

$$\text{Error} = (I_{\rm DAC} R)(k_1 R) + (I_{\rm DAC} R)^2 (k_2 R). \tag{19}$$

This interesting result shows that the constant capacitance term k_1 gives rise to the linear error term $(I_{\rm DAC} R)(k_1 R)$, which is just the final value multiplied by the circuit time constant as in the linear solution, and the voltage-dependent capacitance term $k_2 V_{\rm OUT}$ gives the undesirable nonlinear error term of $(I_{\rm DAC} R)^2 (k_2 R)$. We deduce similar behavior with higher order terms in the final result if we had included higher order terms in (16). We also see that because of the independence of these terms, it is not possible to directly swamp out the voltage-dependent capacitance with the constant portion, but the effect of the voltage-dependent capacitance will be minimized if the nonlinear time constant $k_2 R \ll T/2$, the half-clock period. In practice, we design for $\tau = k_1 R \approx (T/2)/10$, as described in the previous section, and for $k_2 R \ll k_1 R$; this satisfies the $k_2 R \ll T/2$ condition. Numerical simulations of the system using the full nonlinear model of (15) to model the capacitance indicate that the theoretical differential SFDR is larger than 98 dBc if C_L: $C_{J_0} < 1$: 30, and this scaling was used in the output-stage circuit presented here.

E. Isolation and Current Sources

Isolation of the switching of the output stage from the current sources of the DAC is essential because this switching would otherwise disturb the settled position of the DAC. In such a case, the DAC would have to resettle during the track phase, which is undesirable because the DAC settling is in general nonlinear, as explained in the introduction. The circuitry responsible for this isolation is shown in Fig. 11.

There are two levels of isolation circuitry. A double cascode composed of devices M_2 and M_1 is present between the

[1] For the implementation here, this equates to $R_L \geq 100\ \Omega$ for the best possible performance. The technique can, however, be used for lower resistive loads by proportionately reducing the on-chip R (this necessitates proportionately larger DAC output currents and hence higher power consumption for the same output voltage swing).

[2] Note at this point that if we let $k_2 = 0$ in (18), we can invert to obtain the familiar linear solution $V_{\rm OUT} = I_{\rm DAC} R(1 - e^{-t/k_1 R})$, which is an exponential rise of the output voltage to the final value of $I_{\rm DAC} R$ as expected.

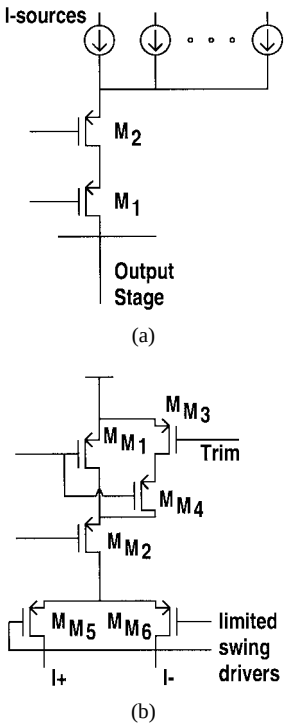


Fig. 11. Common isolation and current source circuitry.

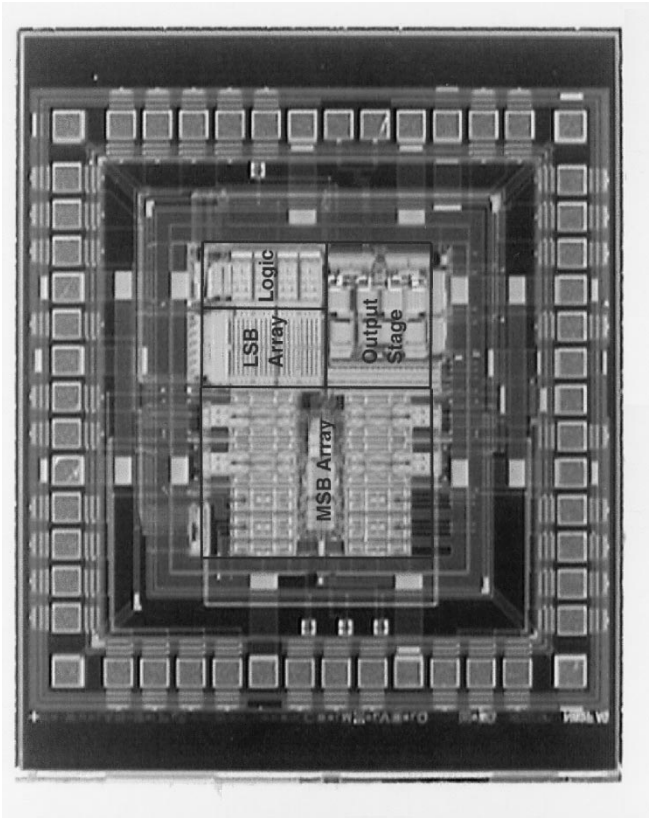


Fig. 12. Die photo.

output stage and the current sources, thus forming isolation circuitry common to the entire current source array, as shown in Fig. 11(a). The size of the M_2 and M_1 devices is set so as to ensure that their time constants do not impede settling of the DAC by midcycle; in addition, the size of M_2 is also large enough to result in a small swing ($\approx$ 200 mV) at its source node over the whole current output range of the DAC. This eases the requirement on the output resistance of the current sources to obtain 14-bit static linearity. A constant bias current, equal to half the DAC full-scale output current and independent of the input signal, is forced through the cascode devices at all times to ensure they do not turn off for low signal currents, which would degrade the operating speed. The 5-V power supply used is required to bias the PMOS current sources and cascode devices in the saturation region.

Fig. 11(b) is the current source schematic used for each of the MSB's. A limited swing driver (not shown) is used to drive the switches M_{M_5} and M_{M_6}, which operate in the saturated region. Thus a triple cascode, composed of the switches, cascode device M_{M_2}, and current source device M_{M_1}, is formed, and this both enhances the level of isolation from the output stage and guarantees the required static linearity.

Since the aim of this prototype chip was to attain high dynamic linearity, the matching of the current sources to 14-bit linearity is carried out by an external trim circuit. The trim voltage controls the branch of the MSB current flowing through M_{M_4} and M_{M_3} by modulating the on-resistance of the linear mode device M_{M_3}. In full versions of this DAC, the trim voltage will be supplied by an on-board calibration circuit. The off-chip calibration scheme consists of a network of 15 voltage references and potentiometers to set the 15 MSB trim voltages. The stability of the circuit is limited by the temperature coefficients of these components, implying that after initial calibration, the trim voltages eventually drift away from the calibrated position over time, necessitating recalibration. For dynamic linearity testing purposes, the arrangement is satisfactory, as described further in Section IV.

F. Differential Implementation

The output circuit is implemented differentially to take advantage of the differential outputs of the current DAC driving it. This cancels out the even-order nonlinearities, including the second-order nonlinearity introduced by the on-chip resistors R_{1+}, R_{1-} and R_{2+}, R_{2-} (single-ended testing on the fabricated chip shows that this nonlinearity is significant above the 12-bit level). A higher degree of differential symmetry can be built into the output stage than can be done for conventional DAC's. This is because the switching characteristics have been reduced to the four switches of the differential RZ circuit. In a conventional DAC, the differential performance is dependent upon the timing of the signals fed to the differential switches of all the current sources; it is not possible to synchronize these as well as is possible in the case of the four RZ switches. For the conventional DAC, the crossing point of the differential signals is significant, and for different current sources, this point is affected by skew considerations, mismatch at various points on the die, and process drift. Using the output stage reduces the differential matching problem to a case of matching two track signals and two reset signals, and it is possible to do this with greater accuracy.

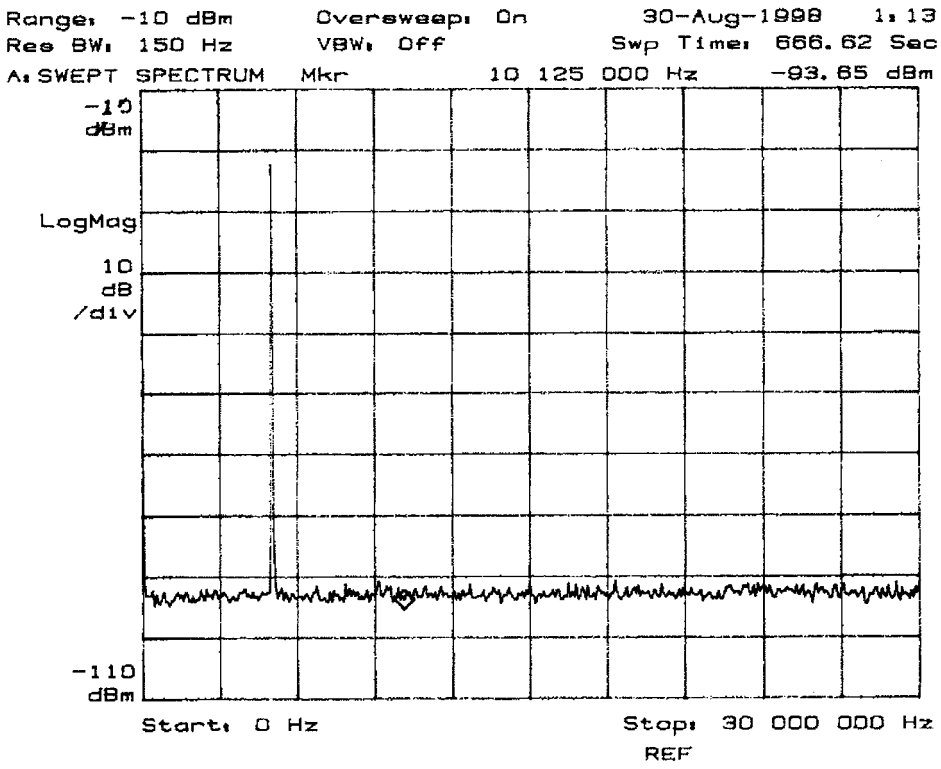


Fig. 13. Low-frequency spectrum.

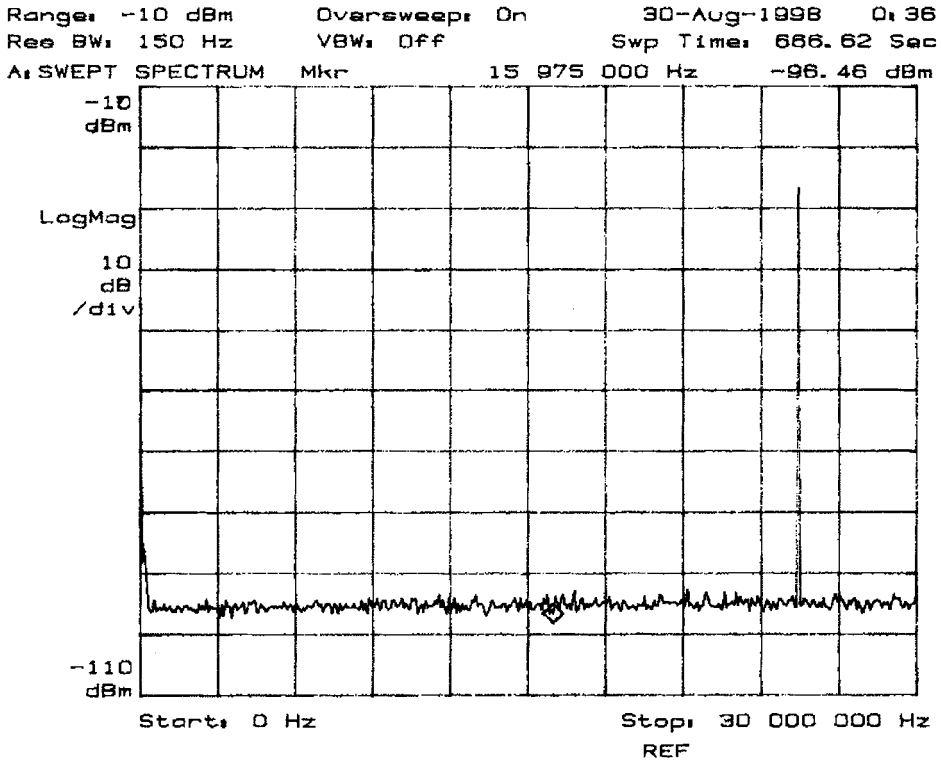


Fig. 14. High-frequency spectrum.

IV. Measurement Results

Fig. 12 shows a die photo of the fabricated chip. The die occupies an area of 3.69×3.91 mm^2 in a 0.8-μm CMOS process. The output stage is in the lower right quarter of the die, occupying approximately 25% of the active area; the rest of the area is taken up by the DAC and associated biasing circuitry. A 0.8-μm process was selected for this chip because of the limitations imposed on the oxide thickness by the

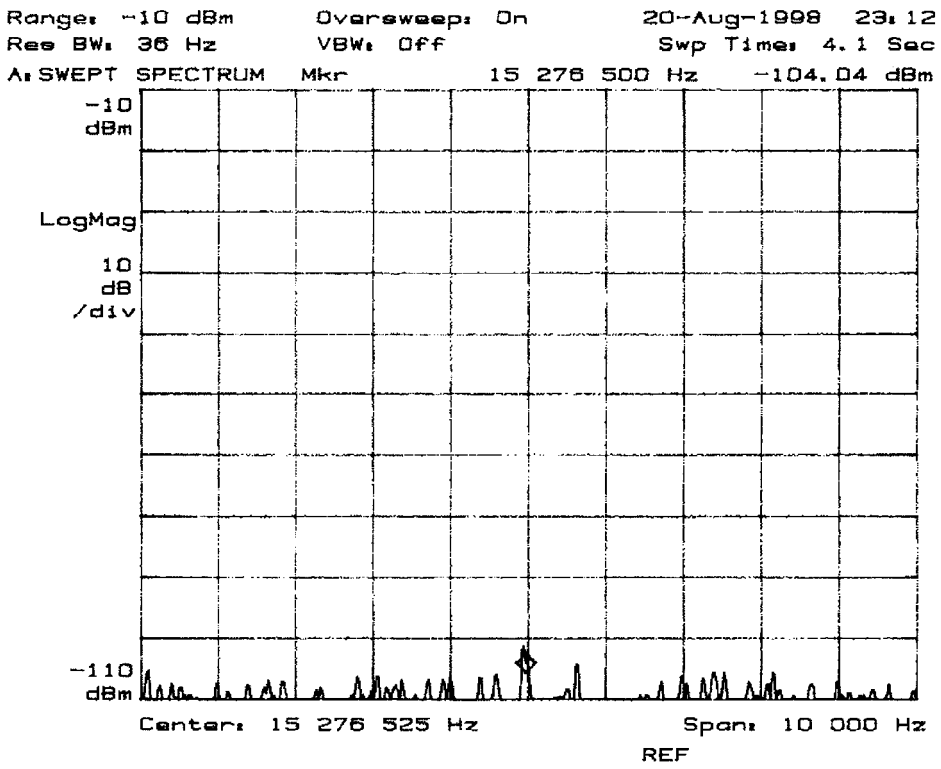


Fig. 15. Low-frequency spectrum—largest spur.

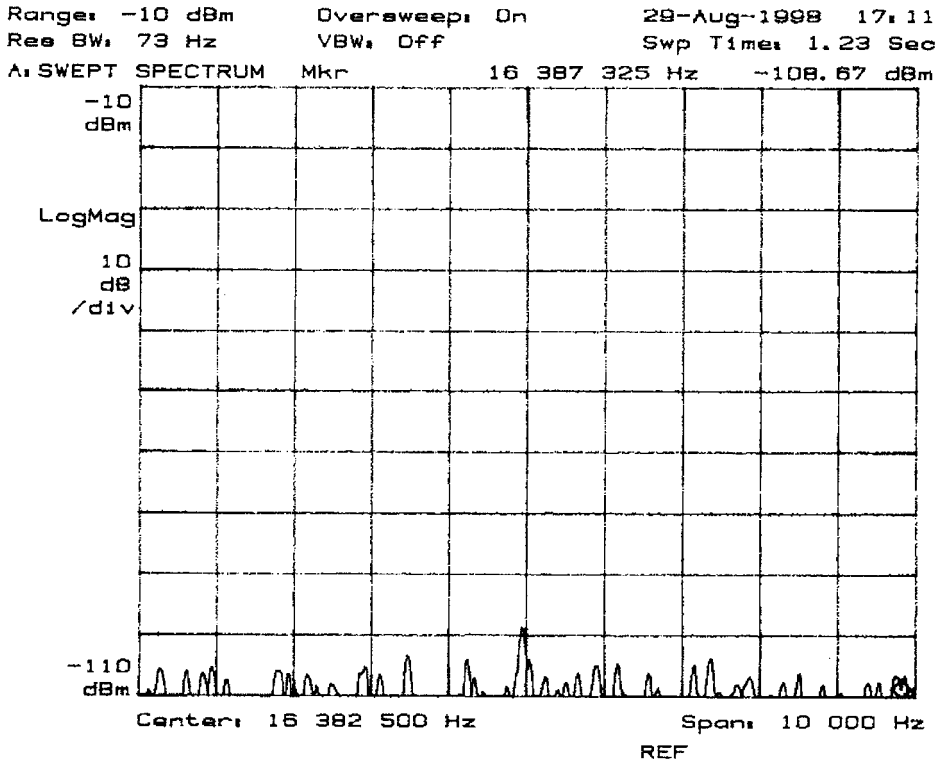


Fig. 16. High-frequency spectrum—largest spur.

bootstrapping, but modern 0.5-μm processes would also meet this requirement, and would result in improved performance due to the lower switch R_{ON}.

Figs. 13 and 14 show the output of the DAC when synthesizing sinewaves at low (5.1 MHz) and high (25.5 MHz) positions in the Nyquist baseband, respectively. The results shown are for a 60-MS/s clock (30-MHz Nyquist baseband) and are obtained when the outputs are combined differentially by means of a transformer. The output network consists of R/C loads on the primary side of the transformer at the chip outputs

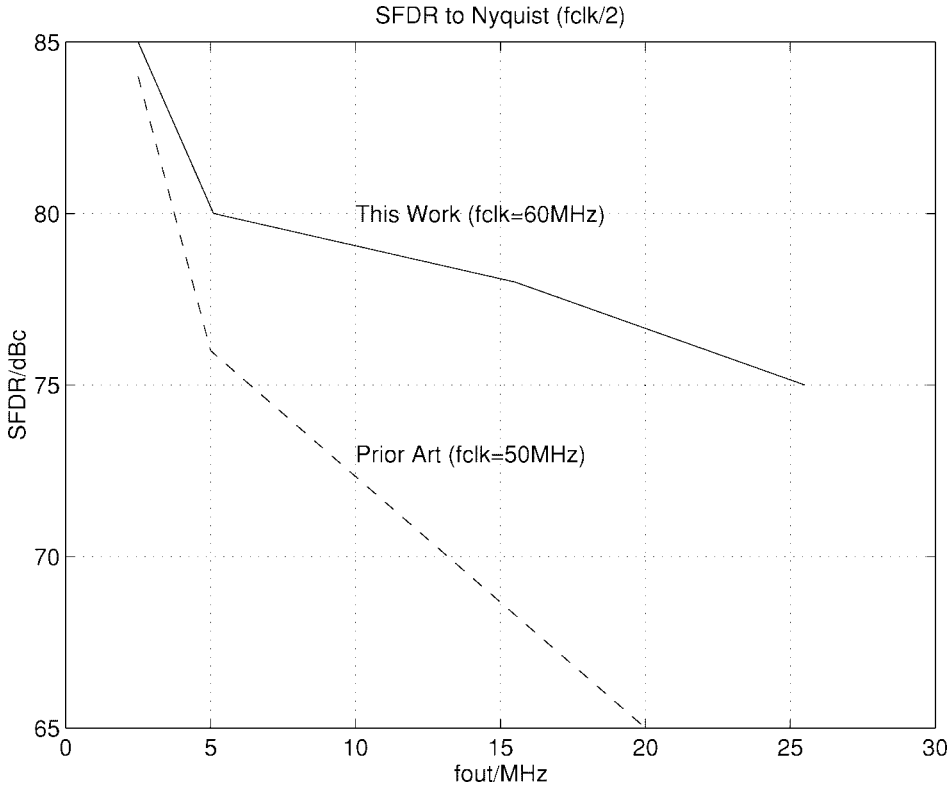


Fig. 17. Comparison with prior art.

driving a high impedance probe on the spectrum analyzer on the secondary side (hence the power level of the fundamental in Figs. 13 and 14). In both plots, the harmonics are below the noise floor introduced by the spectrum analyzer and test setup, so closeup plots of the largest spurs are provided with lower noise floors in Figs. 15 and 16. (The entire Nyquist baseband was analyzed in sections between recalibration sequences to account for all possible harmonic/nonharmonic spurs. The uncalibrated static linearity of the DAC was measured from INL and DNL plots before calibration to be at the 10-bit level, as was designed for.) From this, we see that at 60 MS/s, DAC SFDR is 80 dB for 5.1-MHz input signals and is down only to 75 dB for 25.5-MHz input signals. We expect the output SFDR to remain relatively constant across the baseband because in the RZ output stage, both low- and high-frequency input signals are synthesized as high-frequency outputs.

Single-ended testing at the loads available in the output test circuit on the primary side was also carried out; the results of this showed that for higher frequencies in the baseband the SFDR is somewhat degraded as compared to the differential case. In particular, at 60-MS/s clock, single-ended DAC SFDR is 77 dB for 5.1-MHz input signals and is down to 64 dB for 25.5-MHz inputs. These figures indicate the relative benefits obtained from the closely matched differential implementation of the output stage.

For higher clock rates, the SFDR performance of the chip was also seen to degrade. Although the chip was functional to above 100-MS/s clock rates, the SFDR at 8-MHz input signal at these clock rates is down to the levels observed almost at the Nyquist rate with the 60-MS/s clock, as can be seen from the results summarized in Table I. Partly, this is because the dynamic nonlinearities of the DAC output occupy a greater proportion of the clock cycle at higher clock rates. Limitations of the test circuit also contributed to this figure, however, particularly coupling from the digital inputs to the DAC analog outputs on the testing board.

TABLE I
CHIP SUMMARY

Resolution	14 bits
INL (after calibration)	$< \pm$ 0.5 LSB
DNL (after calibration)	$< \pm$ 0.5 LSB
Update Rate	100MS/s
Full-Scale Output Current	20mA
Full-scale Output Swing	1Vpp txfrmr-coupled
SFDR (f_{clk}=10.0MS/s, f_{in}=0.8MHz)	85 dBc
SFDR (f_{clk}=30.0MS/s, f_{in}=2.5MHz)	82 dBc
SFDR (f_{clk}=60.0MS/s, f_{in}=5.1MHz)	80 dBc
SFDR (f_{clk}=60.0MS/s, f_{in}=25.5MHz)	75 dBc
SFDR (f_{clk}=100.0MS/s, f_{in}=8.5MHz)	74 dBc
Two-Tone SFDR (f_{clk}=60.0MS/s, f_{in_1}=25.5 MHz, f_{in_2}=25.6MHz)	75 dBc, (>80dBc, IM_3)
Max. Power (5V supply, f_{clk}=100MS/s)	750mW
Die Area (in 0.8μm CMOS)	3.69mm x 3.91mm

The power consumption, 750 mW at 100 MS/s, is relatively high for a 20-mA/5-V current-mode DAC for a number of reasons. Approximately half the power is consumed in the biasing network of the DAC current sources to ensure that the current sources settle within half a clock cycle, hence deriving the maximum possible benefit from the track/reset output stage. Furthermore, the buffers driving the

bootstrapped switches consume approximately 200 mW of power to obtain the required performance when tracking the switch source voltages. After accounting for the 100 mW consumed by the DAC output currents and a further 50 mW due to constant current forced through the isolation cascode devices, the residual power is mainly that consumed in the digital circuitry, composed of the thermometer decoding for the MSB's and ULSB's and the associated latches and buffers.

Fig. 17 compares the SFDR of the DAC presented here to the best reported at the time of publication [20]. It can be seen that although the static (low frequency) performance of the two DAC's is similar, at higher frequencies, the advantages of the RZ DAC for dynamic linearity become clear.

V. Conclusions

A high-speed and high-resolution DAC designed for spectral performance (dynamic linearity) has been presented. The key features of this DAC include a differentially implemented linear return-to-zero output stage, which tracks the DAC output at midcycle to avoid switching transients and then resets it to ground, a fast settling current-mode DAC, and isolation of the two circuits from each other to preserve the settled position of the DAC when the track phase begins. The features of the RZ stage that lead to the dynamic linearity performance have been explained.

Acknowledgment

The authors thank M. Miller for his help with testing.

References

[1] D. Mercer and L. Singer, "12 bit 125 MS/s CMOS D/A designed for spectral performance," in *Proc. Int. Symp. Low Power Electronics and Design*, 1996, pp. 243–246.
[2] I. Jorgensen and S. Tunheim, "A 10 bit 100 MS/s BiCMOS D/A converter," *Analog Integrated Circuits Signal Process.*, pp. 15–28, Dec. 1997.
[3] D. Mercer, "A 16 bit D/A converter with increased spurious free dynamic range," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1180–1185, Oct. 1994.
[4] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12 bit intrinsic accuracy high speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1959–1969, Dec. 1998.
[5] C. Lin and K. Bult, "A 10 bit 500 MS/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1948–1958, Dec. 1998.
[6] B. Tesch and J. Garcia, "A low glitch 14 bit 100 MHz D/A converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1465–1469, Sept. 1997.
[7] J. Vandenbussche, G. Van der Plas, A. Van den Bosch, W. Daems, G. Gielen, M. S. J. Steyaert, and W. Sansen, "A 14b 150 MSample/s update rate Q^2 random walk CMOS DAC," in *ISSCC Dig. Tech. Papers*, 1999, pp. 146–147.
[8] R. Hester, S. Mukherjee, D. Padgett, D. Richardson, W. Bright, M. Sarraj, M. Agah, A. Bellaouai, I. Chaudry, J. Hellums, K. Islam, A. Loloee, J. Nabicht, F. Tsay, and G. Westphal, "CODEC for echo-canceling, full-rate ADSL modems," in *ISSCC Dig. Tech. Papers*, 1999, pp. 242–243.
[9] D. W. J. Groeneveld, H. J. Schouwenaars, H. A. H. Termeer, and C. A. A. Bastiaansen, "A self-calibration technique for monolithic high-resolution D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1517–1522, Dec. 1989.
[10] M. Moyal, M. Groepl, and T. Blon, "A 25 kft 768 kb/s CMOS transceiver for multiple bit-rate DSL," in *ISCC Dig. Tech. Papers*, 1999, pp. 244–2456.
[11] P. Hendriks, "Specifying communications DAC's," *IEEE Spectrum*, vol. 34, pp. 58–69, July 1997.
[12] T. Miki, Y. Nakamura, K. Okada, and Y. Horiba, "Transient analysis of switched current source," *IEICE Trans. Electron.*, vol. E75-C, pp. 288–296, Mar. 1992.
[13] M. Pelgrom, A. Duinmaijer, and A. Webers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.
[14] M. S. J. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, "Custom analog low power design: The problem of low voltage and mismatch," in *Proc. IEEE Custom Integrated Circuit Conf.*, 1997, pp. 285–292.
[15] K. Khanoyan, F. Behbahani, and A. Abidi, "A 10b, 400 MS/s glitch-free CMOS D/A converter," in *1999 Symp. VLSI Circuits Dig. Tech. Papers*, paper 8-1.
[16] P. Vorenkamp and J. Verdaasdonk, "Fully bipolar 120 MS/s 10 bit track and hold circuit," *IEEE J. Solid-State Circuits*, vol. 27, pp. 988–992, July 1992.
[17] P. Vorenkamp and R. Roovers, "A 12 bit 60 MS/s cascaded folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1876–1886, Dec. 1997.
[18] P. Lim and B. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE J. Solid-State Circuits*, vol. 26, pp. 643–651, Apr. 1991.
[19] T. Lin and H. Samueli, "A 200-MHz CMOS $x/\sin(x)$ digital filter for compensating D/A converter frequency response distortion," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1278–1285, Sept. 1991.
[20] "14-bit, 100MSPS+ TxDAC D/A converter," Datasheet, Analog Devices, Inc., Wilmington, MA, 1998.

Alex R. Bugeja (M'97) was born in Malta in 1973. He received the B.Eng. (Hons.) degree in electrical engineering from the University of Malta in 1994 and the M.S. degree in engineering sciences from Harvard University, Cambridge, MA, in 1996. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Illinois at Urbana-Champaign.

Since 1998, he has been a Design Engineer in the Data Converter Products group with Texas Instruments, Dallas, TX. His research interests include high-speed and resolution data converters and mixed-signal circuit and system design.

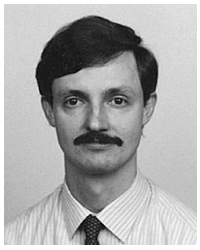
Bang-Sup Song (S'79–M'83–SM'88–F'99) received the B.S. degree from Seoul National University, Seoul, Korea, in 1973, the M.S. degree from the Korea Advanced Institute of Science in 1975, and the Ph.D. degree from the University of California, Berkeley, in 1983.

From 1975 to 1978, he was a Research Staff Member with the Agency for Defense Development, Korea, working on fire-control radars and spread-spectrum communications. From 1983 to 1986, he was a Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, NJ, and was also an Adjunct Professor in the Department of Electrical Engineering, Rutgers—The State University, Piscataway, NJ. From 1986 to 1999, he was a Professor in the Department of Electrical and Computer Engineering, University of Illinois, Urbana. He currently holds the Powell Endowed Chair in Wireless Communication in the Department of Electrical and Computer Engineering, University of California, San Diego.

Dr. Song received a Distinguished Technical Staff Award from AT&T Bell Laboratories in 1986, a Career Development Professor Award from Analog Devices in 1987, and a Xerox Senior Faculty Research Award in 1995. His IEEE activities have been in the capacities of an Associate Editor, a Guest Editor, and a Program Committee Member for IEEE Transactions on Circuits and Systems, IEEE Journal of Solid-State Circuits, IEEE International Solid-State Circuits Conference, and IEEE Symposium on Circuits And Systems.

Patrick L. Rakers (M'86) received the B.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 1984 and the M.S. degree in electrical engineering from the Illinois Institute of Technology, Chicago, in 1989.

Since joining Motorola Corp., Schaumburg, IL, in 1984, he has been involved in the research and design of mixed-signal integrated circuits with emphasis on data conversion. He is currently a Corporate Member of Technical Staff in the Communication Systems and Technology Research Labs of Motorola Labs. He has received seven patents and is an author of seven IEEE publications.



Steven F. Gillig (M'95) received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 1974 and 1976, respectively, and the M.B.A. degree from the University of Chicago, Chicago, IL, in 1990.

Since joining Motorola Corp., Schaumburg, IL, in 1976, he has been involved in the research and design of several generations of IC's for wireless communication equipment, beginning with the world's first production portable cellphone. He has received 24 patents. He is currently Manager of Integrated Circuit Research in the Communication Systems and Technologies Labs of Motorola Labs.