ECE594A
Winter 2005
Mixed Signal Electronics

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Course Outline

1. Technology Overview
   A. Materials
   B. MOSFET Scaling trends
   C. Implications of CMOS scaling to mixed signal IC design
   D. SiGe BiCMOS

Course Outline

2. Data conversion circuits
   A. Track/Hold circuits
   B. D/A converters
   C. A/D converters

Course Outline

3. Data transmission circuits

   A. Clock generation and recovery

   B. Frequency generation

      PLL, DLLs

   C. Phase noise and jitter

   D. Serial data transmission circuits (SERDES)

Course Outline

Now, it's your turn. Two options:

1. Review and present journal paper(s)
    1. Topic of your choice – must be approved
    2. 20 minute presentation
    3. Facilitate discussion in class
    4. Paper must be available at least 2 days ahead of time.

Course Outline

2. Design project on data conversion or transmission circuit
    1. 0.18 um public domain CMOS
    2. (or your favorite technology – you provide model parameters)
    3. Submit a proposal
    4. No layouts
    5. ADS, MATLAB, HSPICE available.
    6. 20 minute presentation required

Course grading

- Case 1:
  - Paper presentation 40%
  - Midterm 40%
  - Homework 20%
- Case 2:
  - Design Project 50%
  - Midterm 35%
  - Homework 15%

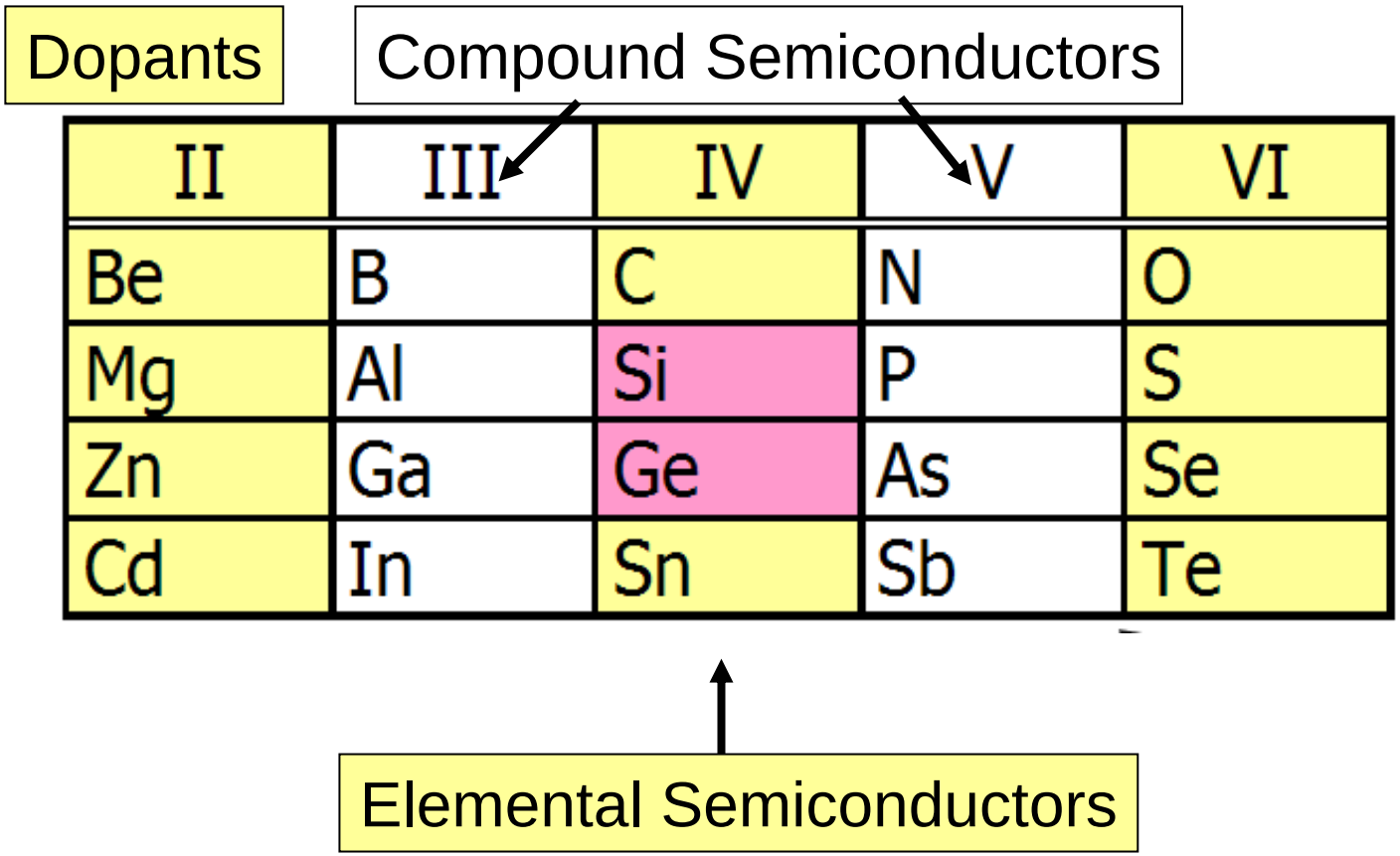
Lecture 1

- High Speed IC Technology Comparisons
  - Materials
  - Devices
  - Scaling trends
  - Performance trends

Compare Materials

- Semiconductor transport properties:
  - compare Si, SiGe, and III-Vs
- Heterojunctions
- Substrates

Elements



S. Long, Compound Semiconductor IC Symposium 2004 Primer Course

Substrate material properties

Material	Thermal conductivity	Dielectric constant	Wafer size	Electrical conductivity	Cost
Silicon	1.45 W/cm-K	11.7	300mm	n or p	Low
GaAs	0.45	13.1	100-150	n, p, or semi-ins.	Mediu
InP	0.68	12.4	50-100	N, p, or semi-ins.	High
Sapphire	0.42	9.4	200	Insulating	Low
SiC	3.0 – 3.8	9.8	50-75	N, p, or semi-ins.	VERY high

S. Long, Compound Semiconductor IC Symposium 2004 Primer Course

Elemental Semiconductor: Si

- Workhorse of the industry
  - Great substrates, oxide, metallization systems
  - Excellent density of devices, interconnect
  - High thermal conductivity
- Limited in transport properties
  - $Ve_{sat} \cong 1 \times 10^7$ @ 10^5 V/cm
    - Limits f_T of device

    $\mu_e \cong 1400$ cm^2/V-s $\mu_h \cong 300$ cm^2/V-s
    - Increases access resistances
    - Strained layers improve however

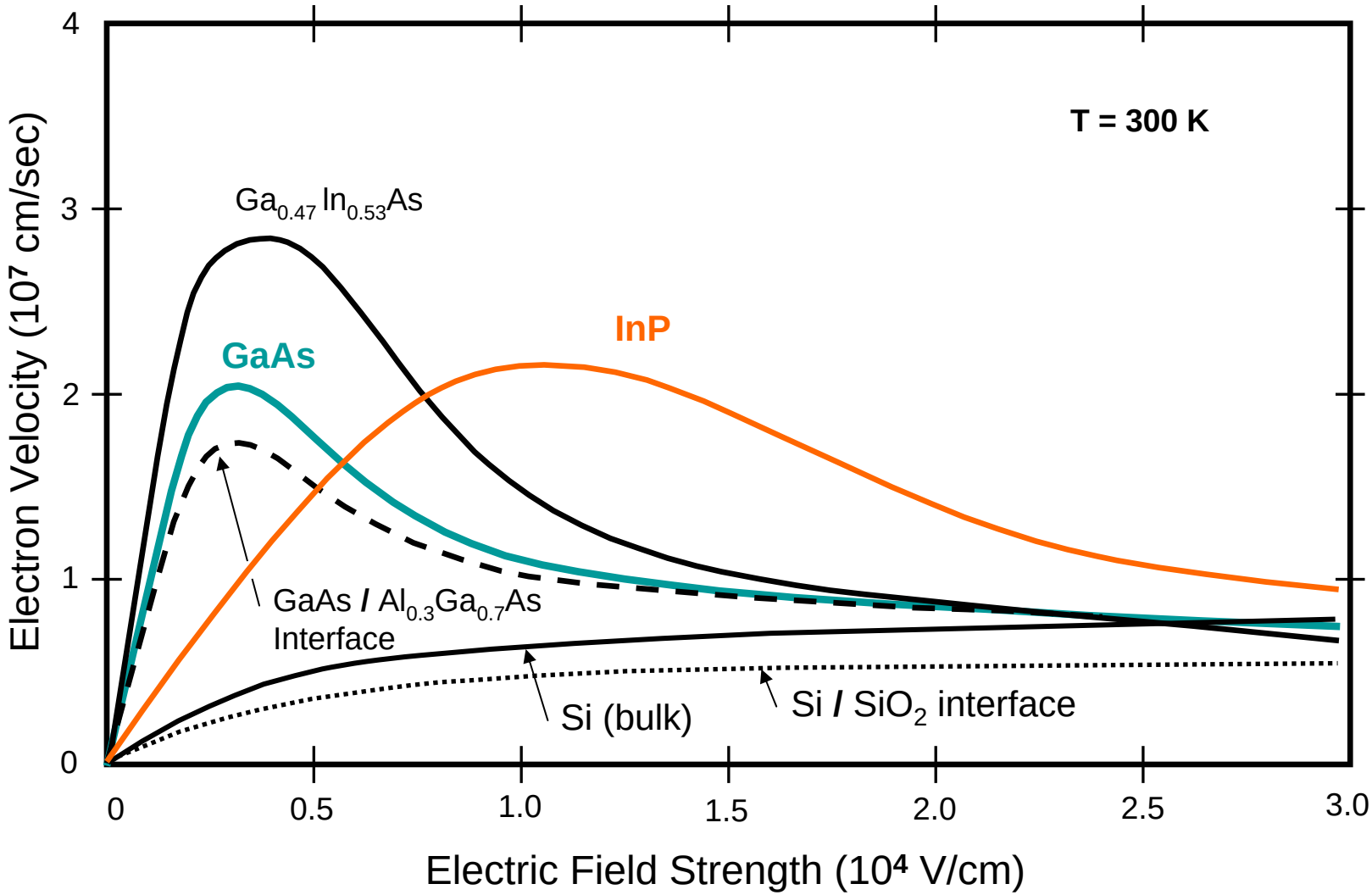
Improving Si: SiGe

- Overcoming transport limitations
  - Extremely short gate lengths < 60 nm
    - f_T > 150 GHz f_{max} > 200 GHz (SOI)
    - Strained Si channel increases mobility
  - Narrow base widths + doping gradients
    - Transport improves but access resistance (R_{bb}) degrades
  - Silicon-Germanium base
    - Graded bandgap – quasi-electric field: reduces τ_b
    - Higher hole mobility helps reduce R_{bb}
    - Retains most of processing advantages of Si

Why III – Vs?

- Transport: high electron velocities
  - $In_{0.47}Ga_{0.53}As$: $v_{sat} \cong 2.7 \times 10^7$ cm/s
  - Reduces transit time, increases f_T
- Optoelectronic properties
  - Many direct bandgap compounds available
  - Lasers, LEDs
- Heterojunctions
  - Allow bandgap engineering!

Electron Velocity versus Electric Field Strength for Various Semiconductors



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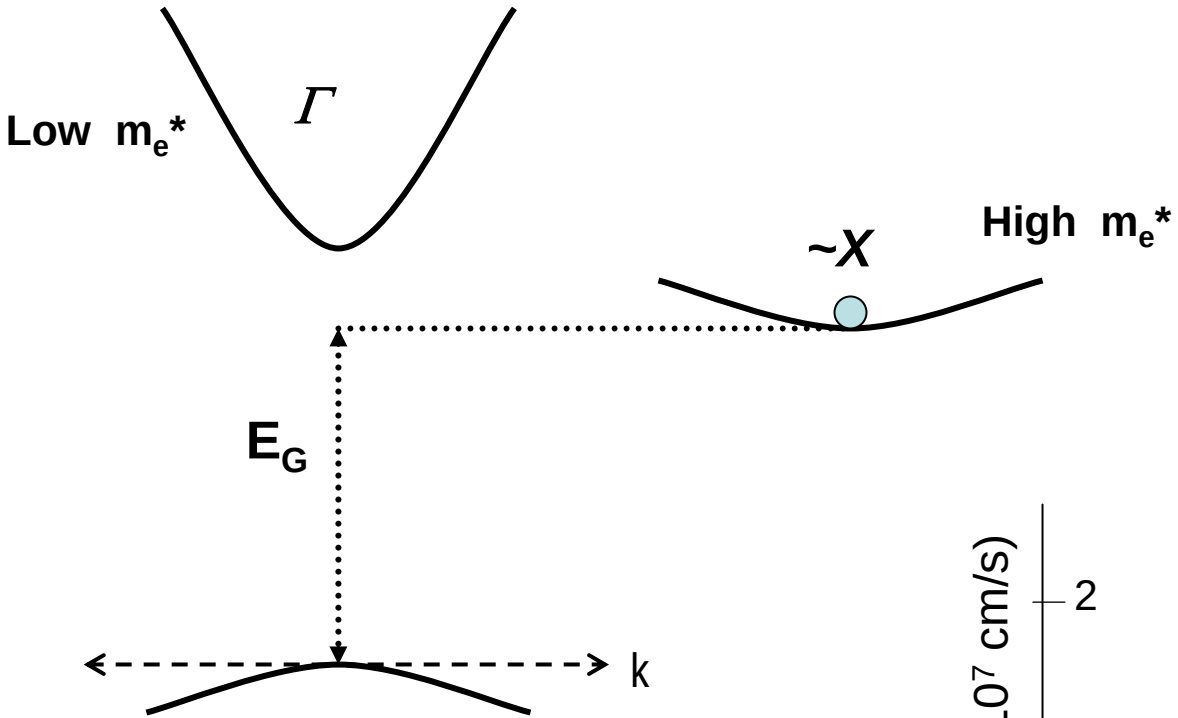
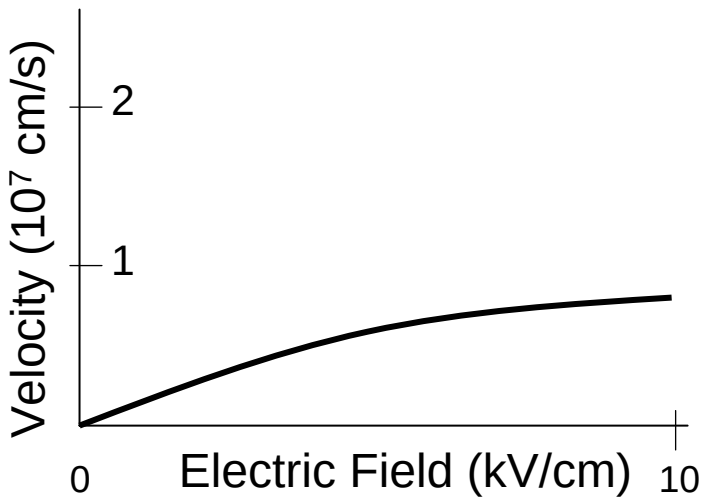
Recall Bandstructure of Si/SiGe in k-space



B. Brar, Rockwell Scientific



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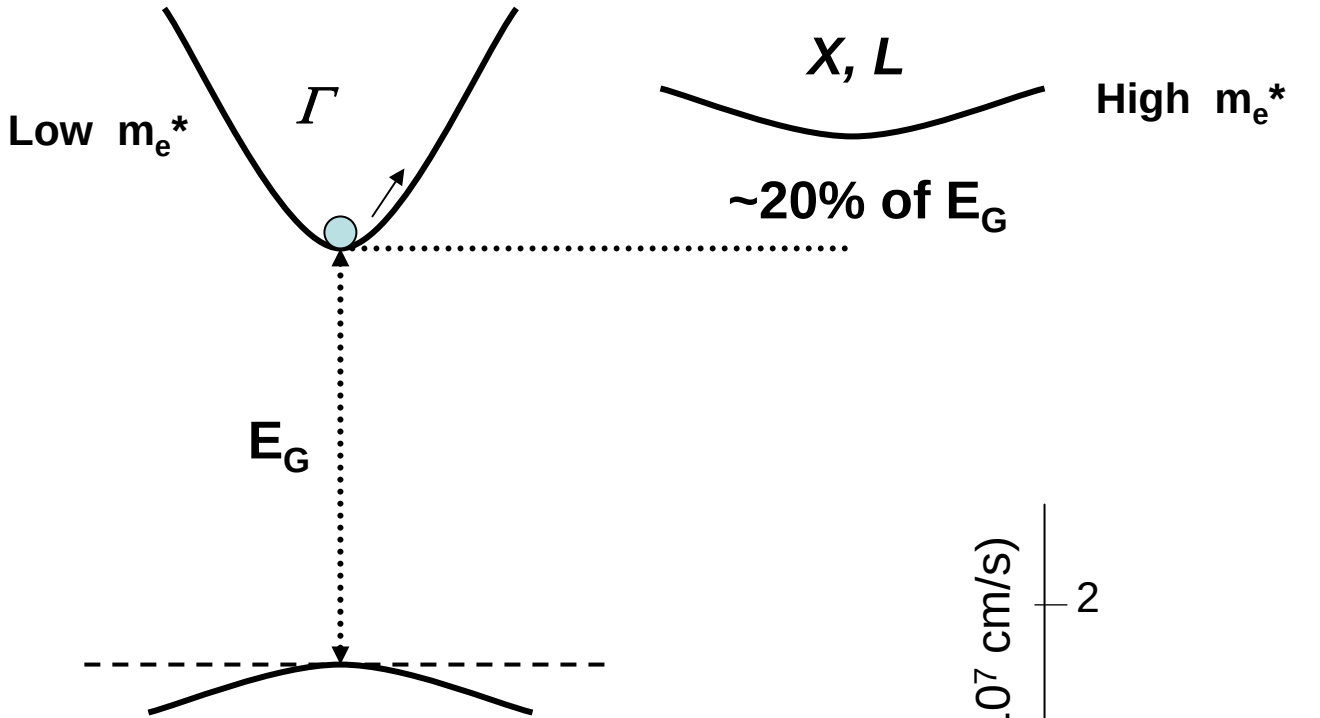
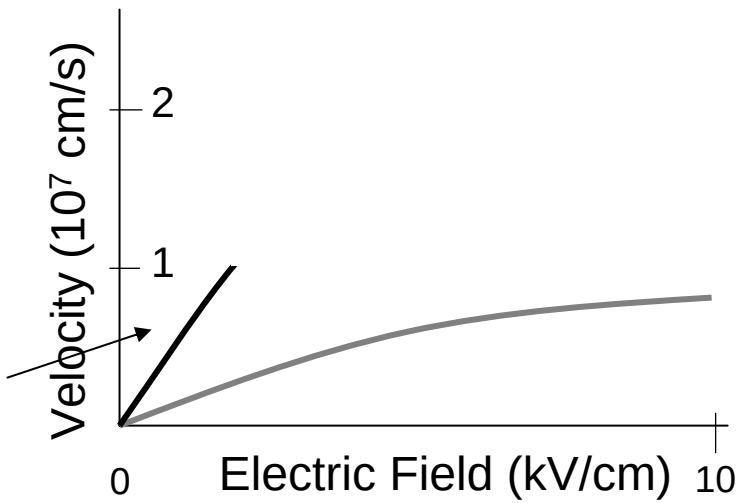
Bandstructure of GaAs



Low m_e^* of Γ valley => high mobility ($v = \mu E$)

B. Brar, Rockwell Scientific



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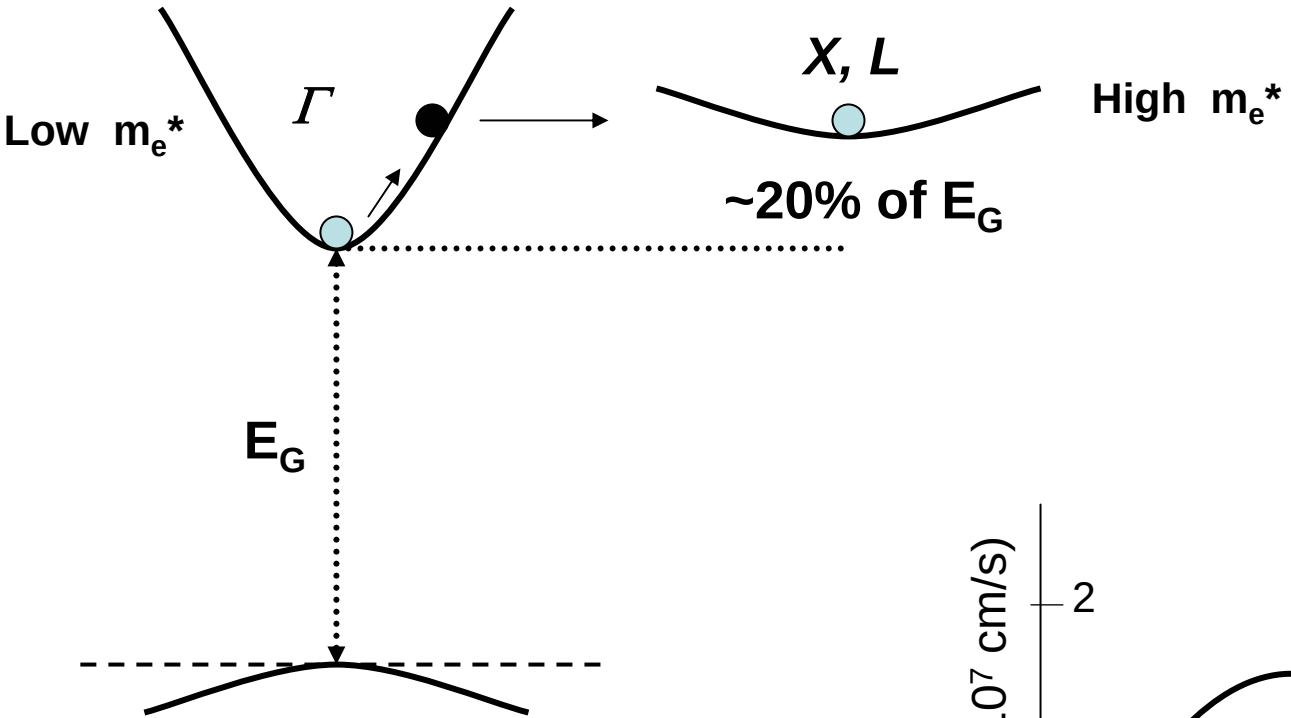
Bandstructure of GaAs



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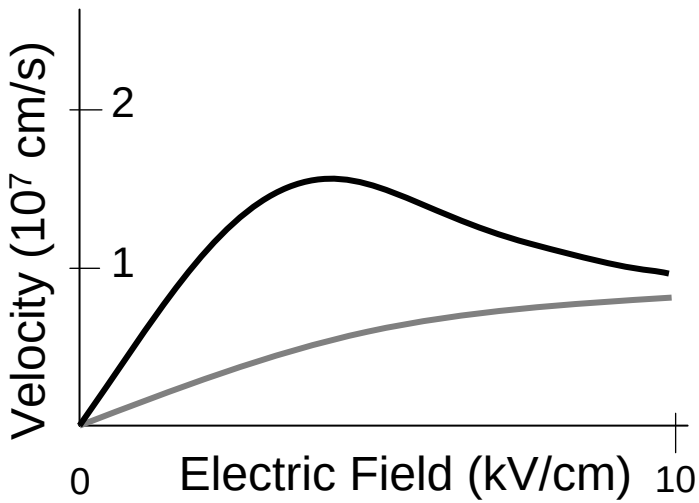

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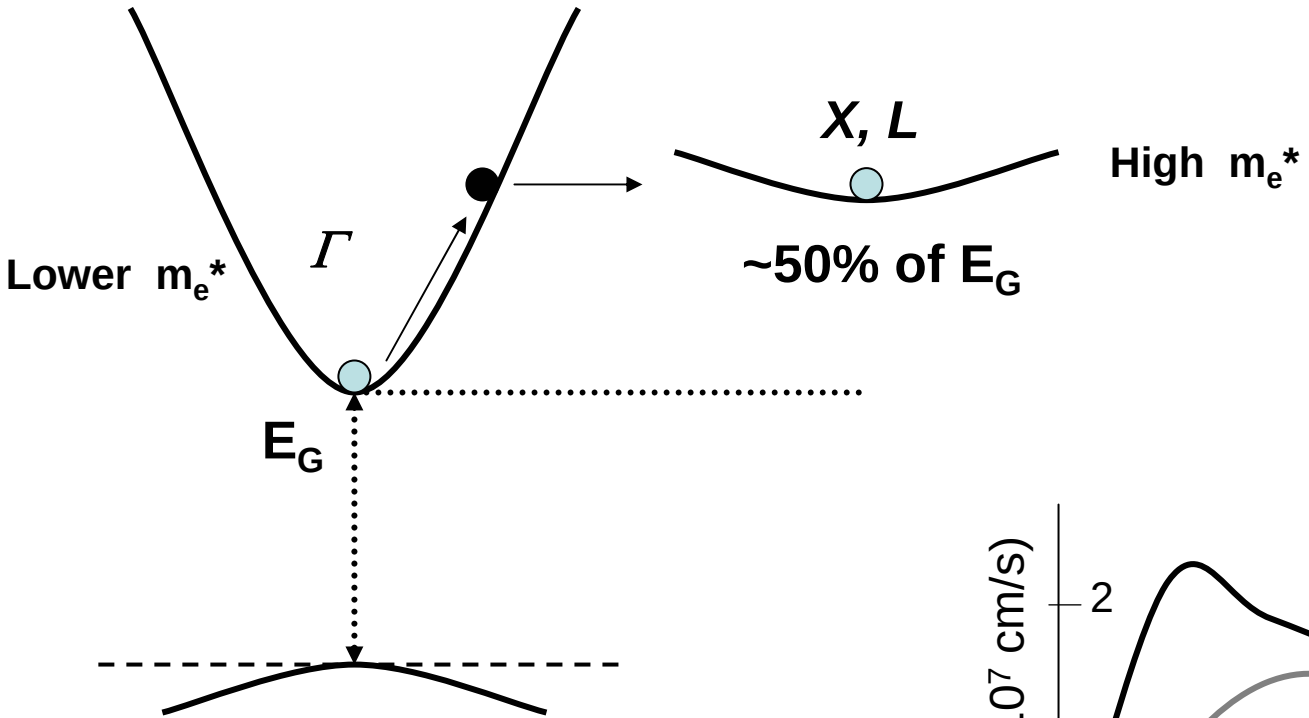
Bandstructure of GaInAs (base & SHBT collector)



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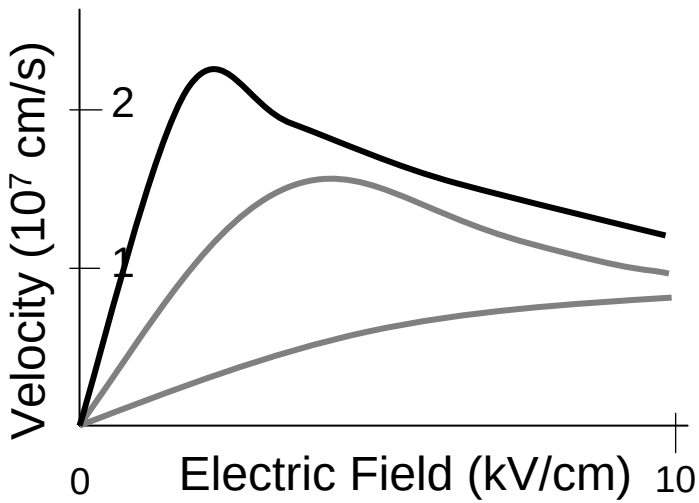

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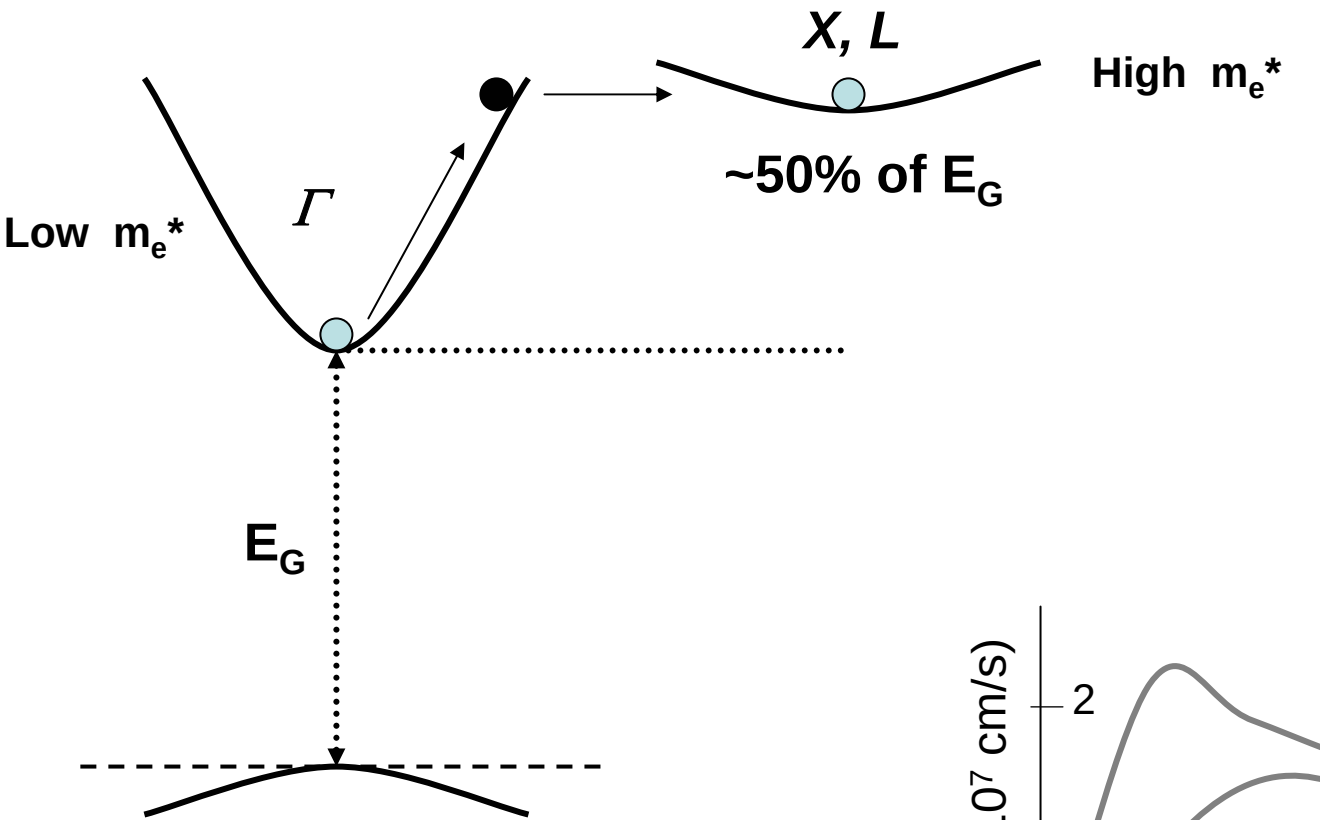
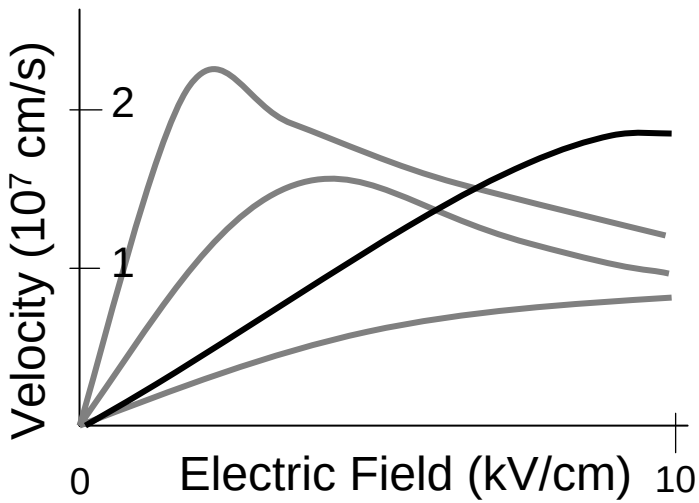
Bandstructure of InP for DHBTs





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Semiconductor Material Parameters

(T = 300 K and "weak doping" limit)

Semiconductor	E_G (eV)	ε_r	Electron Mobility (cm^2/V-sec)	Hole Mobility (cm^2/V-sec)	Peak Electron Velocity (cm/sec)
Si (bulk)	1.12	11.7	1,450	450	N.A.
Ge	0.66	15.8	3,900	1,900	N.A.
InP	1.35 D	12.4	4,600	150	2.1×10^7
GaAs	1.42 D	13.1	8,500	400	2×10^7
$Ga_{0.47}In_{0.53}As$	0.78 D	13.9	11,000	200	2.7×10^7
InAs	0.35 D	14.6	22,600	460	4×10^7
$Al_{0.3}Ga_{0.7}As$	1.80 D	12.2	1,000	100	---
AlAs	2.17	10.1	280	---	---
$Al_{0.48}In_{0.52}As$	1.92 D	12.3	800	100	---

(In bandgap energy column the symbol "D" indicates direct bandgap, otherwise, it is indirect bandgap)

GaN	**3.34D**	**9.5**	**1200**	**150**	**3 x 10^7**

P type

Ref. 1.14, 1.15

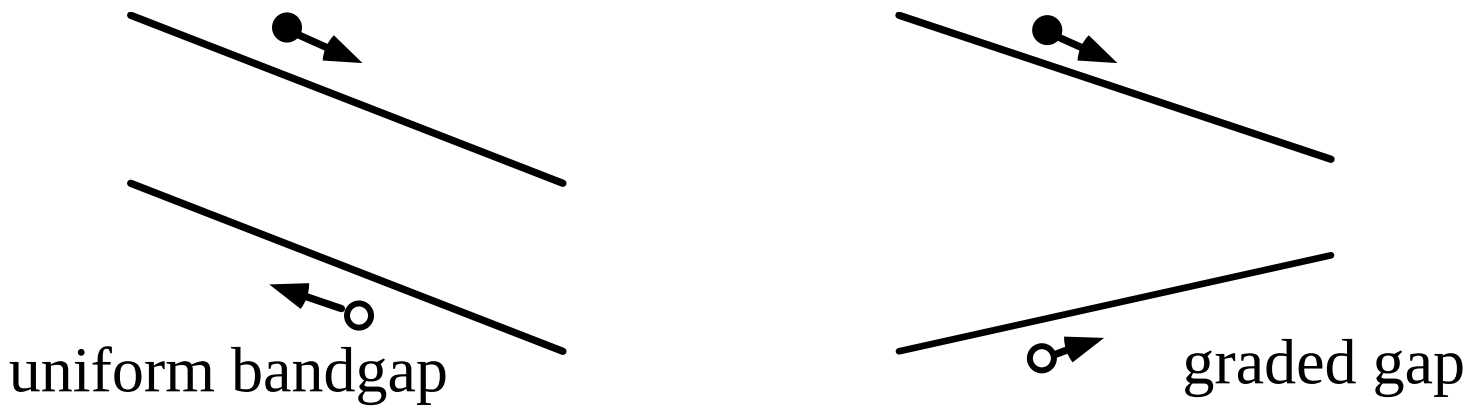
S. Long, GaAs IC Symposium 2002 Primer Course

Heterojunctions

Widely used in III-V's to enhance performance

The Central Design Principle for Heterostructures [1]

" Heterostructures use energy gap variations in addition to electric fields as forces acting on holes and electrons to control their distribution and flow."



[1] H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits," Proc. IEEE 70 (1) pp. 13-25, 1982.

S. Long, Compound Semiconductor IC Symposium 2004 Primer Course

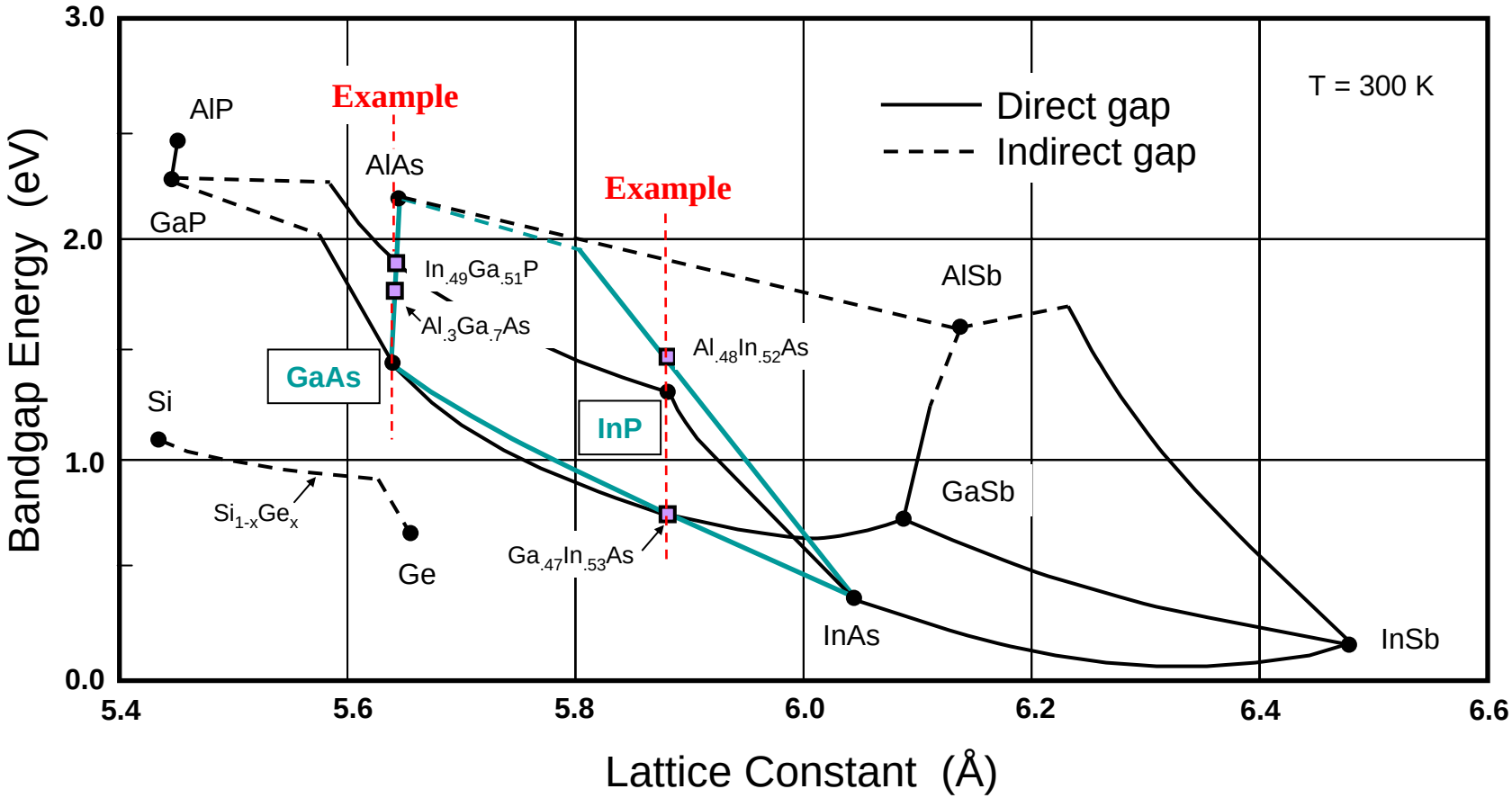
Heterojunctions

- Provide:
  - Carrier Confinement
    - quantum wells
    - 2D electron and hole gas structures
  - Bandgap grading
    - Quasi-electric fields reduce transit times
  - Optical Confinement
    - index grading
    - stepped index

Heterojunctions

- Technology
  - Growth
    - MBE or MOCVD
  - Lattice Matching
    - limits possible combinations of materials
    - BUT: elastic strain (pseudomorphic) can be tolerated
    - lattice mismatch x thickness = constant

Bandgap Energy vs. Lattice Constant



From S. Long, D. Estreich, C. Chang, M. Venkataraman, "Compound Semiconductor Digital IC Technology," Chap. 69, in VLSI Handbook, CRC Press, 2000.

So, what's the downside?

- Poor thermal conductivity compared with Si
- Low ρ contacts are more difficult
- Process technology is comparatively primitive
  - Substrate size
  - Low device and interconnect density
- Transit time is only one part of the problem
  - Digital: RC time constants generally dominate
  - Analog: f_{max} is usually more important than f_T

Compare InP and SiGe HBTs

Parameter	InP/InGaAs	Si/SiGe	benefit (simplified)
collector electron velocity	3E7 cm/s	1E7 cm/s	lower τ_c , *higher J*
base electron diffusivity	40 cm^2/s	~2-4 cm^2/s	lower τ_b
base sheet resistivity	500 Ohm	5000 Ohm	lower R_{bb}
comparable breakdown fields			

Consequences, if comparable scaling & parasitic reduction:

~3:1 higher bandwidth at a given scaling generation

~3:1 higher breakdown at a given bandwidth

Problem for InP: SiGe has much better scaling & parasitic reduction

Technology comparison today:

Production SiGe and InP have comparable speed

SiGe has much higher density and integration scale

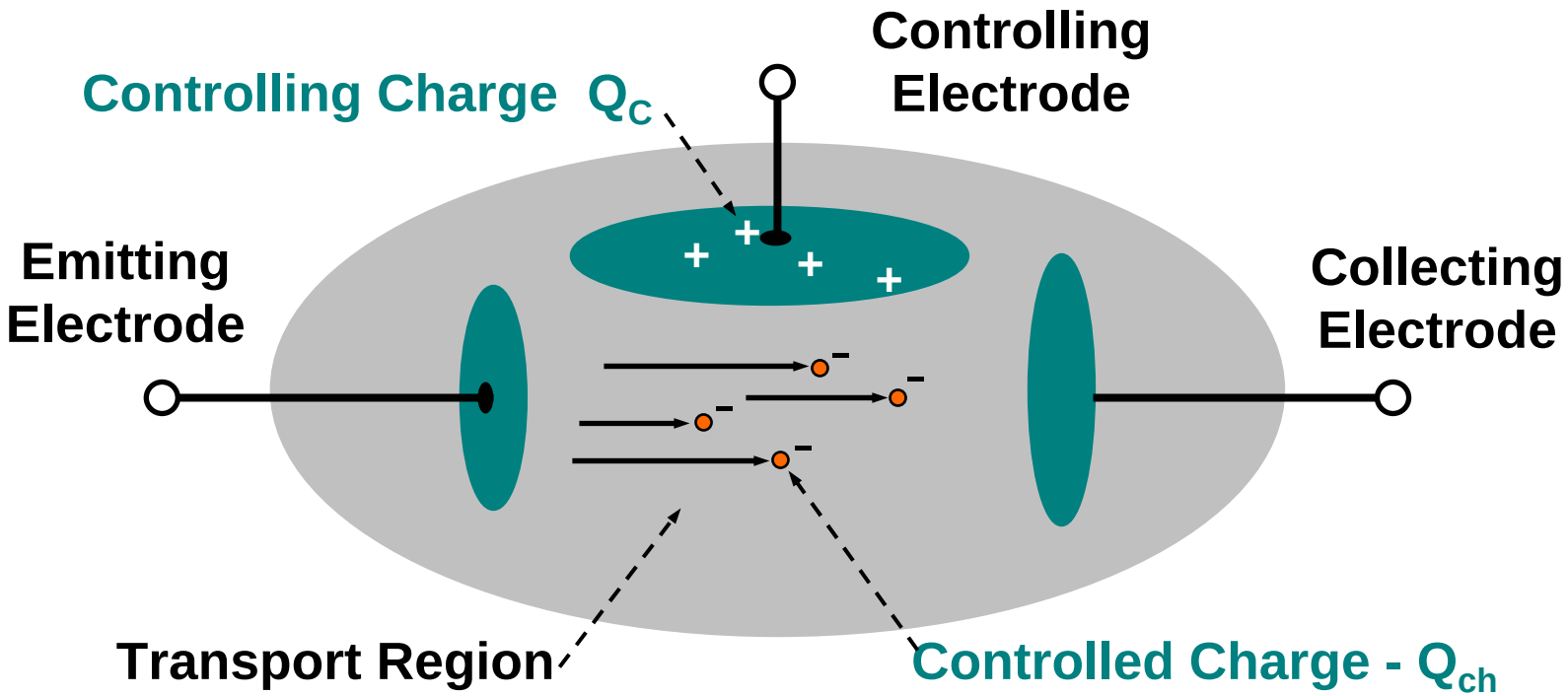
Materials Summary

- Material transport properties
  - **better v_{sat} for electrons in III-V**
  - **performance edge when speed or bandwidth are the main goals**
- Heterojunctions add to device performance
  - **holes and electrons can be independently controlled**
  - **lowest noise FETs, highest f_T, f_{max} HBTs and HEMTs**
- Process
  - **linewidths, circuit densities also critical**
  - **Si and SiGe has huge advantages here**

What makes a transistor fast?

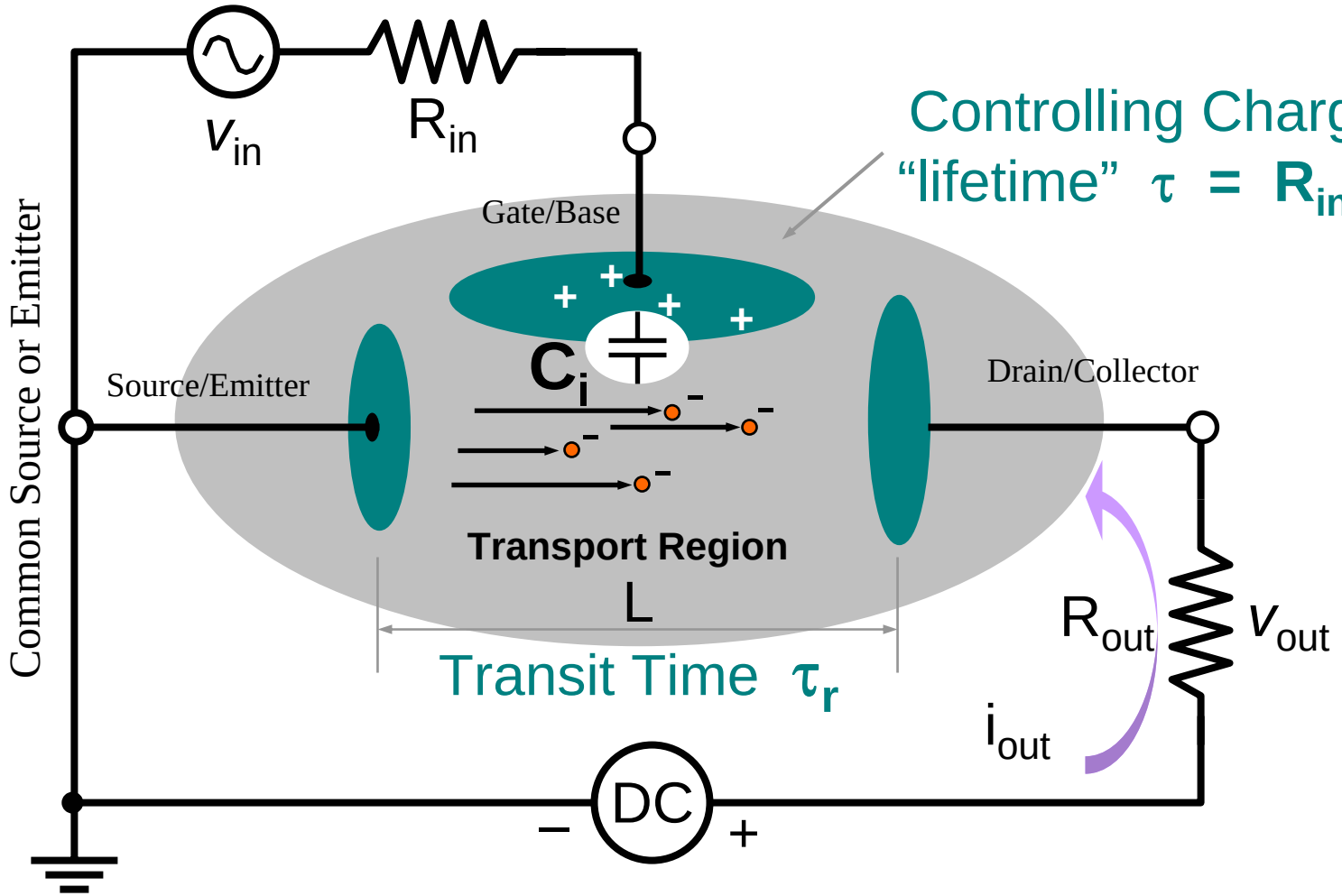
- Decrease transit time
- Reduce access resistance
- Decrease RC delays
- Figures of Merit do not necessarily predict performance for every circuit application

Active device used to discuss the "charge control principle"



CHARGE CONTROL PRINCIPLE: A charge Q_C on the control electrode can at most introduce an equal charge in the transport region. In symbols, $-Q_{ch} \leq Q_C$

Introduction of “charge control” time constants



We have introduced two time constants: τ and τ_r

Consider the transconductance -- g_m

By definition g_m is

$$g_m = \frac{-\Delta i_{out}}{\Delta v_{in}} .$$

But capacitance $C_i = \dfrac{\Delta Q_c}{\Delta v_{in}}$,

Output current $\Delta i_{out} = \dfrac{-\Delta Q_c}{\tau_r}$ from charge control.

Hence, we get $\mathbf{g_m = \dfrac{C_i}{\tau_r}}$ ← Charge Control form

Maximizing Active Device Transconductance (g_m)

$$g_m = \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{V_{out}} \Rightarrow g_m = \frac{C_i}{\tau_r}$$

C_i is a measure of the work required to introduce a charge carrier

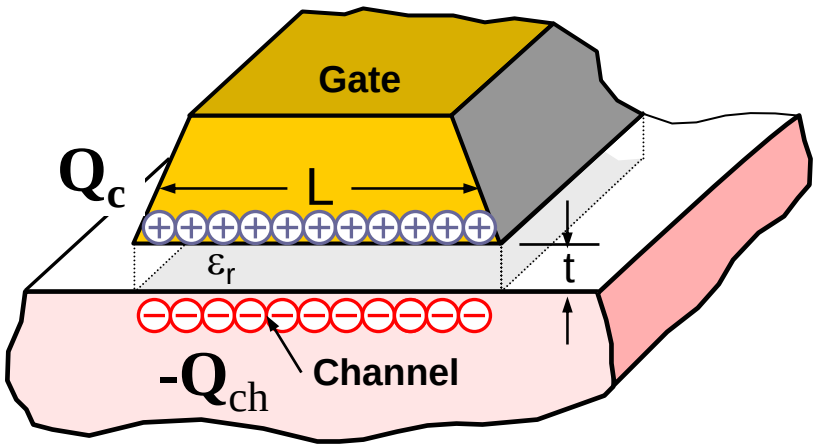
τ_r is average transit time of a charge carrier

(1) Transit time τ_r depends upon
- a. Charge carrier velocity (material dependent)
- b. Transport region length (geometry)

(2) Input capacitance C_i depends upon
- a. Charge separation (for FET the gate-to-channel spacing & BJT merged charge in base)
- b. Dielectric constant (material dependent)

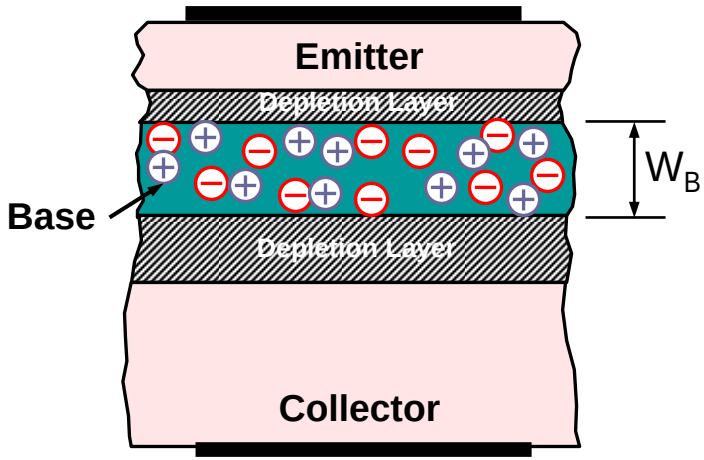
Maximizing Controlled Charge in Devices

FET Structure



Control charge Q_c is separated from controlled charge $-Q_{ch}$

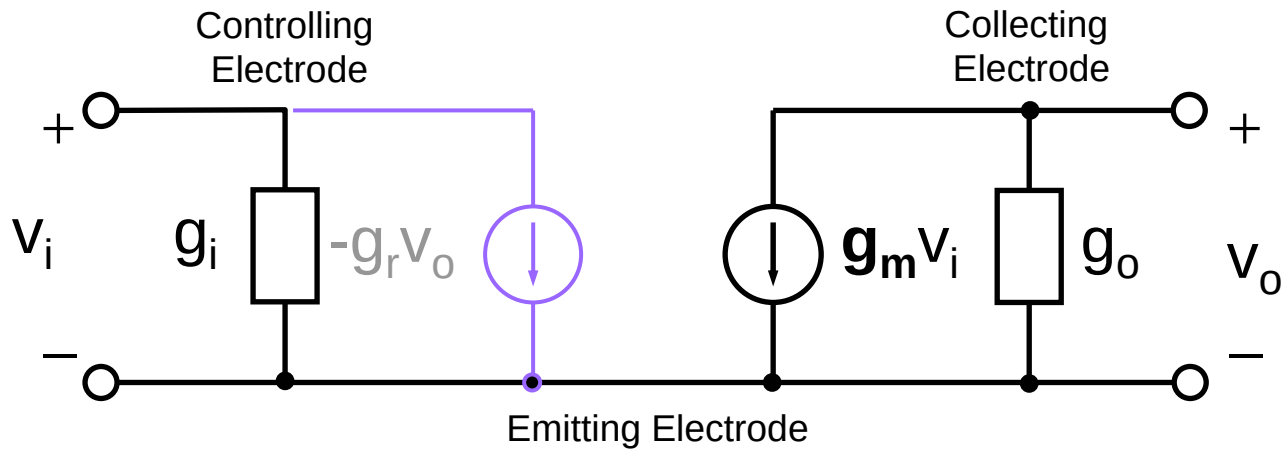
BJT/HBT Structure



Control charge Q_c & controlled charge $-Q_{ch}$ share base region

Small-Signal Charge Control Model

(No parasitic or external components included -- intrinsic model only)



$$g_i = \frac{C_i}{\tau} \qquad \boxed{g_m = \frac{C_i}{\tau_r}}$$

$$g_r = -\frac{C_0}{\tau} \qquad g_o = \frac{C_o}{\tau_r}$$

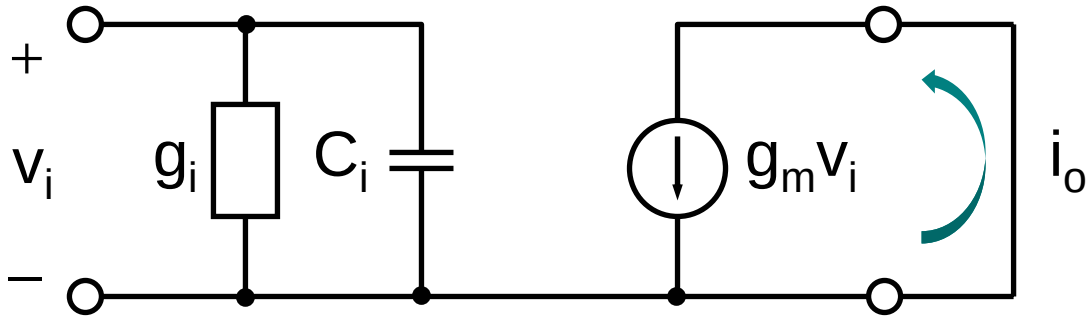
Where τ = controlling charge "lifetime" and τ_r = transit time; also output capacitance C_o is from unwanted charge at collecting electrode coupling to ground.

Circuit Performance

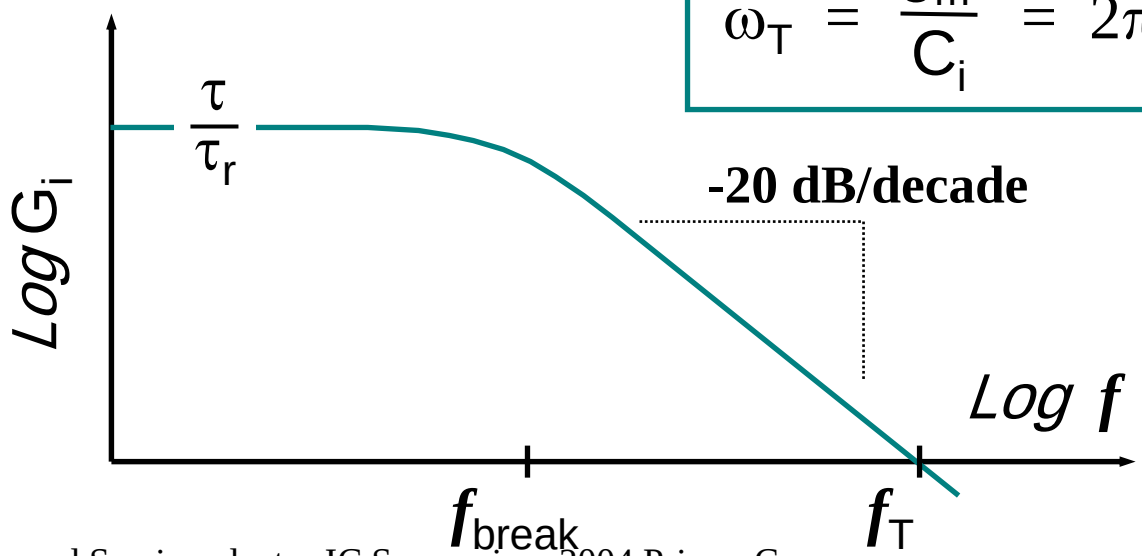
- Figures of Merit: f_T, f_{max}
- Static Frequency Dividers

An Interpretation of Current Gain-Bandwidth Product f_T

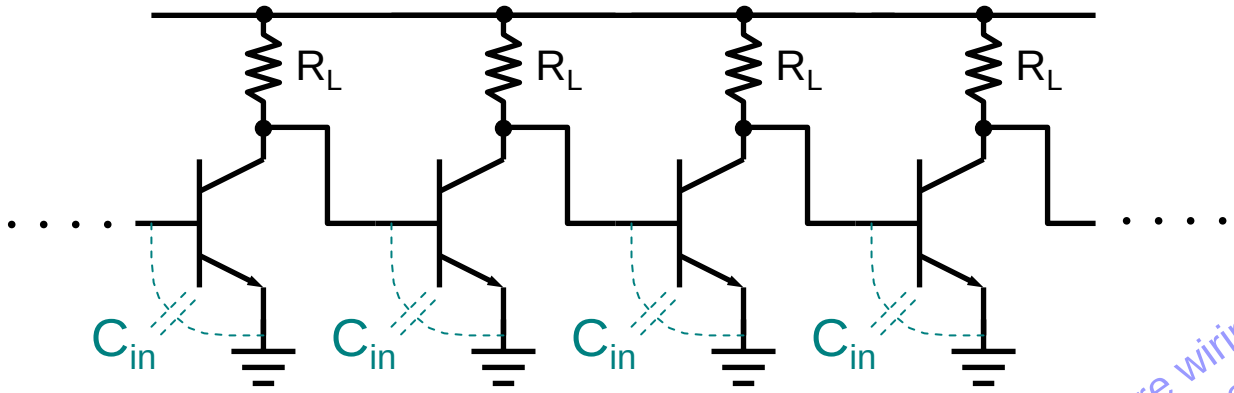
Starting with $G_i = \dfrac{1}{\omega\tau_r}$ then if $G_i = 1$ implies $\omega_T = \dfrac{1}{\tau_r}$



$$\omega_T = \frac{g_m}{C_i} = 2\pi f_T$$



Cascade of Common-Emitter Stages



Ignore wiring & other parasitic capacitances

$$\text{Gain/stage} = -g_m R_L$$

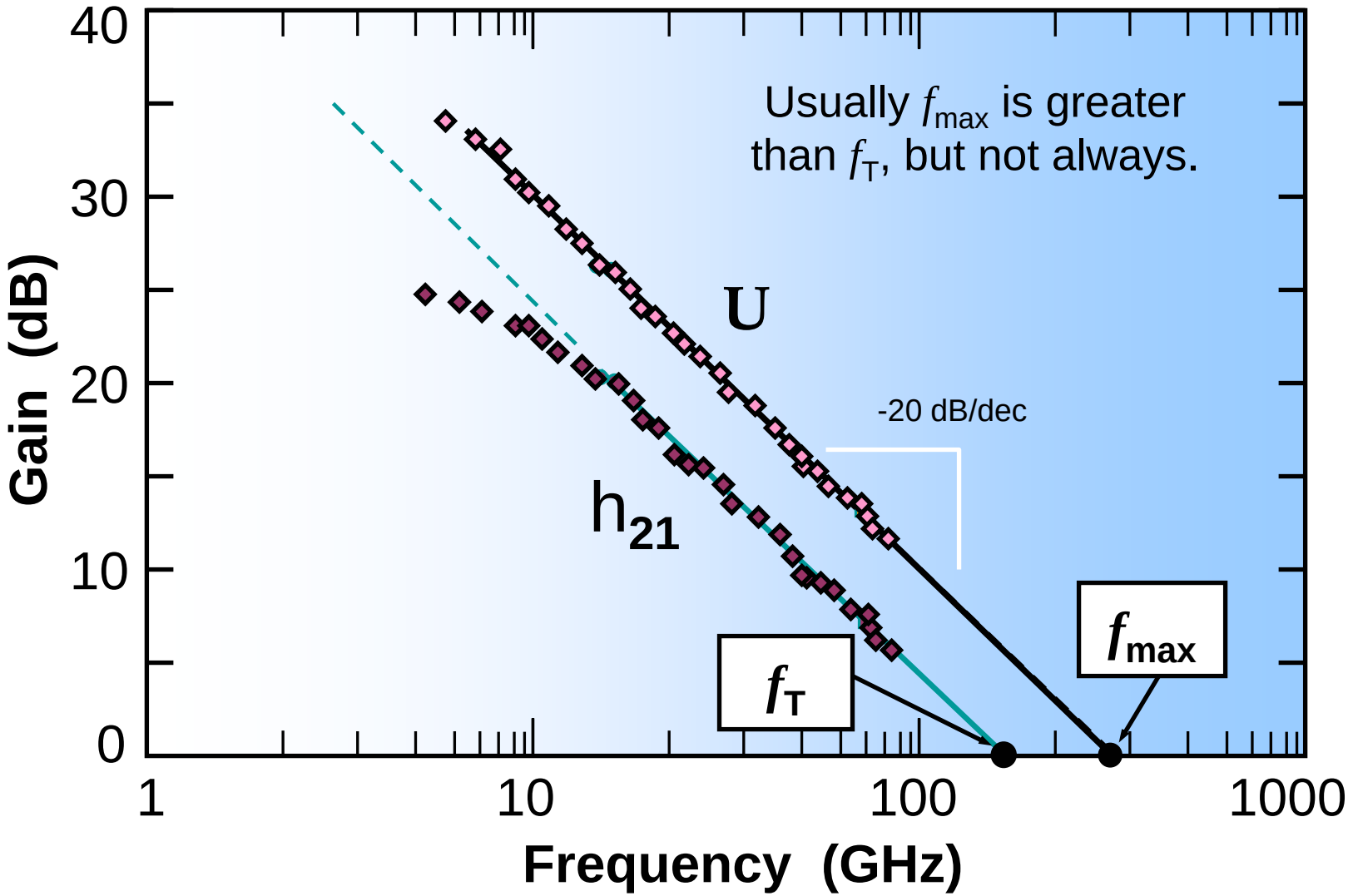
$$\text{Bandwidth} = 1/(2\pi R_L C_{in})$$

$$\text{GBW -Product} = g_m/2\pi C_{in} = f_T$$

f_T is a rough measure of how well an active device can perform when cascaded with a chain of identical active devices.

Historically, f_T was easiest parameter to measure.

Figures of Merit – Include h_{21} and f_T

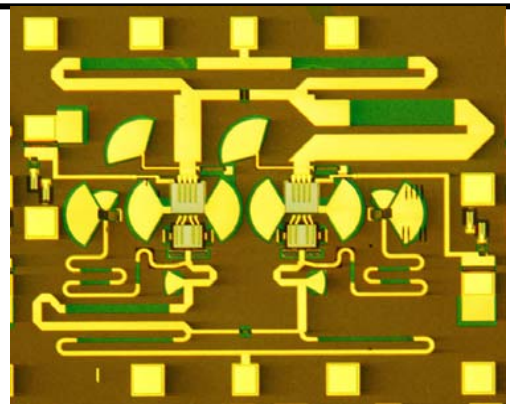


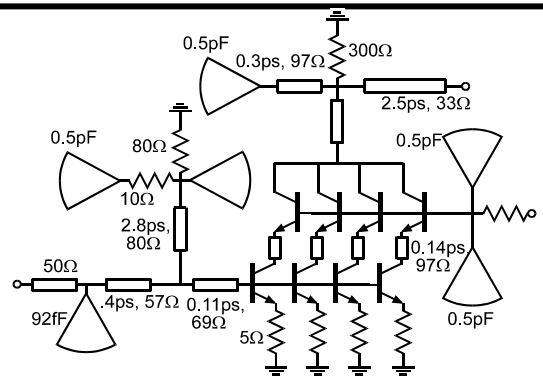
D. Estreich, Compound Semiconductor IC Symposium 2004 Primer Course

What do we need: f_τ , f_{max} , or … ?

Tuned ICs (MIMICs, RF):
fmax sets gain,
& max frequency, not ft.

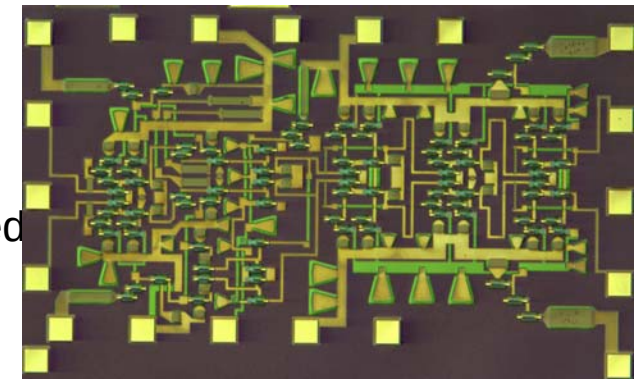
…low ft/fmax ratio makes tuning design hard (high Q)

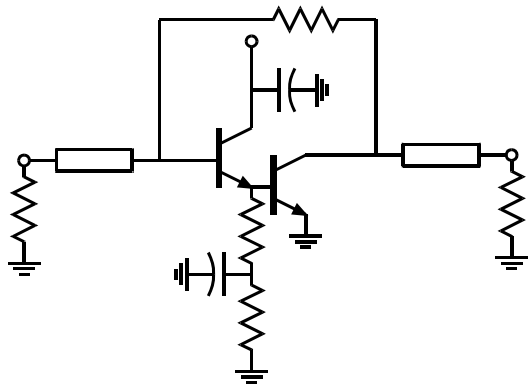




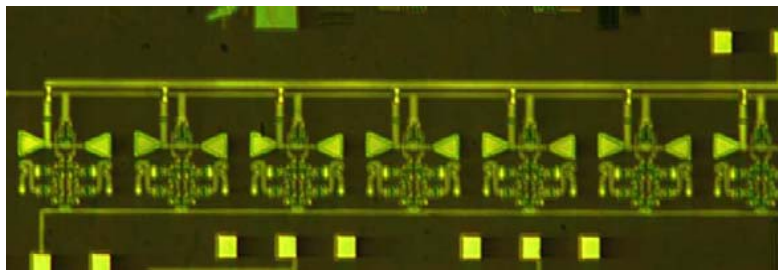
Lumped analog circuits
need high & comparable ft and fmax.

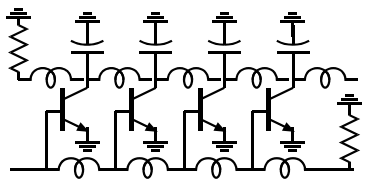
(1.5:1 fmax/ft ratio often cited as good…)





Distributed Amplifiers
in principle, fmax-limited,
ft not relevant….
(low ft makes design hard)





What determines digital circuit speed?

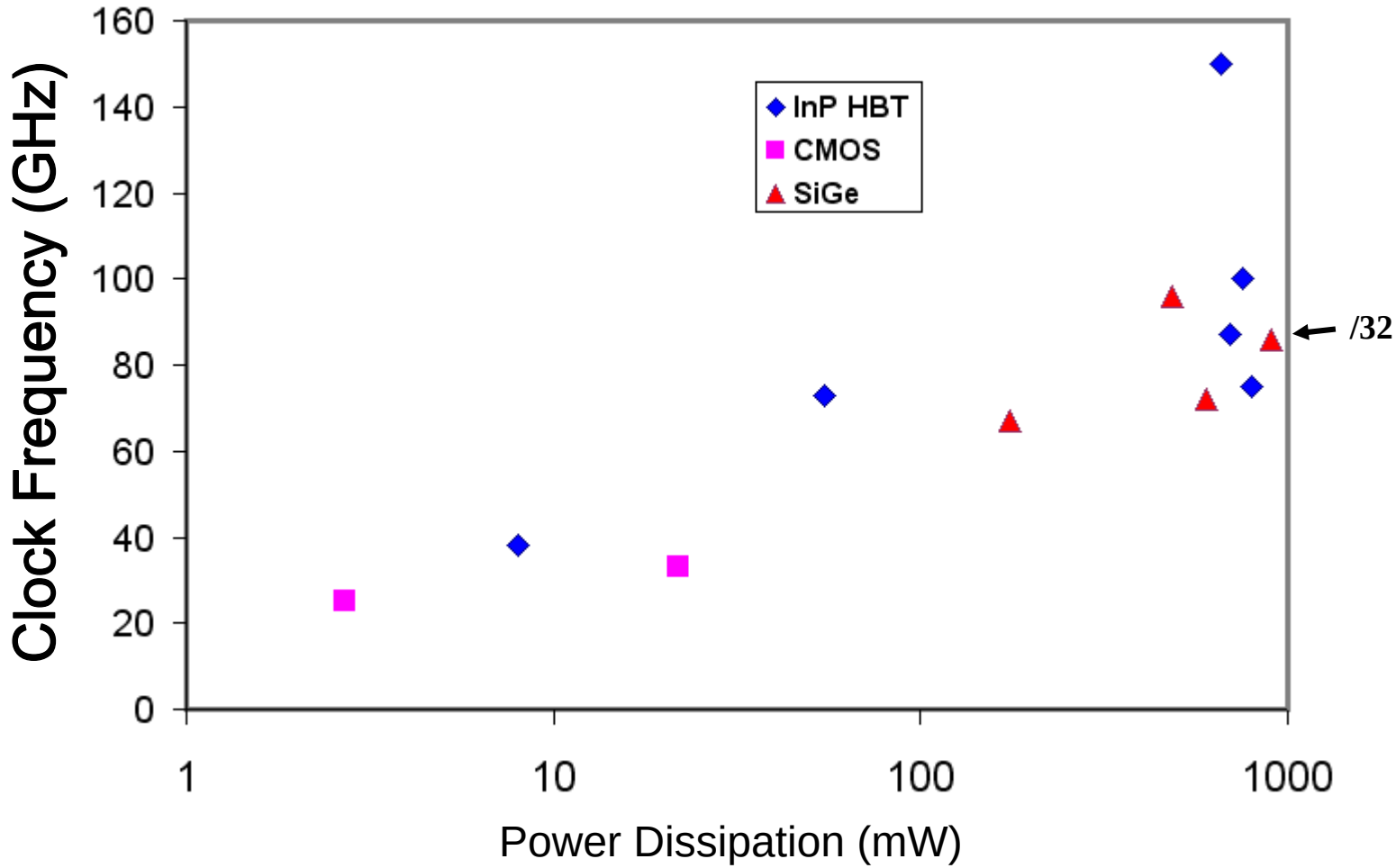
- Neither f_T nor f_{max} predict digital circuit speed

$$\frac{1}{2\pi f_T} = \tau_B + \tau_C + \frac{kT}{qI_C}\left(C_{je} + C_{cb}\right) + \left(R_{ex} + r_c\right)C_{cb}$$

$$f_{\max} = \sqrt{f_T / 8\pi R_{bb} C_{cb}}$$

- RC time constant analysis can guide the design
- Must minimize interconnect RC loading and maximize device current per area.

Frequency Dividers - 2004



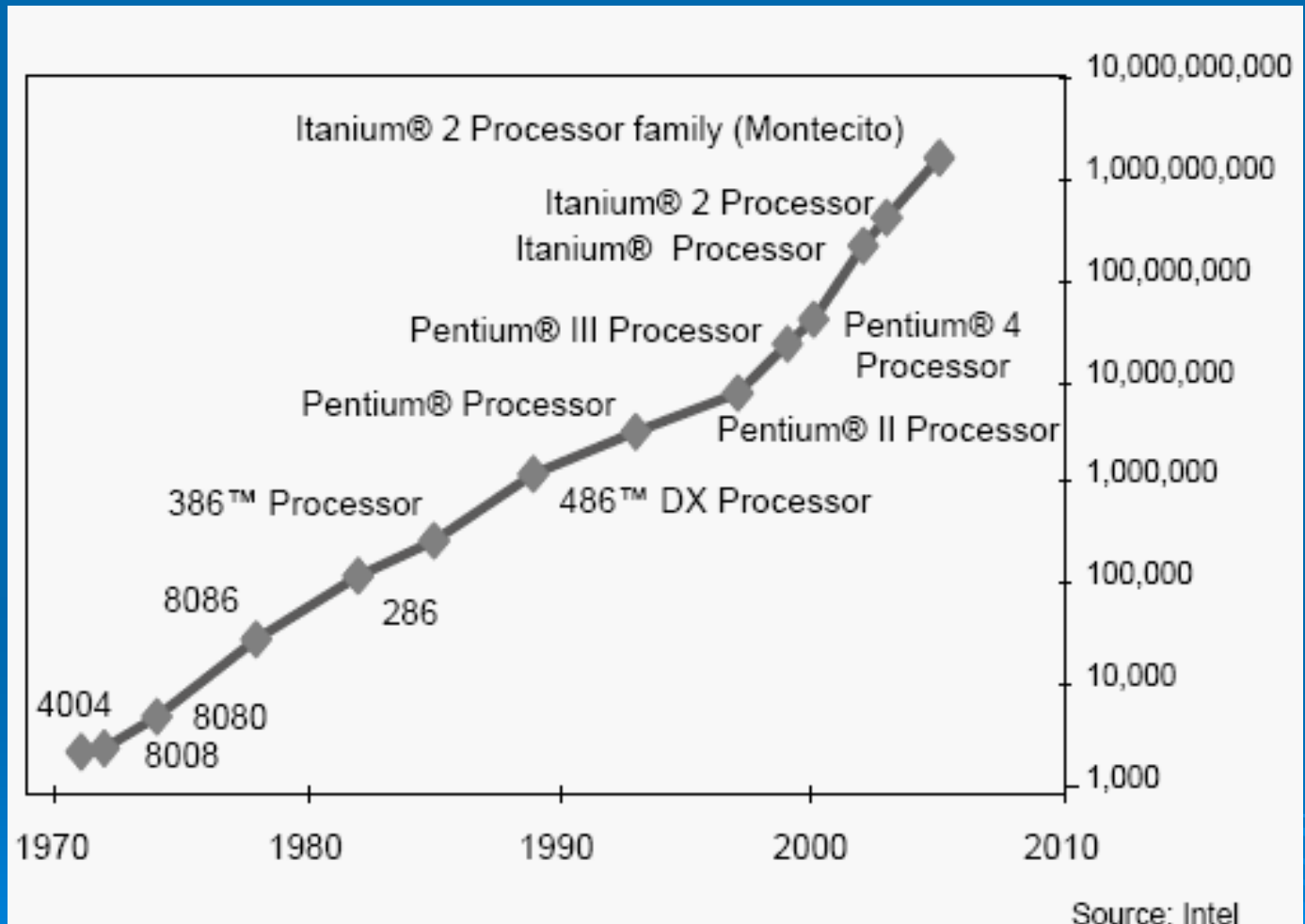
Benchmark: master-slave flip-flop configured as 2:1 **static** frequency divider

S. Long, Compound Semiconductor IC Symposium 2004 Primer Course

Scaling trends for CMOS

- Complexity
- Processing issues
- Performance trends and tradeoffs
- Future device innovations
- Scaling effects on analog circuits

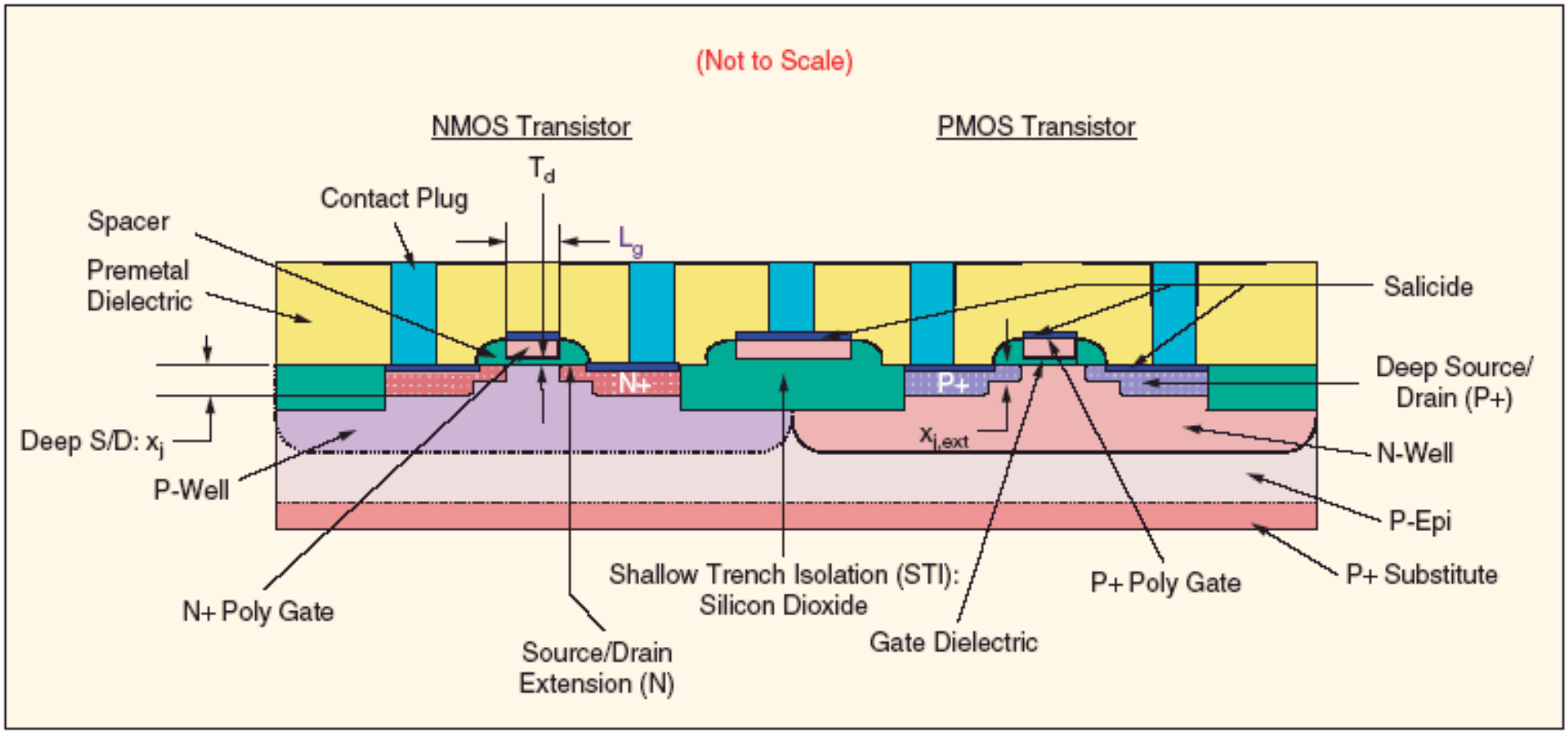
Growth in Complexity



Sunlin Chou, ISSCC 2005 Plenary Speech

Figure 1.3.1: Transistors per microprocessor.

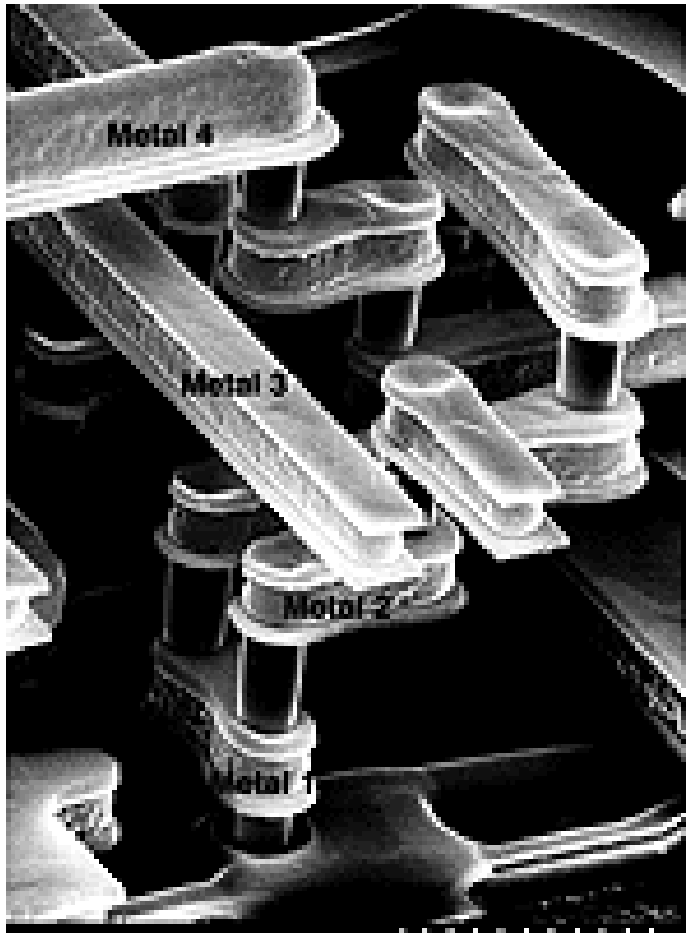
A Modern CMOS Process



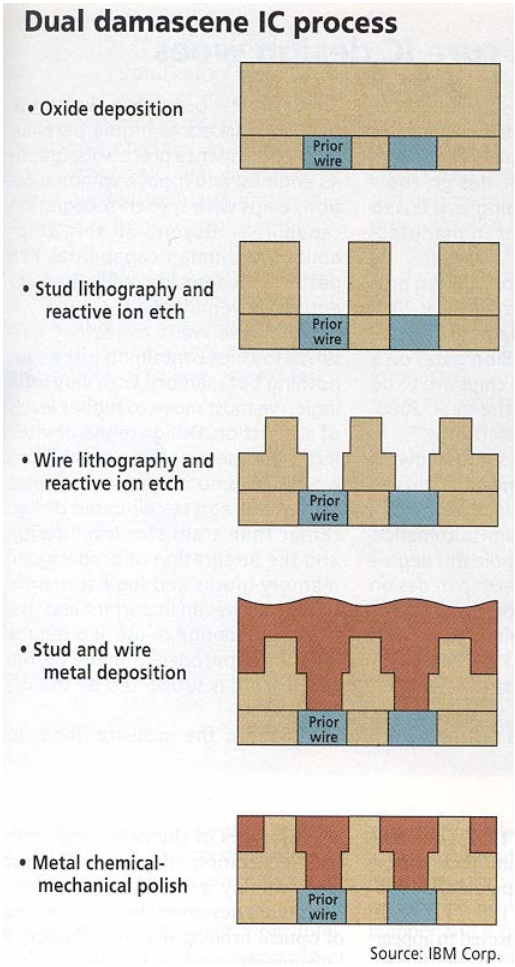
8. Schematic cross section of a typical PMOSFET and NMOSFET. (Figure from [3].)

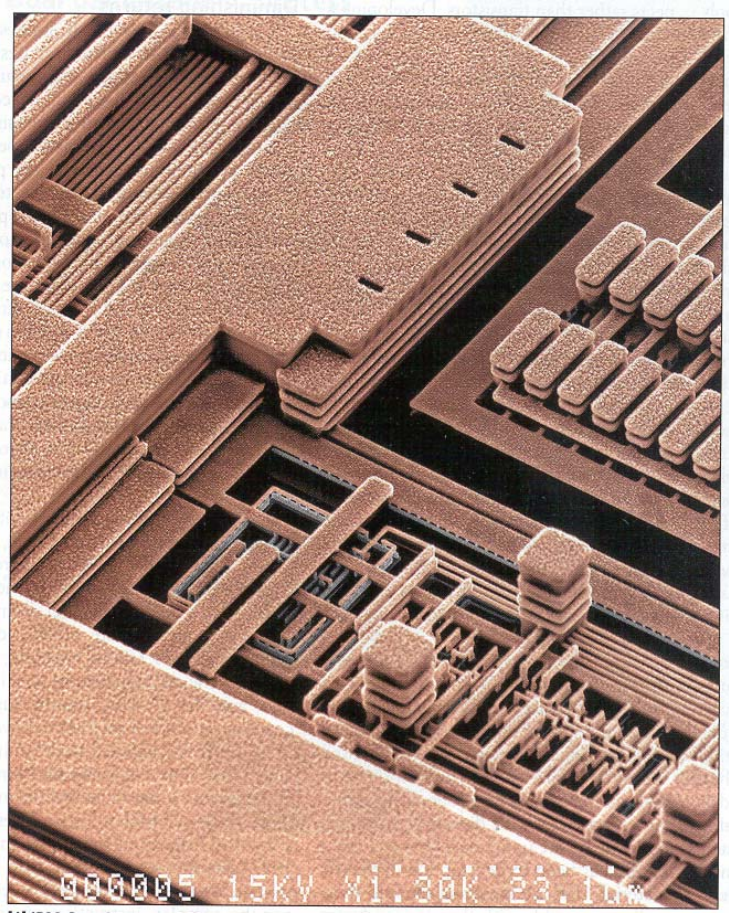
P. Zeitzoff, J. Chung, “A Perspective from the 2003 ITRS Roadmap, IEEE Circuits And Devices Magazine,” Jan-Feb 2005.

Advanced Metallization



Advanced Metallization





ITRS Roadmap for Silicon

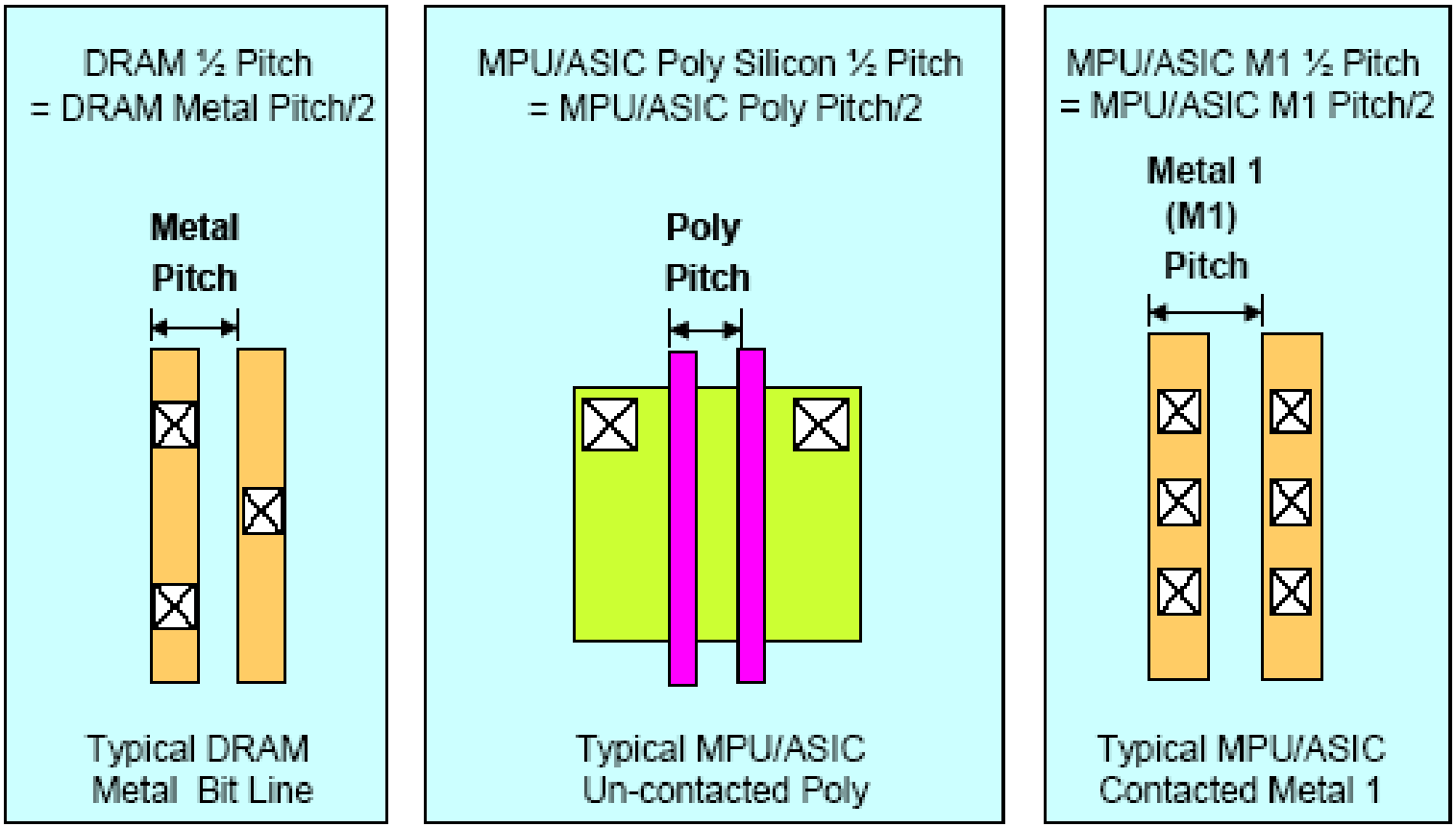


Figure 4 Definition of Metal Half Pitch

Half-pitch history

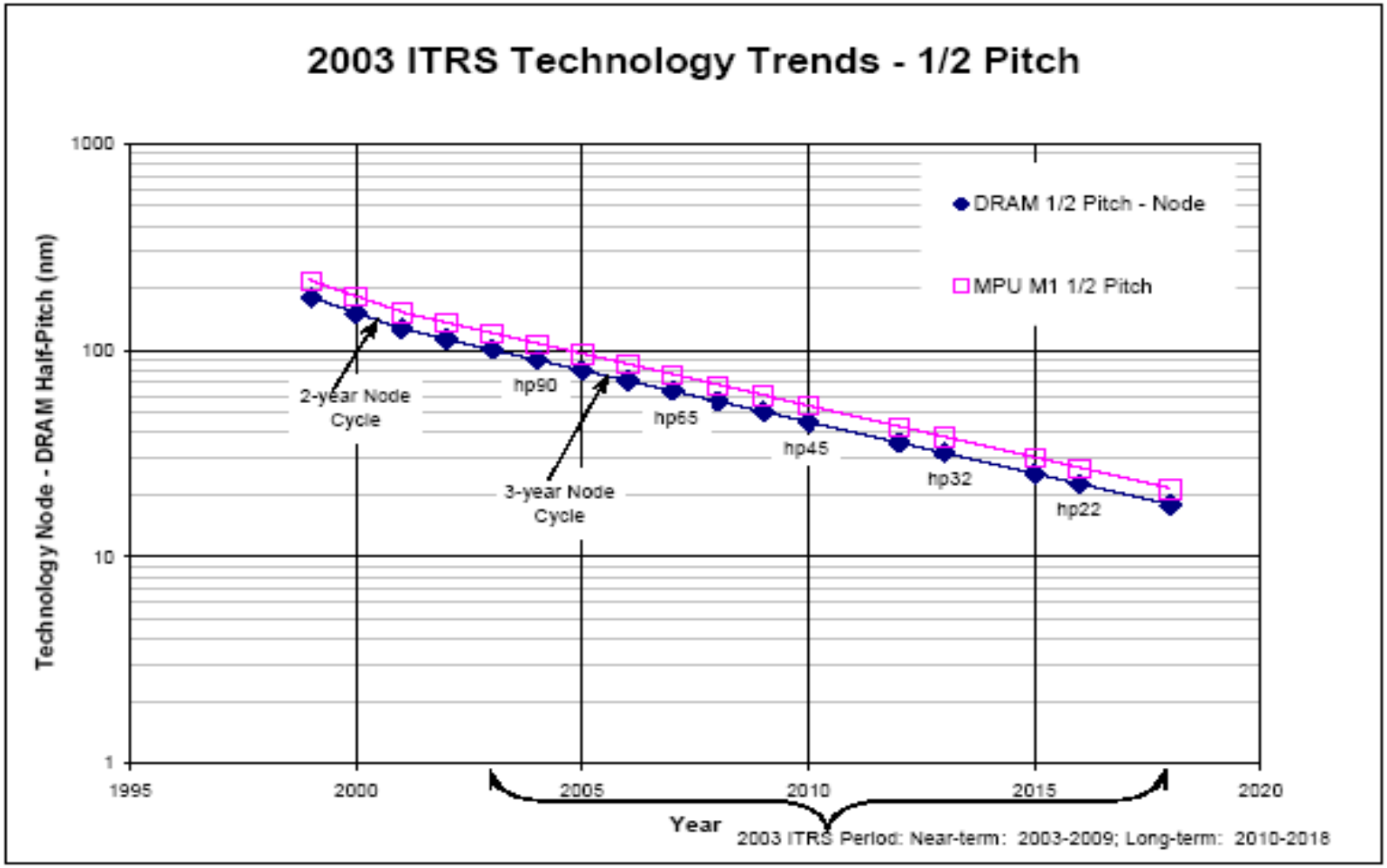
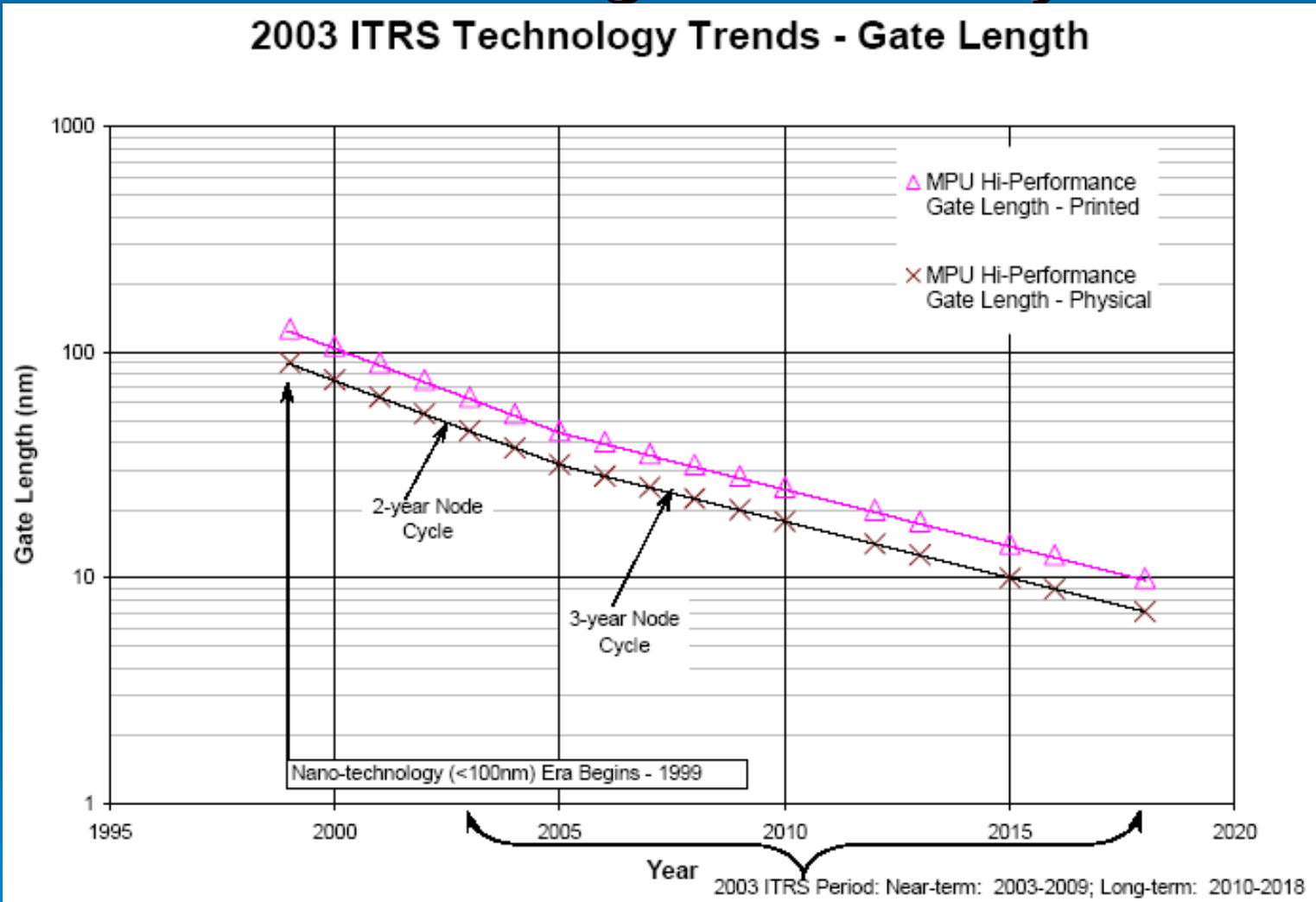


Figure 7 2003 ITRS—Half Pitch Trends

http://public.itrs.net

Still on the target – 2004 ITRS

Gate Length History

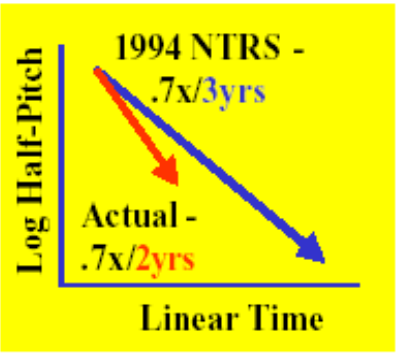


public.itrs.net from 2003 ITRS executive summary

Scaling of Lithography

Scaling Calculator +

Node Cycle Time:



0.7x 0.7x

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5x

N N+1 N+2

* CARR(T) = Compound Annual Reduction Rate (@ cycle time period, T)

Node Cycle Time (T yrs):

*CARR(T) =

[(0.5)^(1/2T yrs)] - 1

CARR(3 yrs) = -10.9%

CARR(2 yrs) = -15.9%

Scaling Challenges

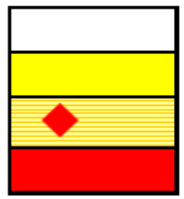
- Lithography
  - 193nm with lithographically friendly design rules
  - 193nm immersion lithography
  - 157nm? EUV?
- Power dissipation: $P=CV^2f + NWI_{off}Vdd$
  - Gate leakage current
  - Disproportionate scaling of Vdd and Vth
  - Off current increases with each generation
- Boron diffusion from p+ gate thru oxide

2004 Roadmap for Lithography

Table 77a Lithography Technology Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM							
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	Contact in resist (nm)	130	110	100	90	80	70	60
	Contact after etch (nm)	115	100	90	80	70	65	55
WAS	Overlay	35	32	28	25	23	21	19
IS	Overlay [A]	35	32	28	25	23	21	19
	CD control (3 sigma) (nm)	12.2	11	9.8	8.6	8	7	6.1
	MPU							
	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	120	107	95	85	76	67	60
	MPU ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
WAS	MPU gate in resist (nm)	◆ 65	53	45	40	35	32	28
IS	MPU gate in resist (nm)	65	◆ 53	45	40	35	32	28
	MPU gate length after etch (nm)	45	37	32	28	25	22	20
	Contact in resist (nm)	130	122	100	90	80	75	60
	Contact after etch (nm)	120	107	95	85	76	67	60
WAS	Gate CD control (3 sigma) (nm)	◆ 4.0	3.3	2.9	2.5	2.2	2	1.8
IS	Gate CD control (3 sigma) (nm)	◆ 4.0	◆ 3.3	2.9	2.5	2.2	2	1.8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



public.itrs.net

Lithography – 2010 +

Table 77b Lithography Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM									
WAS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Contact in resist (nm)	55		45	40		35	30		25
IS	Contact in resist (nm)	55	50	45	40	37	35	30	27	25
WAS	Contact after etch (m)	50		35	30		25	21		18
IS	Contact after etch (m)	50	40	35	30	28	25	21	20	18
WAS	Overlay	18		14	12.8		10	8.8		7.2
IS	***Overlay [A]***	18	16	14	13	12	10	8.8	8	7.2
WAS	CD control (3 sigma) (nm)	5.5		4.3	3.9		3.1	2.7		2.2
IS	CD control (3 sigma) (nm)	5.5	4.8	4.3	3.9	3.4	3.1	2.7	2.4	2.2
	MPU									
WAS	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54		42	38		30	27		21
IS	MPU/ASCI Metal 1 (M1) ½ pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU ½ Pitch (nm) (uncontacted gate)	45		35	32		25	22		18
IS	MPU ½ Pitch (nm) (uncontacted gate)	45	40	35	32	28	25	22	20	18
WAS	MPU gate in resist (nm)	25		20	18		15	13		10
IS	MPU gate in resist (nm)	25	22	20	18	17	15	13	11	10
WAS	MPU gate length after etch (nm)	18		14	13		10	9		7
IS	MPU gate length after etch (nm)	18	16	14	13	11	10	9	8	7

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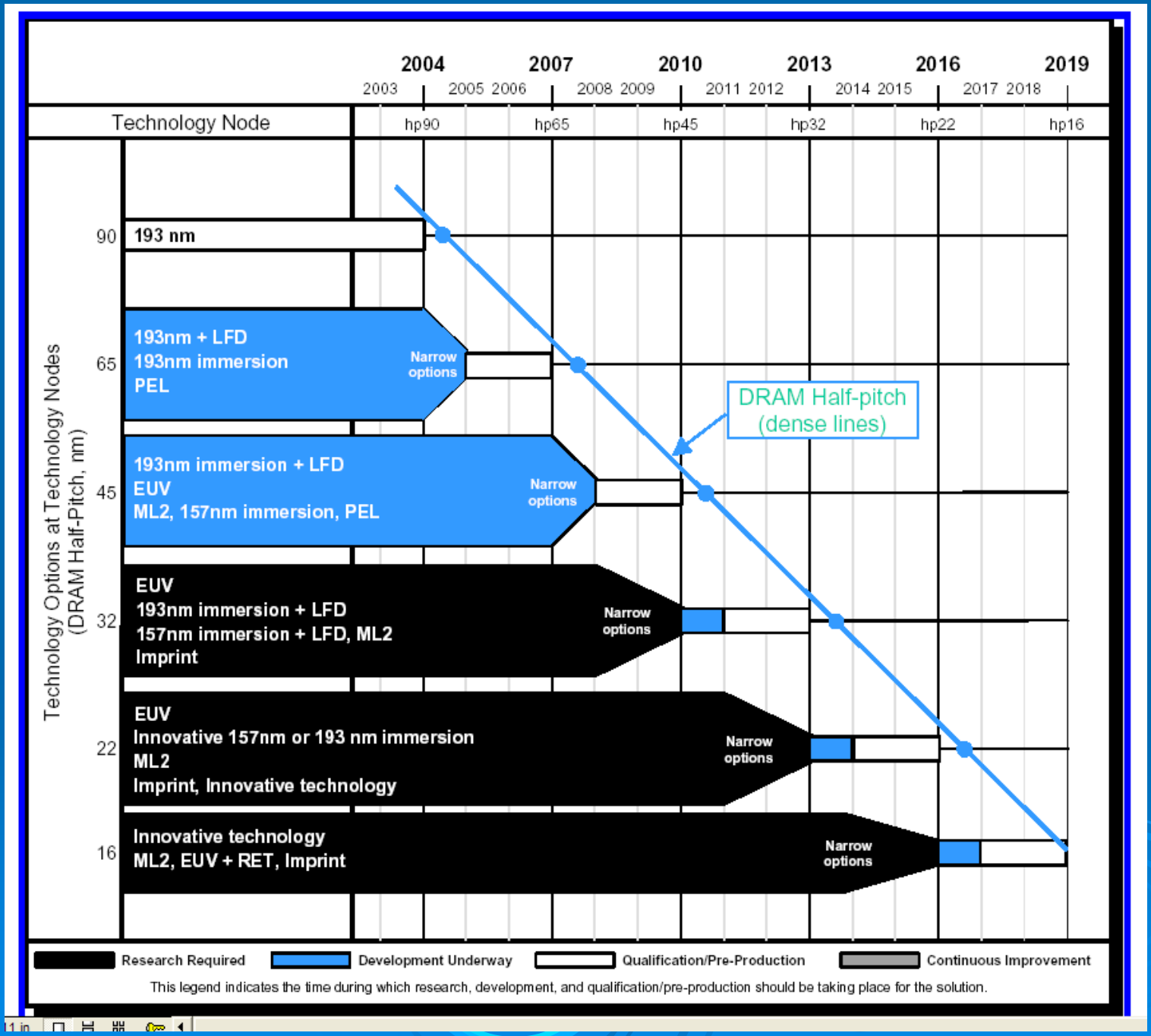

2004
2007
2010
2013
2016
2019
2003
2005 2006
2008 2009
2011 2012
2014 2015
2017 2018
Technology Node
hp90
hp65
hp45
hp32
hp22
hp16
Technology Options at Technology Nodes
(DRAM Half-Pitch, nm)
90
65
45
32
22
16
193 nm
193nm + LFD
193nm immersion
PEL
Narrow options
193nm immersion + LFD
EUV
ML2, 157nm immersion, PEL
Narrow options
EUV
193nm immersion + LFD
157nm immersion + LFD, ML2
Imprint
Narrow options
EUV
Innovative 157nm or 193 nm immersion
ML2
Imprint, Innovative technology
Narrow options
Innovative technology
ML2, EUV + RET, Imprint
Narrow options
DRAM Half-pitch
(dense lines)
Research Required
Development Underway
Qualification/Pre-Production
Continuous Improvement
This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

And: NRE Cost is Increasing

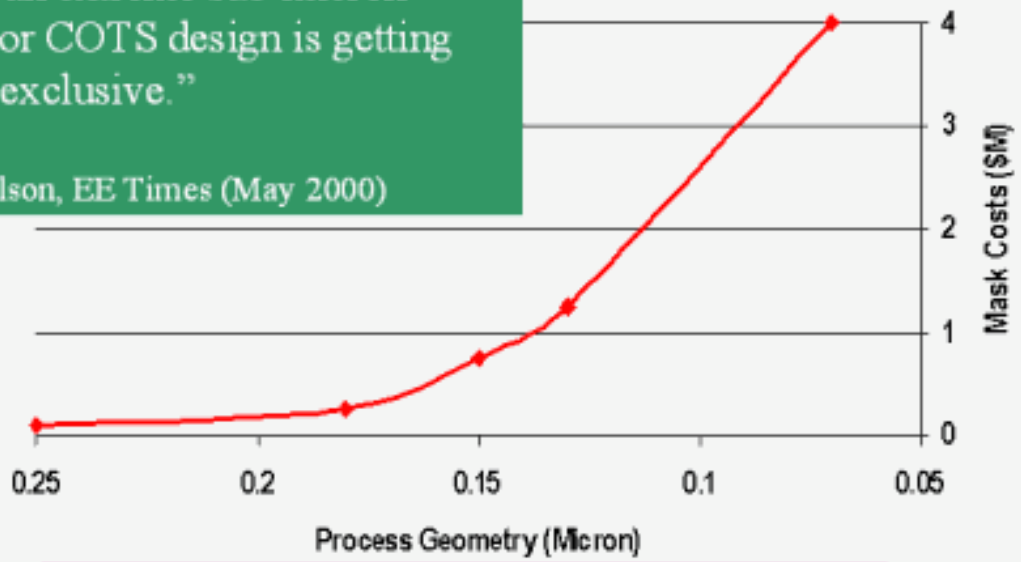
1996 1997 1998 1999 **2000 2001 2002 2003**

The Innovation Revolution

Exploding NRE / Mask Costs

"The club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive."

Ron Wilson, EE Times (May 2000)



70nm ASICs will have $4M NRE

ALTERA. Mentor Graphics XILINX

High Performance Roadmap

Year of Production	2003	2004	2005	2006	2007	2008	2009	2010	2012
Technology Node		hp90			hp65			hp45	
DRAM 1/2 Pitch (nm)	100	90	80	70	65	57	50	45	35
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	18	14
Vdd (V)	1.2	1.2	1.1	1.1	1.1	1	1	1	0.9
Chip Frequency (MHz)									
On-chip local clock	2,976	4,171	5,204	6,783	9,285	10,972	12,369	15,079	20,065
Allowable Maximum Power									
High-performance with heatsink (W)	149	158	167	180	189	200	210	218	240
Cost-performance (W)	80	84	91	98	104	109	114	120	131
Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614	773	1,227

P. Zeitzoff, J. Chung, “A Perspective from the 2003 ITRS Roadmap, IEEE Circuits And Devices Magazine,” Jan-Feb 2005.

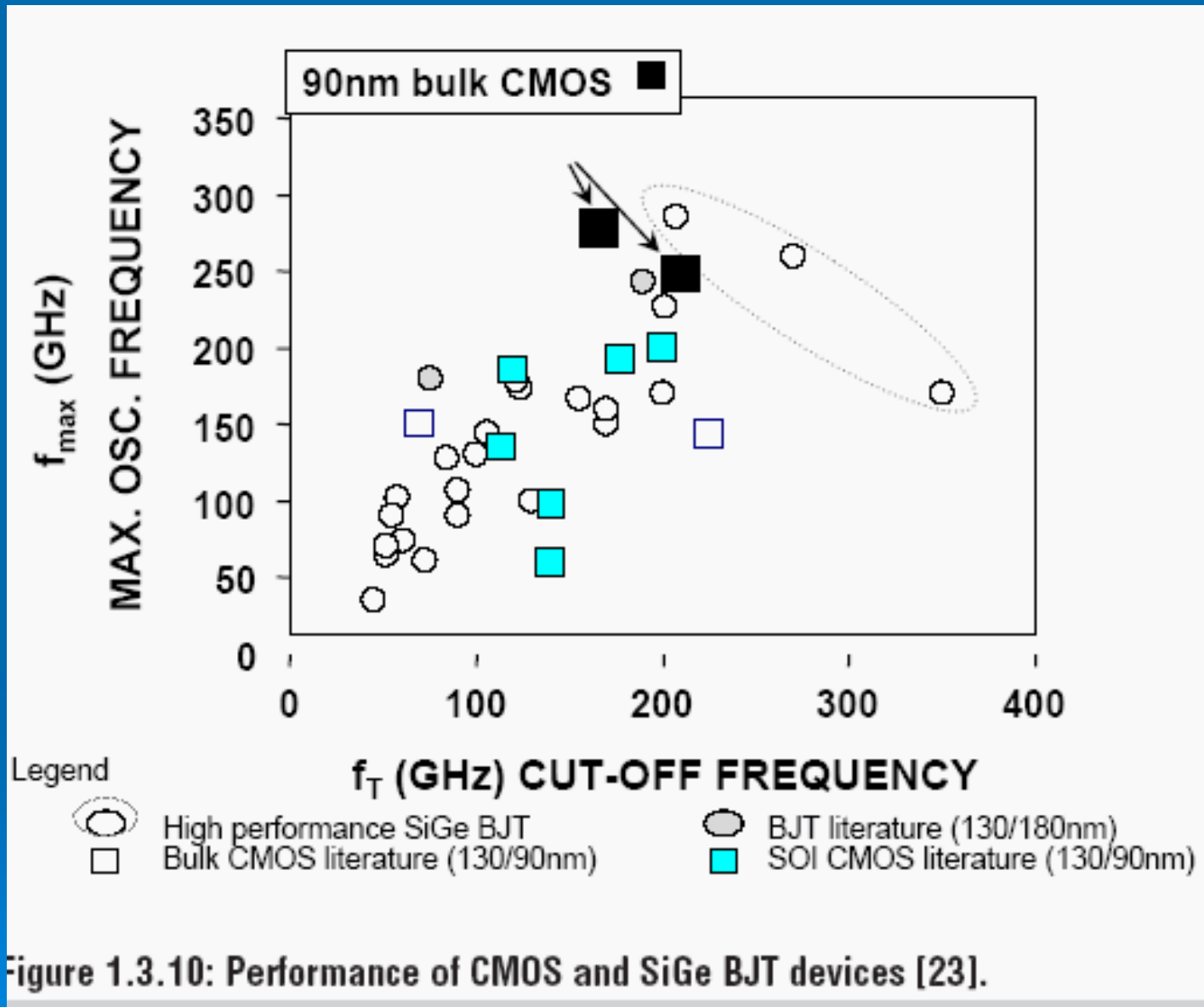
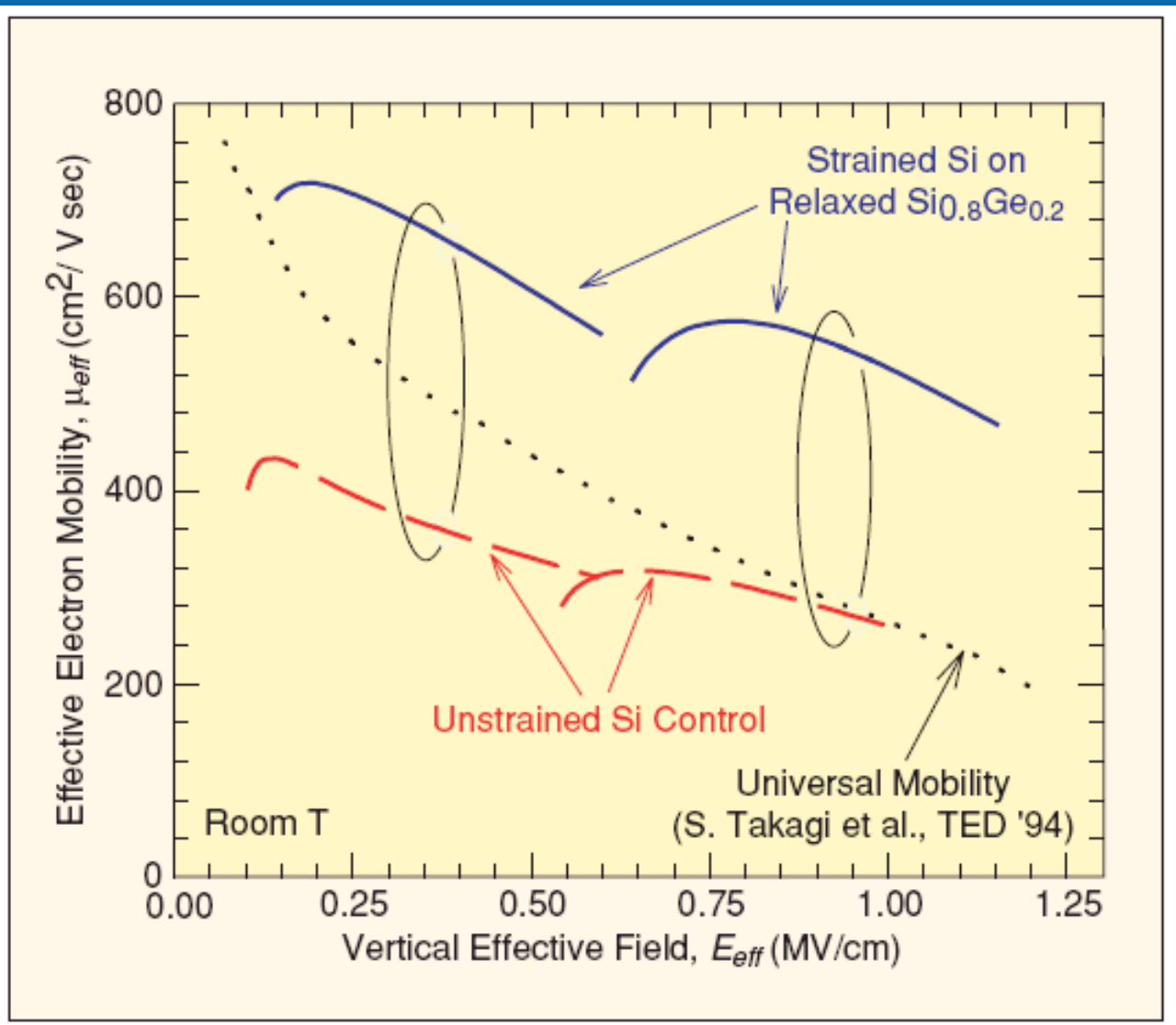
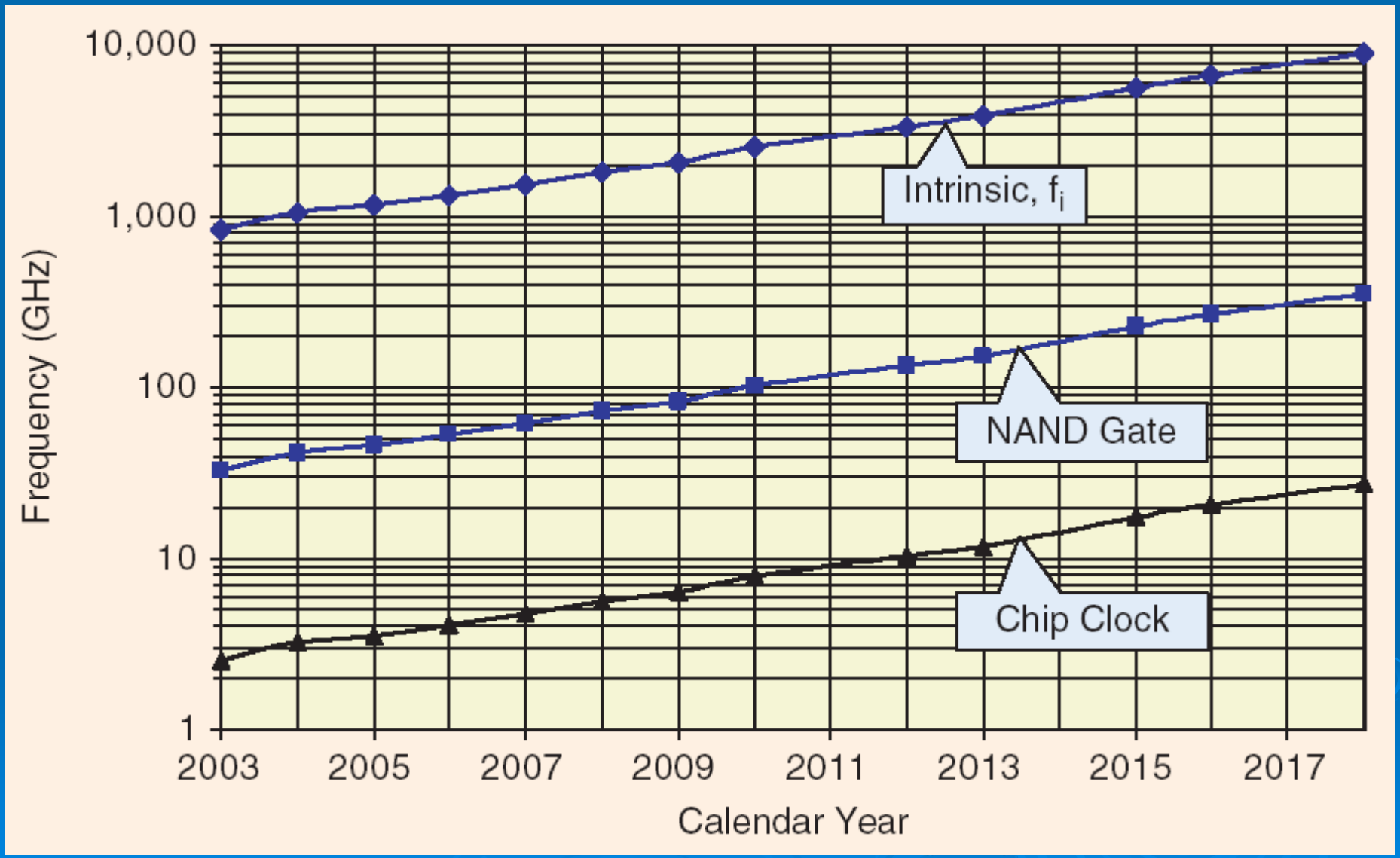


Figure 1.3.10: Performance of CMOS and SiGe BJT devices [23].

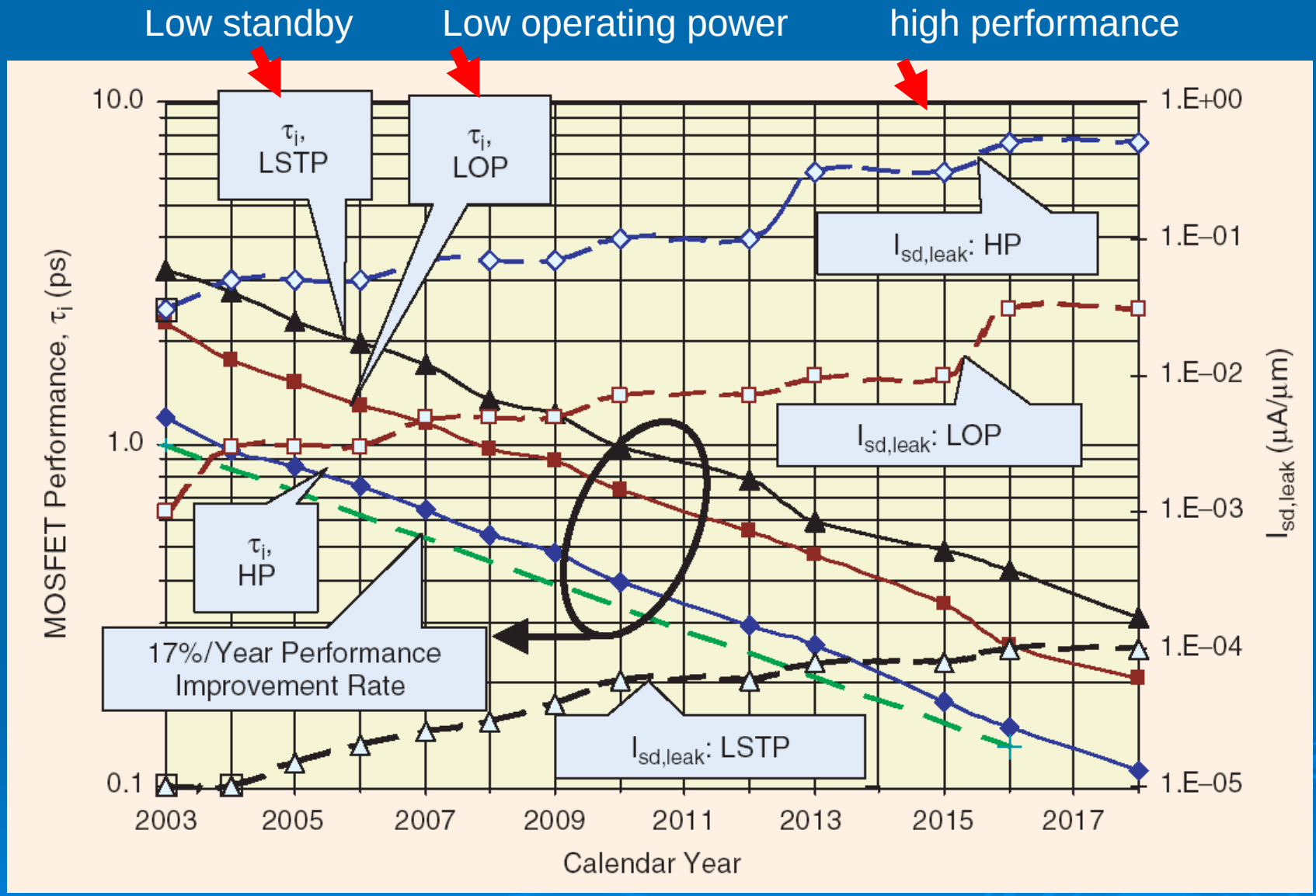
Sunlin Chou, ISSCC 2005 Plenary Speech



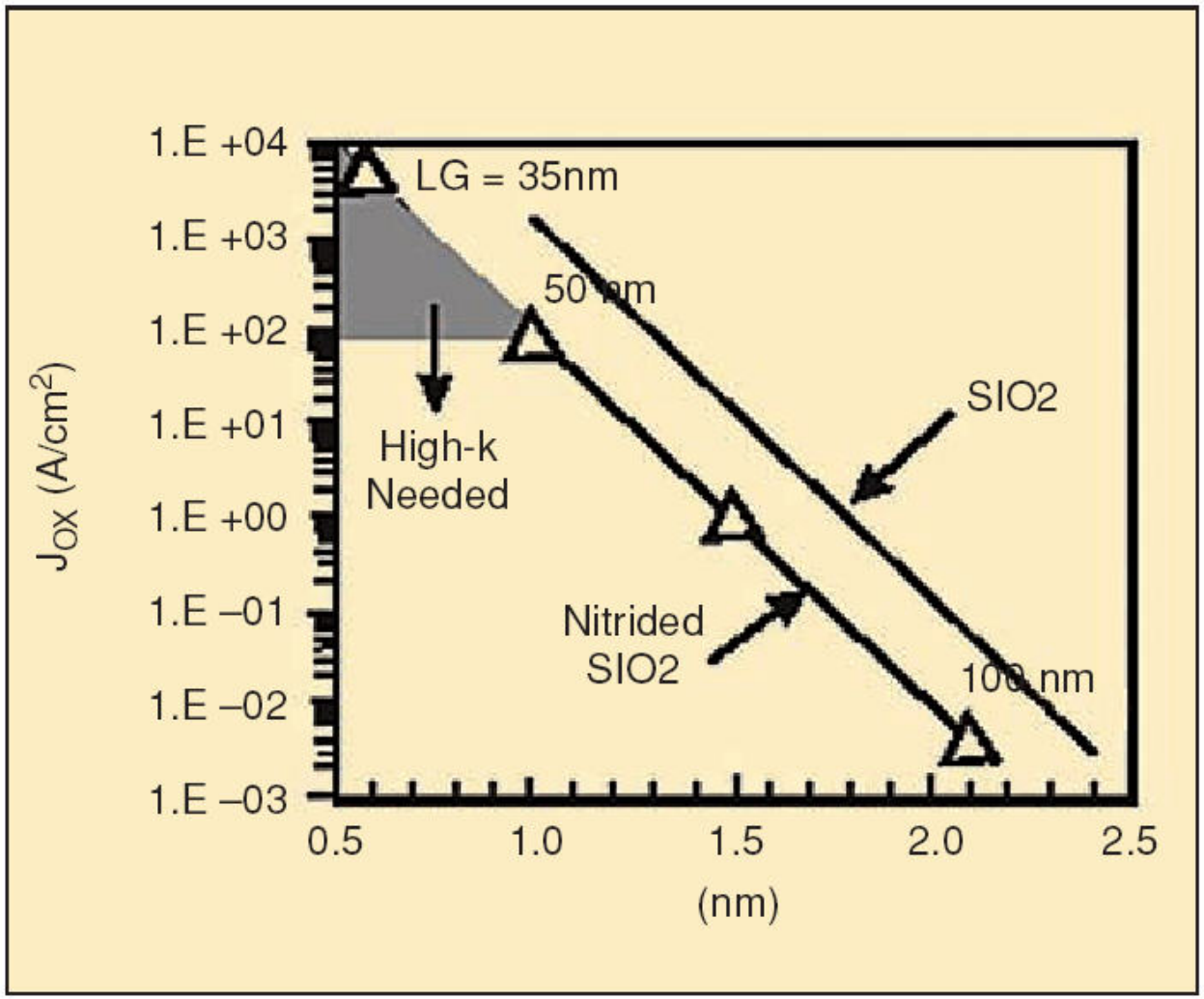
9. Electron mobility enhancement in strained Si MOSFETs [18]. Electron mobility enhancement of ~1.8 × persists up to high E_{eff} (~ 1 MV/cm). Strained-Si allows "moving off" of the universal mobility curve.



P. Zeitzoff, J. Chung, “A Perspective from the 2003 ITRS Roadmap, IEEE Circuits And Devices Magazine,” Jan-Feb 2005.



P. Zeitzoff, J. Chung, “A Perspective from the 2003 ITRS Roadmap, IEEE Circuits And Devices Magazine,” Jan-Feb 2005.



9. Gate leakage dependence on physically effective oxide thickness for pure and nitrided oxide [33].

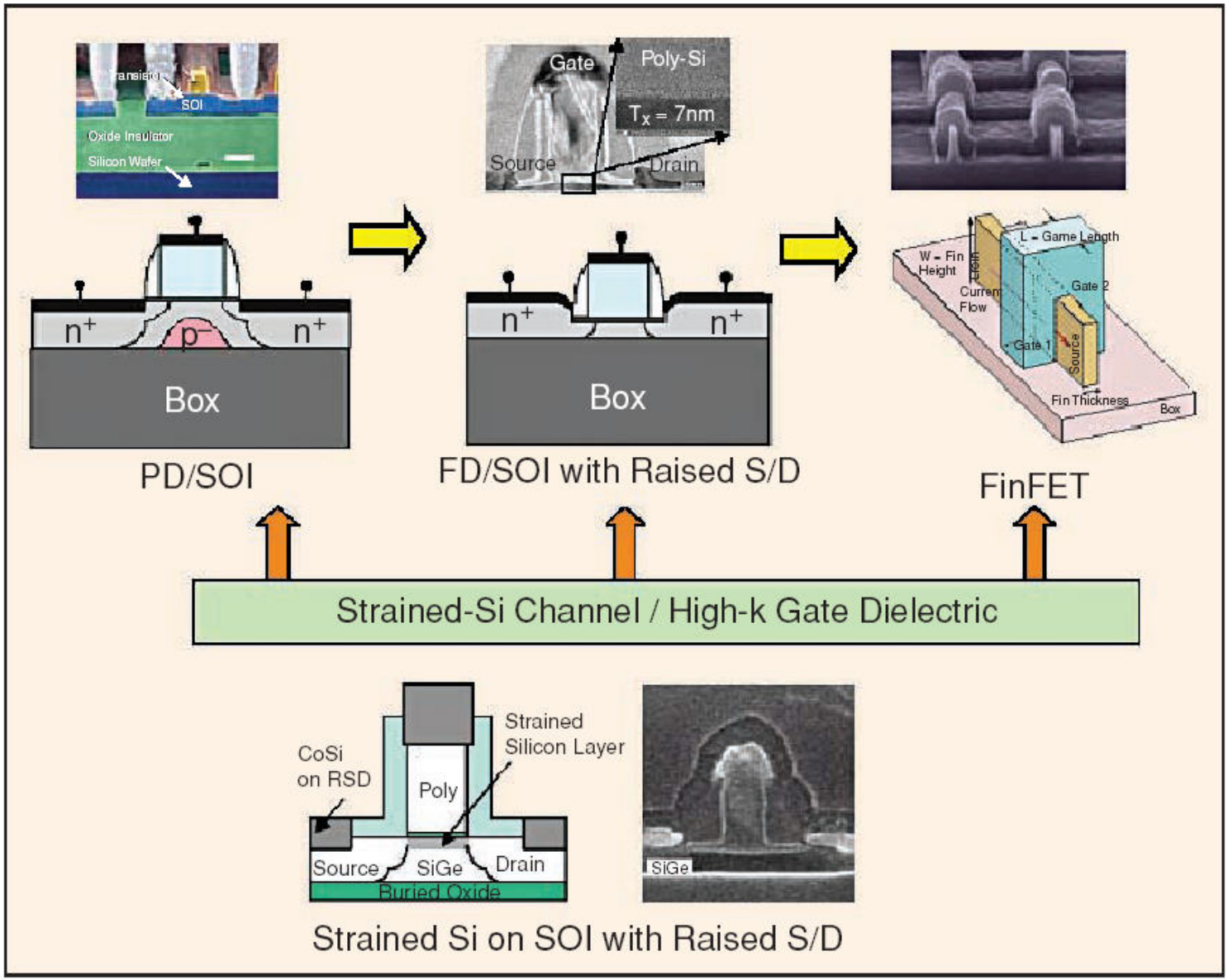
C.T. Chuang et al., "Scaling Planar Silicon Devices," IEEE Circuits And Devices Magazine," Jan-Feb 2004.

Tradeoffs

- High Performance
  - High speed in exchange for high leakage
- Low Standby Power
  - Lower speed in exchange for low leakage

Critical problems to be solved

- Hi k dielectric gate materials (2006-7)
  - Leakage unacceptably high in next generation
- Polysilicon depletion in gate electrode
  - Metal gates (2007 and beyond)
- Planar bulk CMOS inadequate? (>2008)
  - Fully-depleted SOI
  - FINFET
  - Nonclassical structures



1. High-performance logic technology roadmap. Device structure evolution: from PD SOI [3] to FD SOI with raised source/drain [6] to FinFET [9].

C.T. Chuang et al., "Scaling Planar Silicon Devices," IEEE Circuits And Devices Magazine," Jan-Feb 2004.

Scaling: challenges for analog

- Scaling causes mismatches to increase due to finer geometry, higher deviation in threshold voltages and current/voltage gains.
- Lower supply voltage reduces dynamic range and linearity.
- Lower supply voltage makes switches more resistive – bad for Track/Hold

Scaling: challenges for analog

- Higher output conductance degrades gain
  - Triode region is extended
- Higher gate and drain/source leakages increase power and influence accuracy of THA
- More “Moore” will happen – mixed signal designers must adapt to less ideal CMOS devices.

CMOS Device Scaling

	0.25um	0.18um	0.13um
V_{dd} (volt)	2.5	1.8	1.3
G_m (ms/um)	0.3	0.4	0.6
R_o (kΩ•um)	130	66.7	24
G_mR_o	39	27	14
A_{vth} (mv•um)	7	5.5	4.5
A_β (%•um)	1.8	1.8	1.8
f_T (GHz)	30	60	80
Vth(v)	0.46	0.42	0.34
I_{off} (pA/um)	10	20	320

Microwave considerations for CMOS and SiGe BJTs

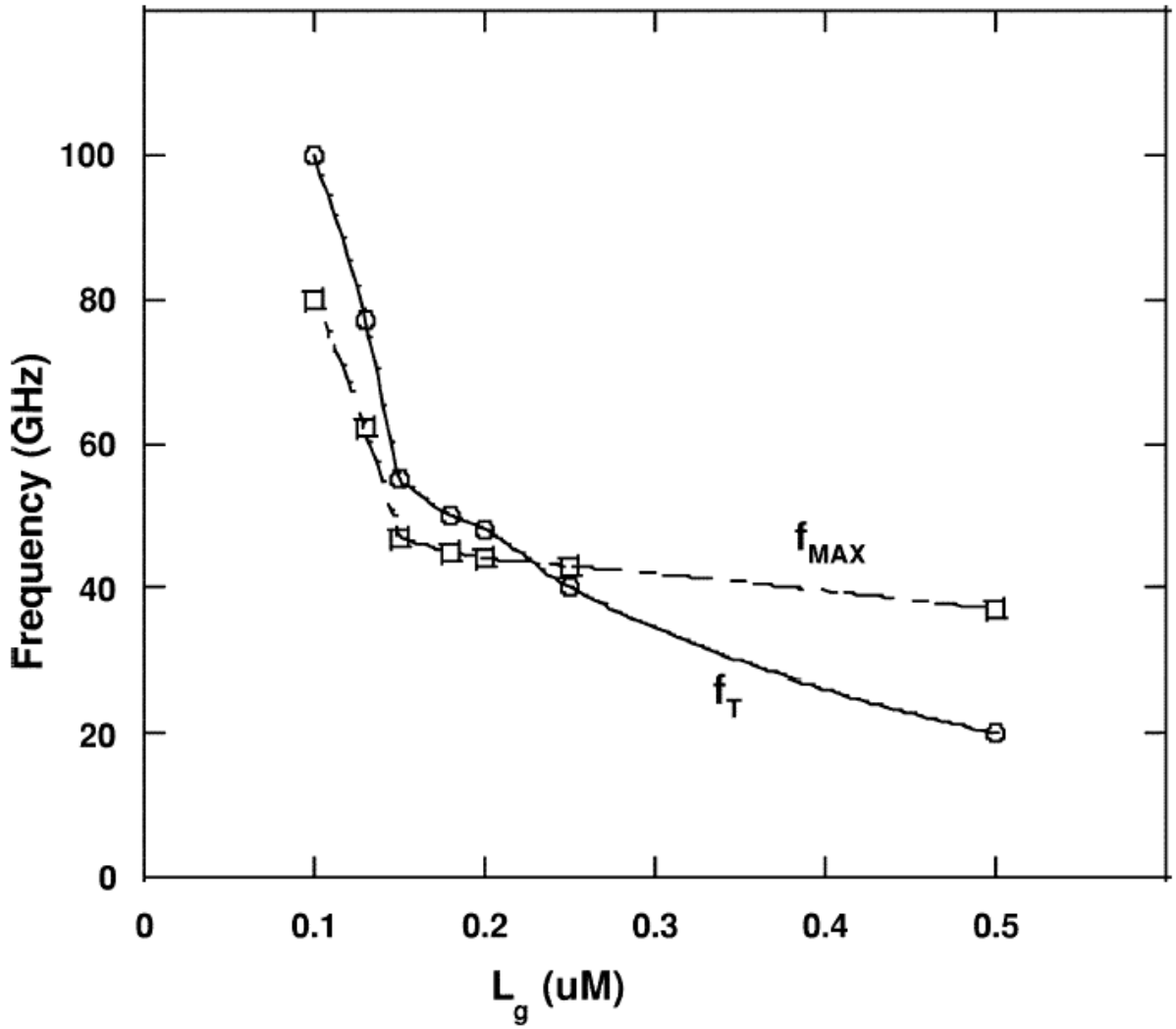


Fig. 6. MOSFET speed as a function of gate length [31]. The f_T and f_{MAX} demonstrate a clear gate length dependence. Note that the ratio of f_{MAX}/f_T decreases with decreasing gate length, demonstrating the increasing impact of parasitic gate resistance.

Larson, “Silicon Technology Tradeoffs for MS/RF SOC,” IEEE Trans Elect Dev., March 2003.

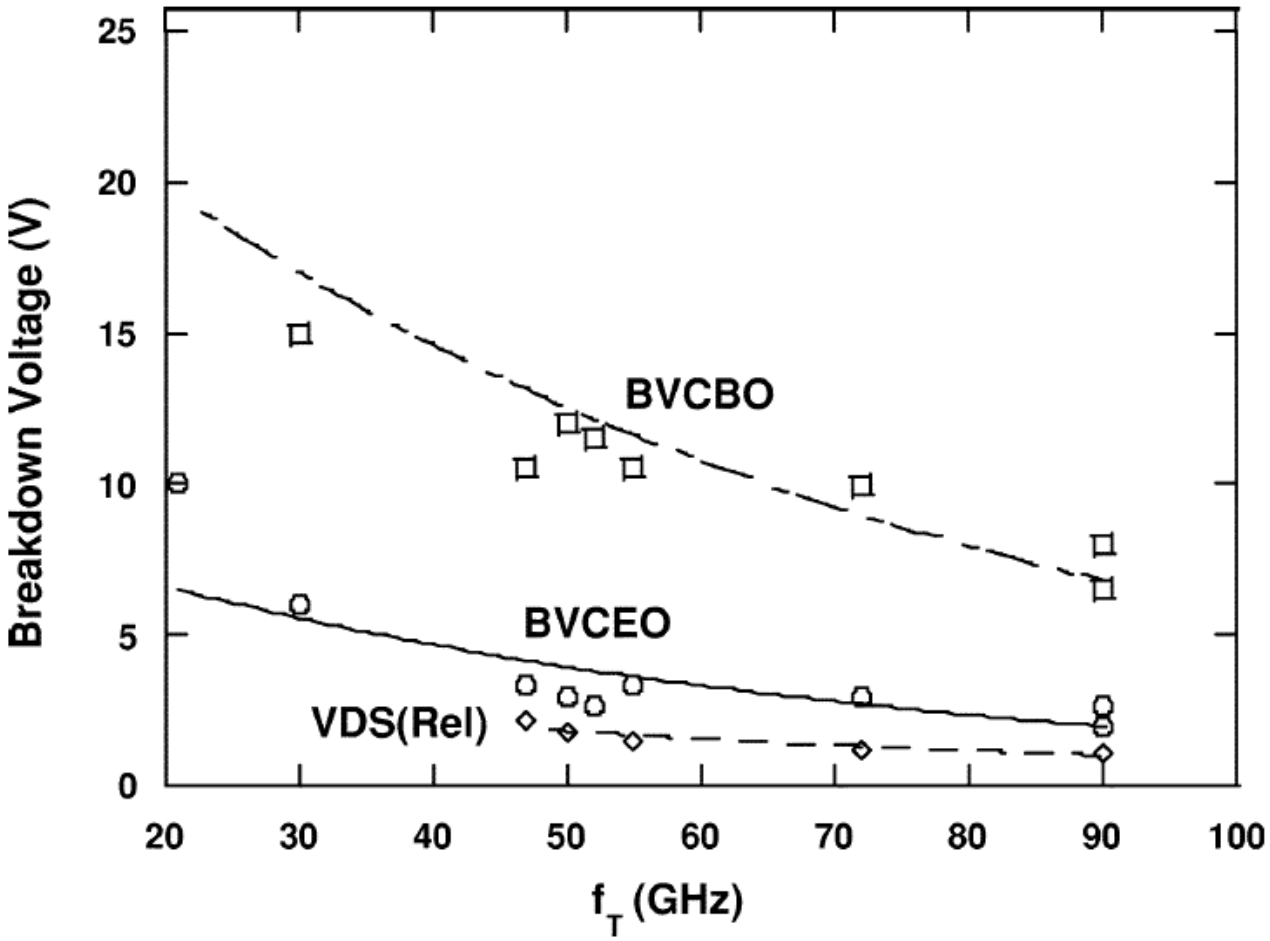


Fig. 7. Comparison of voltage limitations of MOSFETs and HBTs as a function of f_T [31], [35]. The VDS(Rel) of the MOSFET is the recommended operating voltage to minimize long-term degradation of the transistor. The Si/SiGe HBT BVCEO and BVCBO maintain a roughly 1 : 3 relationship from 20 to 90 GHz.

Larson, “Silicon Technology Tradeoffs for MS/RF SOC,” IEEE Trans Elect Dev., March 2003.

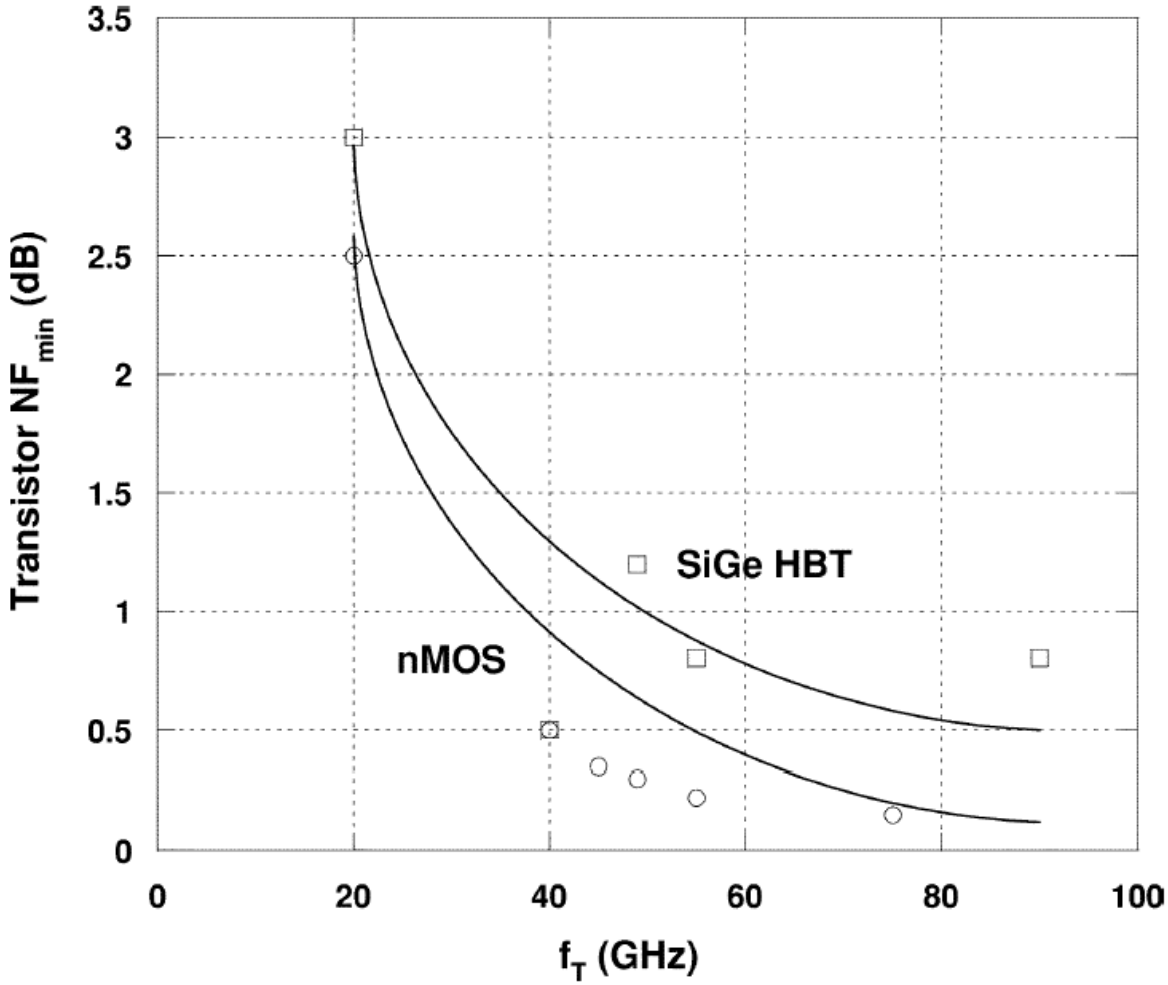
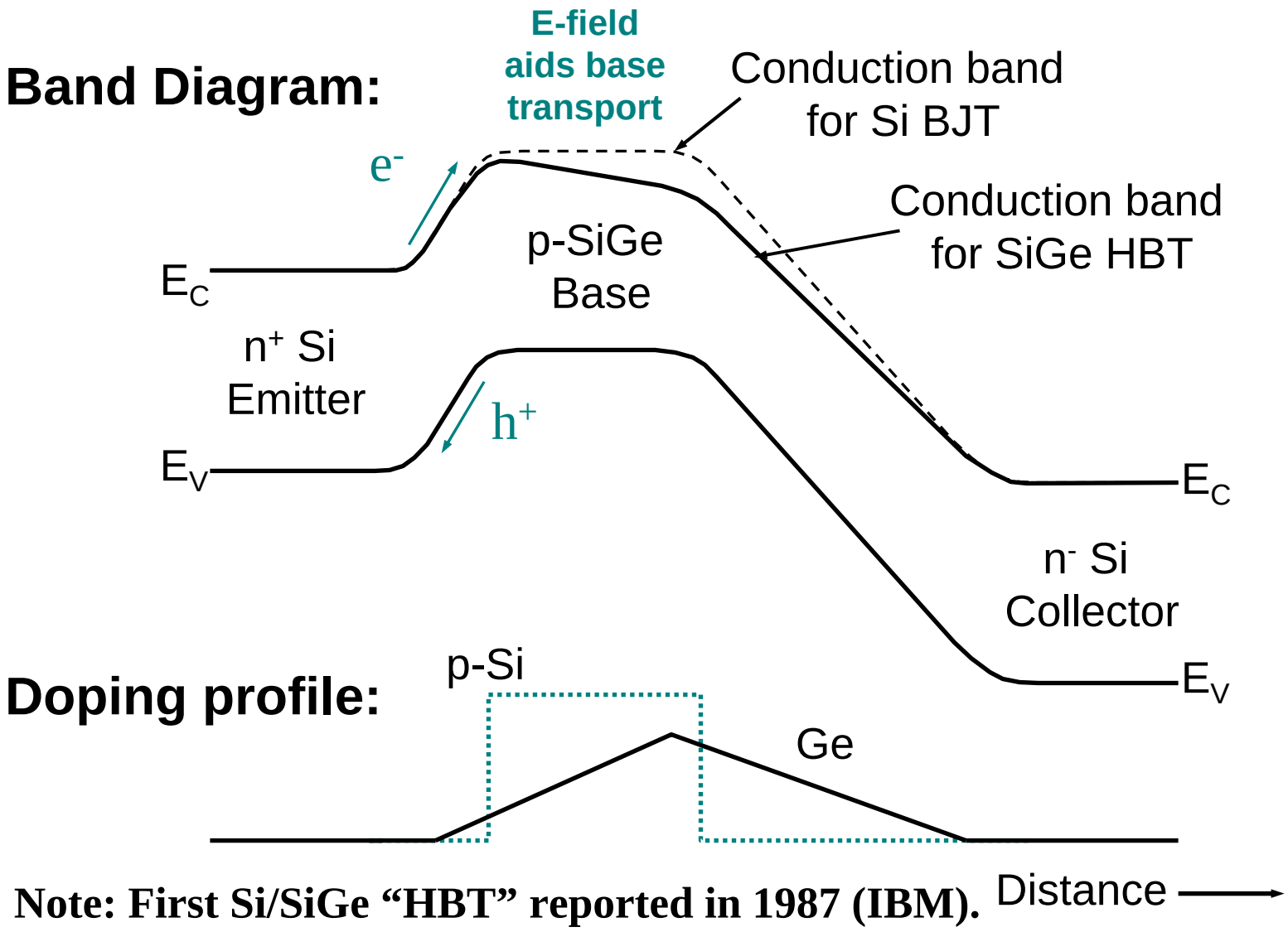


Fig. 12. Comparison of reported SiGe HBT and MOSFET minimum device noise figures as a function of peak f_T. For an equivalent intrinsic device speed, the MOSFET typically has an approximately 0.5-dB advantage, but this is difficult to realize in practice in a monolithic circuit due to the higher source impedance required.

Larson, “Silicon Technology Tradeoffs for MS/RF SOC,” IEEE Trans Elect Dev., March 2003.

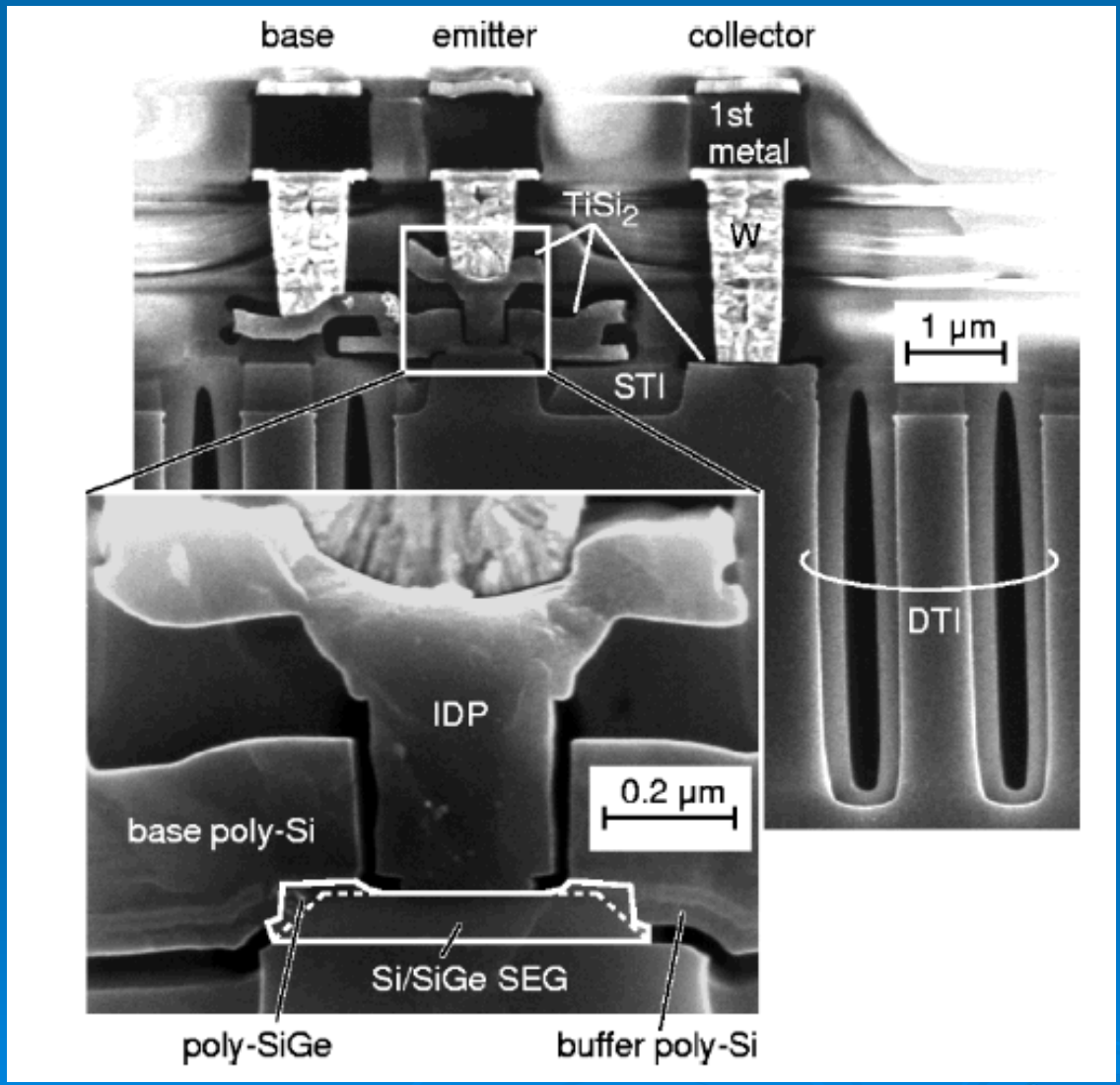
SiGe BiCMOS ICs

Band Structure: Si/SiGe "Heterojunction Bipolar Transistor"



Note: First Si/SiGe "HBT" reported in 1987 (IBM).

Self-aligned, selective epi SiGe HBT



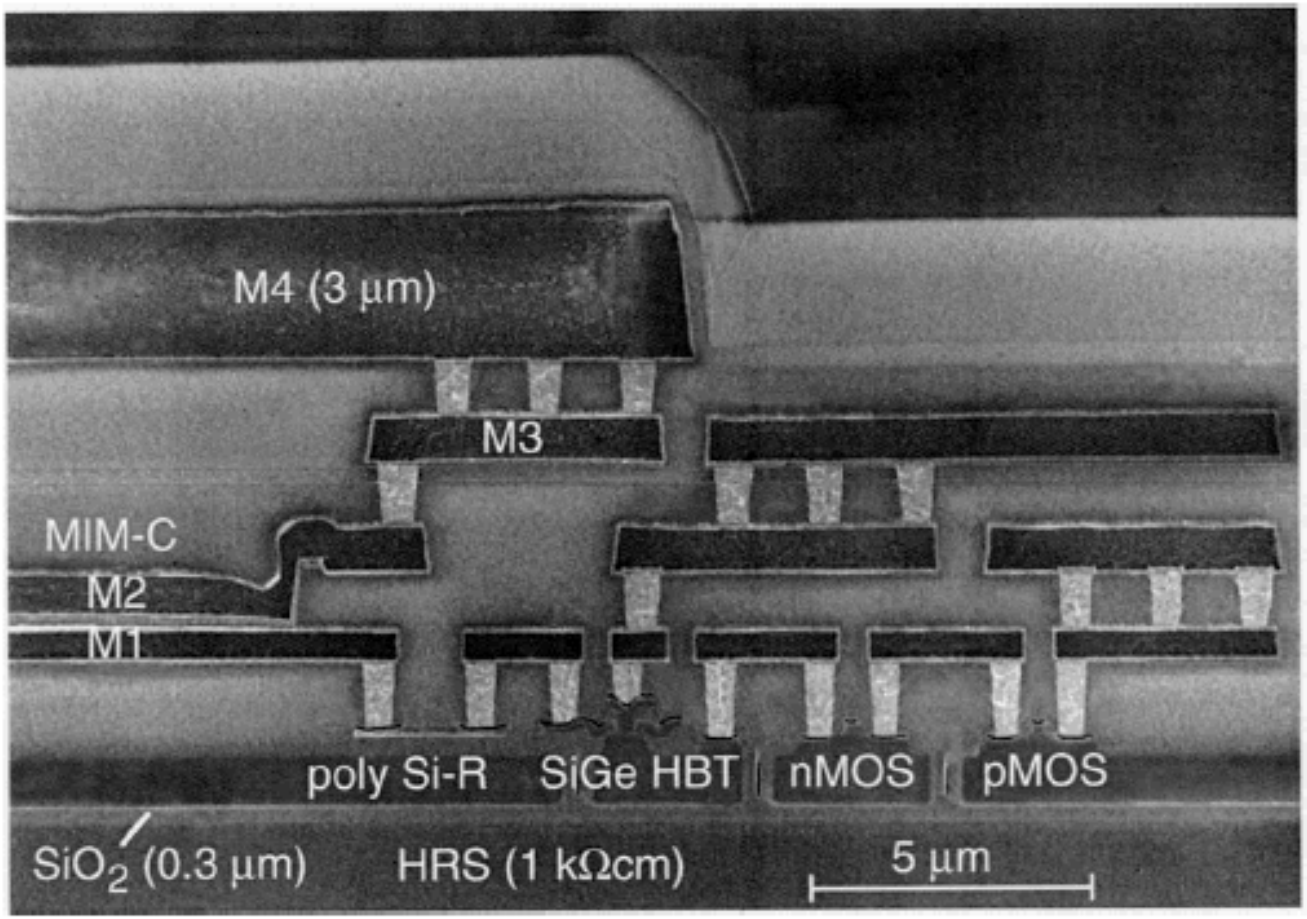
Fmax = 180 GHz
5.5 ps ECL delay

Deep trench isolation

SOI
Hi res substrate

K. Washio, SiGe HBT and BiCMOS Technologies for Optical Transmission and Wireless Communication Systems," IEEE Trans. On Elect. Dev., Vol. 50, #3, pp. 656-668, March 2003.

Wafer cross section



K. Washio, SiGe HBT and BiCMOS Technologies for Optical Transmission and Wireless Communication Systems," IEEE Trans. On Elect. Dev., Vol. 50, #3, pp. 656-668, March 2003.

F_T F_{max} vs I_C

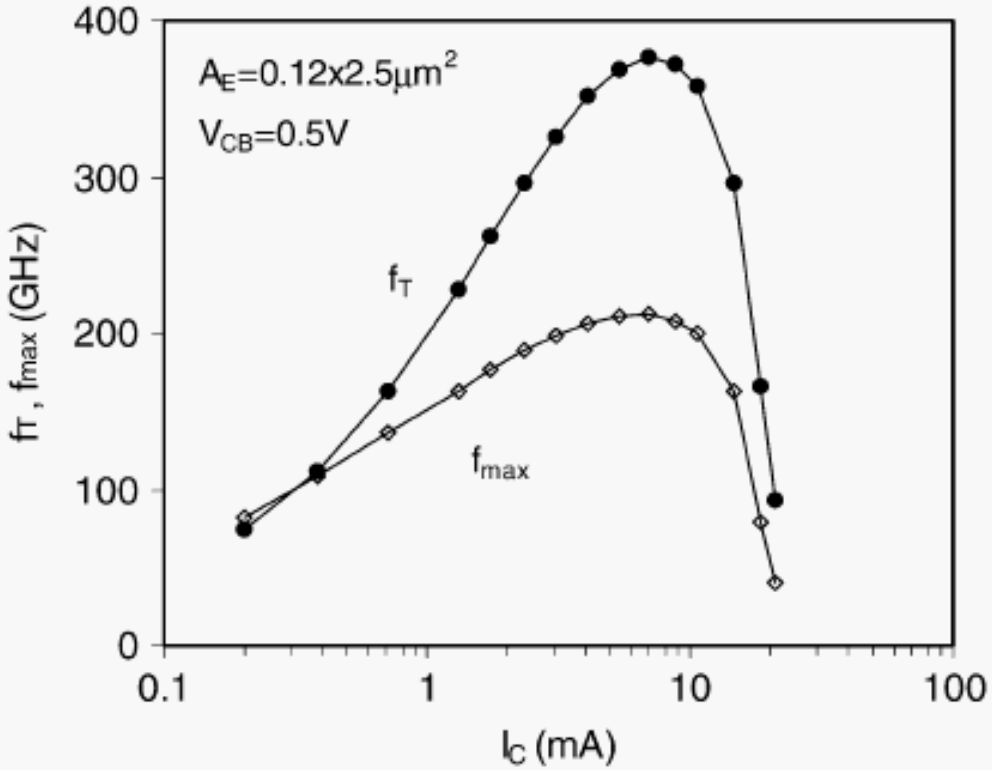


Fig. 4. f_T and f_{max} of the SiGe HBT extracted from h_{21} and U, respectively, from 40 GHz with -20 dB/dec rolloff. $T = 25$ °C.

J.S. Rieh, et al.,"SiGe Heterojunction Bipolar Transistors and Circuits Towards Terahertz Communication Applications," IEEE Trans. On Microwave Theory and Techn., Oct. 2004.

SiGe Generations

TABLE I

COMPARISON OF KEY PERFORMANCE PARAMETERS FOR SiGe TECHNOLOGIES FROM IBM. THE EXPERIMENTAL TECHNOLOGY (EXP. TECH.) IS UNDER DEVELOPMENT AND THE DATA THUS FAR ACHIEVED ARE LISTED

	5HP	6HP	7HP	8HP	Exp. Tech
Lithographic node [μm]	0.5	0.25	0.18	0.13	0.13
f_T [GHz]	47	47	120	210	375
f_{max} [GHz]	65	65	100	285	210
Beta	100	100	350	300	3500
BV_{CEO} [V]	3.4	3.4	1.8	1.7	1.4
BV_{CBO} [V]	10.5	10.5	6.5	5.5	5.0
J_C @$f_{T,peak}$ [mA/μm^2]	1.5	1.5	8	12	20

J.S. Rieh, et al.,"SiGe Heterojunction Bipolar Transistors and Circuits Towards Terahertz Communication Applications," IEEE Trans. On Microwave Theory and Techn., Oct. 2004.

References

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2. S. Long, D. Estreich, C. Chang, M. Venkataraman, “Compound Semiconductor Digital IC Technology,” Chap. 69, in VLSI Handbook, CRC Press, 2000.
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4. J. Rabaey, et al, Digital Integrated Circuits, 2nd Ed., Prentice-Hall, 2003.
5. International Technology Roadmap for Semiconductors, 2003 Edition, Executive Summary. public.itrs.net
6. International Technology Roadmap for Semiconductors, Update 2004, Lithography. public.itrs.net
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10. K. Washio, SiGe HBT and BiCMOS Technologies for Optical Transmission and Wireless Communication Systems,” IEEE Trans. On Elect. Dev., Vol. 50, #3, pp. 656-668, March 2003.
11. J.S. Rieh, et al.,”SiGe Heterojunction Bipolar Transistors and Circuits Towards Terahertz Communication Applications,” IEEE Trans. On Microwave Theory and Techn., Oct. 2004.