A High-Speed Sample-and-Hold Technique Using a Miller Hold Capacitance

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Abstract—**This paper introduces a circuit technique for increasing the precision of an open-loop sample-and-hold circuit without significantly reducing the sampling speed. With this technique, the sampling error resulting from input-dependent charge injection of the sampling switch is attenuated by sampling the input voltage onto a capacitance that is small during the sample mode but is, in effect, increased during the transition to the hold mode through the action of Miller feedback. The technique thus allows for a high sampling speed without the precision penalty traditionally associated with open-loop sample-and-hold circuits.**

A sample-and-hold circuit based on the proposed approach has been designed and fabricated in a 1-μm CMOS technology, and an order-of-magnitude reduction in the input-dependent charge injection has been demonstrated experimentally. This prototype circuit is capable of sampling an input to a precision of 8 b with an acquisition time of 5 ns. The experimental sample-and-hold circuit operates from a single 5-V supply and dissipates 26.5 mW.

I. Introduction

As DATA conversion systems continue to improve in speed and resolution, increasing demands are placed on the performance of high-speed sample-and-hold circuits. The throughput of the fastest analog-to-digital converters is typically limited by the speed and precision with which the comparison function can be performed. However, the maximum input signal bandwidth that can be accommodated by a converter at a specified precision is governed by the speed and precision at which the input can be sampled.

In the highest speed, moderate-resolution (8–10 b) fully parallel (flash) converters, the use of an input sample-and-hold circuit avoids sensitivity of the conversion to mismatches in clock distribution to the large number of comparators, mismatches in delay through comparator input stages, and RC delays in the input resistor ladder [1]–[3]. In multistep converter architectures, the need for an input sample-and-hold function is even more important because of the delays associated with quantizing the input in two or more stages. As yet, monolithic implementations of sample-and-hold systems that meet the stringent requirements for high-speed systems are complex in design and are usually fabricated in hybrid technologies.

In order to meet the stringent performance requirements for high-speed data acquisition in an economic monolithic implementation, a circuit technique has been devised to increase the resolution of an open-loop sample-and-hold circuit without the need for precise capacitors or an increase in capacitor size, which would result in a corresponding decrease in sampling rate. In this proposed approach the input is sampled onto an equivalent hold capacitance that is small during the sampling mode but is increased during the hold mode by means of Miller feedback. A sample-and-hold circuit based on the approach has been designed and fabricated in a 1-μm CMOS technology, and an order-of-magnitude reduction in the input-dependent charge injection of the sampling switch has been verified experimentally. The prototype circuit is capable of sampling a voltage input to a precision of 8 b within an acquisition time of 5 ns. The experimental sample-and-hold circuit operates from a single 5-V supply and uses clock signals that are buffered via on-chip inverters.

In Section II, several alternative sample-and-hold architectures are examined. The proposed sample-and-hold technique is then introduced in Section III. An analysis of the channel charge injection mechanism of MOS transistors during turn-off is also presented. Experimental results from a prototype implementation of the proposed sample-and-hold circuit are included in Section IV.

II. Sample-and-Hold Implementation

A. Architectures

Two basic circuit configurations commonly used to implement monolithic sample-and-hold circuits are the open-loop and closed-loop topologies shown in Figs. 1 and 2, respectively. The open-loop architecture potentially offers the fastest implementation of the sampling function [4]–[6]. In its simplest form, an open-loop sample-and-hold circuit consists of a switch, shown implemented with MOS pass transistor $M1$, which samples the input onto a hold capacitance C_{HOLD}. A high-input-impedance unity-gain amplifier buffers the hold capacitance and provides a low-impedance output node that drives the succeeding circuitry. During the sample mode, the sampling switch $M1$ is closed and the voltage across capacitor C_{HOLD} settles to the input voltage level. However, in the transition from the sample mode to the hold mode, the turn-off of the sampling switch results in charge injection effects that introduce a pedestal error ΔV_S at the output, as illustrated in Fig. 1. In designs where an MOS transistor functions as the sampling switch, input-dependent charge injection associated with the fast turn-off of the switch is often the principal source of sampling error [7]–[9]. This pedestal error results in gain error and introduces nonlinearity that distorts the sampled signal. Since the pedestal error

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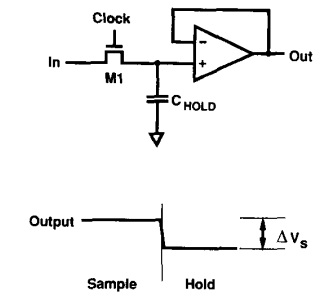

Fig. 1. Open-loop sample-and-hold architecture.

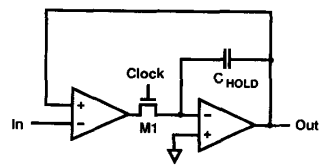

Fig. 2. Closed-loop sample-and-hold architecture.

is not well-controlled, it is difficult to compensate for this error using self-calibration techniques.

Several closed-loop architectures avoid input-dependent charge injection during turn-off of the sampling switch [6]. One such configuration is shown in Fig. 2. In this circuit, the sampling switch is always at virtual ground during sampling. This ensures that the charge injection and corresponding hold pedestal are independent of the input. However, the use of a closed-loop configuration entails a trade-off between speed and precision governed by the gain and bandwidth of the loop transfer function. Since the feedback loop in Fig. 2 encompasses two high-gain stages and an adequate phase margin is required for good settling characteristics, the operating bandwidth of this configuration may be low. Potential disadvantages of a closed-loop approach thus typically include long acquisition time, limited input bandwidth, and increased design complexity.

Open-loop architectures potentially provide the fastest possible sampling. However, even at modest resolutions, the performance of a monolithic open-loop circuit may be severely limited by the characteristics of an MOS sampling switch. In particular, pedestal error induced by charge injection in the switch is likely to limit the achievable precision.

B. MOS Charge Injection

Although an MOS transistor can serve as a zero-offset switch, and the high gate impedance of an MOS device makes charge storage on capacitors and analog pipelining possible, VLSI CMOS technologies are typically not well suited to implementing high-speed sample-and-hold circuits. MOS devices have high ON resistances, and the bandwidths of high-gain MOS operational amplifiers are limited. In addition, there is a substantial amount of signal-dependent charge injection associated with the fast turn-off of MOS switches.

To achieve the highest sampling rate and/or shortest acquisition time, an open-loop sample-and-hold configuration is desired. When the switch in such a configuration is implemented with an MOS transistor, sources of sampling error include inversion channel charge injection and capacitive coupling of the clock signal to the hold node via the gate-to-diffusion overlap capacitance.

The channel charge injection phenomenon has been modeled and characterized in studies that reveal a large linear input-dependent component of charge injection [7]–[9]. An additional nonlinear component, although expected to be small [8], is of increasing concern at high sampling speeds because of the large switch device sizes and small hold capacitances needed. Such nonlinearity directly affects the precision of the sampled data and results in harmonic distortion. The linear input-dependent component of injected channel charge can be accommodated in some applications, because its only effect on the sample-and-hold transfer function is a slight gain deviation from unity. However, even such gain deviation may not be tolerable in applications such as those that require low sensitivity of the sample-and-hold gain to temperature changes; the amount of MOS charge injection is temperature-dependent. The linear component of the injected charge is also a problem in applications where the gain matching between two or more sample-and-hold circuits is important, such as in time-interleaved converter arrays [5]; any mismatch between sampling transistors due to process nonidealities [10] will lead to a mismatch in the amount of linear input-dependent charge injection.

One solution to the problems arising from charge injection is to increase the transition time of the sampling clock since this will result in less input-dependent channel charge injection. However, a consequence of this approach is that the turn-off instant of the sampling switch becomes input dependent, and significant harmonic distortion is induced in the sampled output for wide bandwidth input signals. The net effect is to severely degrade sampling precision at high input frequencies. A more complete discussion of this effect and its implications is included in the Appendix.

High-speed sampling requires a large sampling switch for low switch ON resistance, a small hold capacitance, and a short clock transition time. These conditions make the pedestal error more pronounced. There is thus a basic trade-off between sampling speed and sampling precision. In the following section, a circuit technique is presented for improving this trade-off by reducing the effect of the charge injection of the input sampling switch without some of the drawbacks associated with alternative approaches.

III. Miller Capacitance Sample and Hold

A. Circuit Concept

The proposed sample-and-hold configuration, shown in Fig. 3, is functionally identical to the open-loop circuit of Fig. 1. It combines an input sampling switch $M1$ with a high input-impedance unity-gain buffer. In the circuit of Fig. 3, the equivalent hold capacitance is formed by a combination of capacitors C_1 and C_2, the MOS pass transistor $M2$, and an inverting amplifier with gain A. C_{1B} and C_{2B} represent the parasitic bottom-plate capacitances associated with C_1 and C_2, respectively.

When the circuit of Fig. 3 is in the sample mode, both $M1$ and $M2$ are conducting. The switch $M2$ bypasses the amplifier, and the bottom plates of both C_1 and C_2 are thus connected to the low amplifier output impedance. $M2$ also

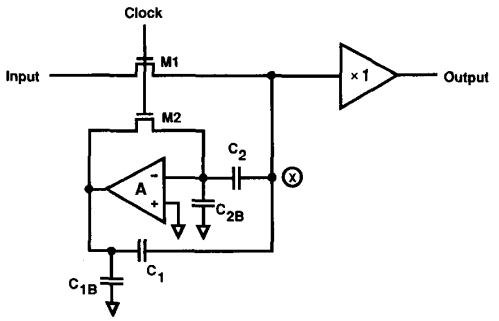

Fig. 3. Sample-and-hold circuit using a Miller hold capacitance.

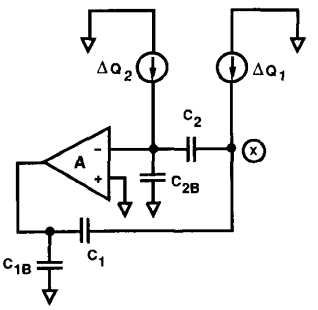

Fig. 4. Equivalent model of Miller-effect sample-and-hold circuit during transition to hold mode.

maintains the amplifier at the threshold point of its transfer characteristic, where the magnitude of its gain is A. With sampling switch $M1$ closed, the input voltage is sampled onto capacitors C_1 and C_2 at the hold node X.

During the transition from the sample mode to the hold mode, the rapid turn-off of transistors $M1$ and $M2$ results in the injection of channel charge and the capacitive coupling of the clock signal onto node X and the bottom plate of capacitor C_2. Since the drain and source of $M2$ are at the threshold point of the amplifier transfer function during the sample mode, the charge injected from its turn-off is essentially independent of the input. The drain and source of $M1$ are at the input potential during sampling; thus the charge injected during turn-off has a large input dependence and is a potential source of sampling error. If the coupling between the two switch transistors during turn-off is assumed to be minimal, then the charge injection and capacitive coupling can be modeled as two independent current source charge injections as shown in Fig. 4. In practice, the turn-off of one transistor does have a small effect on the turn-off behavior of the other. However, both simulations and experimental results indicate that this coupling is small and that the model of Fig. 4 is appropriate. Since the extent of this coupling limits the effectiveness of the approach, the effect is examined further in the following subsection.

Based on the circuit model of Fig. 3 it follows that, for sufficiently large values of the amplifier gain A, the change in voltage at node X due to the turn-off of $M2$ is

$$\Delta V_{S2} = \frac{\Delta Q_2}{C_2} \tag{1}$$

where ΔQ_2 is the net charge injected onto the bottom plate of C_2. Because $M2$ always settles to the threshold of the amplifier transfer characteristic during the sample mode, ΔQ_2 is a constant amount of charge independent of the level of the input. Consequently, ΔV_{S2} simply represents a fixed offset.

The charge injected during the turn-off of transistor $M1$ (ΔQ_1) causes a voltage change at node X given by

$$\Delta V_{S1} = \frac{\Delta Q_1(C_2 + C_{2B})}{C_{2B}(C_1 + C_2) + C_1C_2(A+1)} \tag{2}$$

where A is the gain of the inverting amplifier. It is apparent from this expression that the effect of charge injection from the sampling switch $M1$ at the hold node X has been attenuated by the action of Miller feedback. Furthermore, the equivalent hold capacitance in the hold mode is significantly increased by that feedback.

B. Coupling Between Switches

In theory, when the charge injection from each of the transistors $M1$ and $M2$ in Fig. 3 is assumed to be independent of each other, the pedestal error resulting from input-dependent charge injection is attenuated as indicated in (2). However, $M1$ and $M2$ are coupled by capacitance C_2, which causes the input-dependent turn-off transient of $M1$ to affect the charge injected by $M2$. This coupling results in a small input-dependent component of charge injection from the fast turn-off of $M2$, and the performance improvement that can actually be achieved is somewhat reduced from that predicted by (2). In this section, the extent of the coupling is analyzed.

In order to analytically determine the degree of coupling between $M1$ and $M2$ during turn-off, the behavior of a single transistor during turn-off is first analyzed. The simple configuration of a voltage source sampled by an MOS transistor onto a capacitor, as shown in Fig. 5(a), is considered. In most practical applications the channel transit time is much smaller than the clock transition time; thus, the MOS device can be modeled by an equivalent lumped circuit, as shown in Fig. 5(b), to determine the turn-off transients. The equivalent lumped circuit evenly divides the oxide capacitance between the gate and the drain and source nodes. The channel conductance is obtained from the usual current equations for an MOS transistor. The gate-to-diffusion overlap capacitances are not included in this analysis since they appear in parallel with the modeled oxide capacitances and are not significant. Furthermore, when the channel goes out of inversion, the purely capacitive coupling effects of these overlap capacitances are independent and can be considered separately. From Kirchoff's current law it follows for the circuit of Fig. 5(b) that

$$C_L \frac{dV_S}{dt} = -\beta(V_{HT} + Ut)V_S - \frac{C_{ox}U}{2} \tag{3}$$

where U is the gate voltage slew rate, $\beta = \mu C_{ox}W/L$ and $V_{HT} = V_H - V_L - V_T$, and where V_H is the high clock level, V_L is the low clock level, and V_T is the transistor threshold

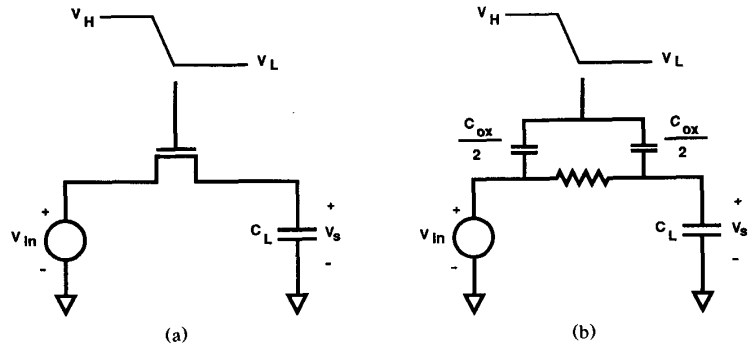

Fig. 5. (a) Single MOS transistor sampling a voltage onto a capacitor. (b) Simple lumped model during turn-off.

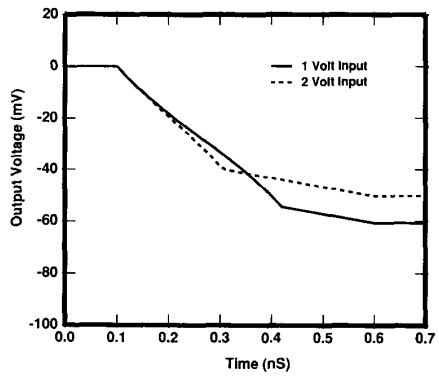

Fig. 6. Typical turn-off waveforms at hold capacitor node for circuit of Fig. 4 for input voltages of 1 and 2 V. DC biases have been subtracted.

voltage. The solution to (3) is

$$V_S(t) = -\sqrt{\frac{\pi U C_L}{2\beta}}\left[\frac{C_{ox}}{2C_L}\right]\exp\left[\frac{\beta U}{2C_L}\left(t-\frac{V_{HT}}{U}\right)^2\right] \cdot\left(\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\,V_{HT}\right] -\operatorname{erf}\left[\sqrt{\frac{\beta}{2UC_L}}\,(V_{HT}-Ut)\right]\right). \quad (4)$$

The error voltage V_{SF} at the point the channel goes out of inversion (i.e., pedestal error) is then

$$V_{SF} = -\left[\frac{C_{ox}}{2C_L}\right]\sqrt{\frac{\pi U C_L}{2\beta}}\operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_L}}\,V_{HT}\right). \quad (5)$$

When the circuit of Fig. 5(a) is simulated in SPICE, the voltage waveform at the hold capacitor node for a typical MOS transistor during turn-off takes on the behavior shown in Fig. 6. In this figure, the two waveforms show the output behavior for different input voltages. The dc bias is nulled out so as to show both waveforms on the same graph. The waveforms are seen to have essentially the same slope when the transistors are conducting. The main difference is that for the case of a 2-V input the switch device goes out of conduction before it does in the case of a 1-V input.

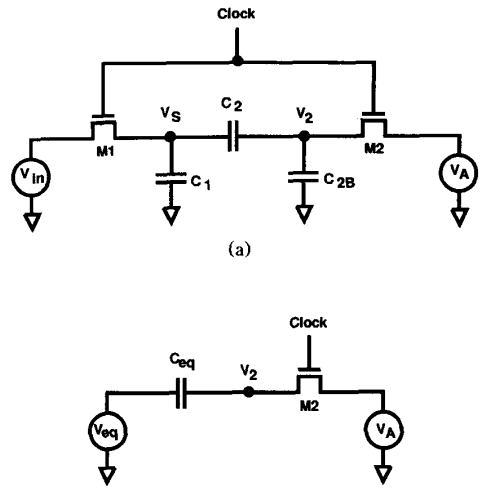

Fig. 7. Equivalent MOS switch configuration in proposed sample-and-hold circuit: (a) schematic and (b) model.

It is apparent from (1) and (2) that the charge injected by $M1$ is attenuated by the amplifier gain, but that the charge injected by $M2$ is not. Therefore, the following analysis focuses on the input dependence of the charge injection from the feedback transistor $M2$, which arises from the capacitive coupling of the turn-off transient of $M1$. The analysis is based on the results obtained above for a single MOS transistor.

Fig. 7 shows an equivalent circuit for modeling charge injection in the proposed sample-and-hold circuit. It consists of two MOS transistors $M1$ and $M2$ sampling onto capacitances C_1 and C_{2B}, with capacitive coupling provided by C_2. A differential equation describing the response of this circuit can easily be derived using the lumped MOSFET model of Fig. 5(b), but it is difficult to analyze. To facilitate the analysis, it is assumed that the form of the turn-off transient from $M1$ is known, and the response resulting from the turn-off of $M2$ is then derived. In particular, V_S is assumed to have a waveform similar to that of Fig. 6, and its response is approximated by a ramp function with a constant slope (i.e., $V_S(t) = U_2 t$, where U_2 is the slew rate of the expected

transient at the hold node). From (3), it follows that, for $V_S = 0$, the slew rate is given approximately by

$$U_2 = -\frac{C_{ox}U}{2C_{Leq}} \tag{6}$$

where $C_{Leq} = C_1 + (C_1C_{2B})/(C_1 + C_{2B})$.

Based on the waveform assumed for V_S, the circuit model during turn-off reduces to that shown in Fig. 5(b). The equivalent coupling capacitance and equivalent voltage source are

$$C_{eq} = C_{2B} + \frac{C_1C_2}{C_1 + C_2} \tag{7}$$

and

$$V_{eq} = U_2 t\left(\frac{C_2}{C_{2B} + C_2}\right). \tag{8}$$

If $M1$ is modeled with the lumped MOS model shown in Fig. 5(b), the differential equation describing the charge injection behavior is

$$C_{eq}\frac{dV_2}{dt} = -\beta(V_{HT} + Ut)V_2 - \frac{C_{ox}U}{2} - C_{eq}\frac{dVeq}{dt}. \tag{9}$$

Upon substituting (8) into (9) it follows that

$$C_{eq}\frac{dv_2}{dt} = -\beta(V_{HT} - Ut)v_2 - \left(\frac{C_{ox}}{2} + \frac{C_{eq}U_2}{U}\frac{C_2}{C_{2B}+C_2}\right)U. \tag{10}$$

The final pedestal error is thus

$$V_{2F} = -\left[\frac{C_{ox}}{2C_{eq}} + \frac{U_2}{U}\frac{C_2}{C_{2B}+C_2}\right] \cdot\sqrt{\frac{\pi UC_L}{2\beta}}\,\mathrm{erf}\left(\sqrt{\frac{\beta}{2UC_{eq}}}V_{HT}\right). \tag{11}$$

This error contains two components: 1) charge injection from the fast turn-off of $M2$, and 2) voltage change seen at V_2 due to capacitor division of voltage change at V_S.

If the turn-off of $M1$ did not affect the amount of charge injected by $M2$, the pedestal error would be

$$V_{2F'} = -\left[\frac{C_{ox}}{2C_{eq}}\right]\sqrt{\frac{\pi UC_L}{2\beta}} \cdot\mathrm{erf}\left(\sqrt{\frac{\beta}{2UC_{eq}}}V_{HT}\right) - \frac{U_2}{U}\frac{C_2}{C_{2B}+C_2}. \tag{12}$$

The difference between (11) and (12) is the component of the pedestal error caused by the change in the amount of charge injection of $M2$ due to the effect of the turn-off of $M1$; it is given by

$$V_{2F} - V_{2F'} = \frac{U_2}{U}\frac{C_2}{C_{2B}+C_2}\left[1 - \sqrt{\frac{\pi UC_L}{2\beta}} \cdot\mathrm{erf}\left(\sqrt{\frac{\beta}{2UC_{eq}}}V_{HT}\right)\right]. \tag{13}$$

When nominal parameter values are substituted in this expression, the total change in injected channel charge of $M2$ due to the transient caused by the turn-off of $M1$ is found to be approximately 7%. This value in itself does not reflect the input dependence of the charge injected by $M2$. The actual input dependence of this small change in injected channel charge is deduced to be minimal from the following observation. Fig. 6 shows that the voltage slew rate U_2 has only a weak input dependence, particularly at the beginning of the turn-off transition. The change in slope of voltage V_S occurs towards the end of the turn-off transition when the conductances of both transistors are significantly lower and, therefore, the coupling is greatly reduced.

Equation (13) shows that as the clock slew rate U increases, the total change in channel charge of $M2$ injected due to the transient caused by the turn-off of $M1$ approaches zero; the total charge injected by $M2$ will tend to 50% of the total channel charge of $M2$.

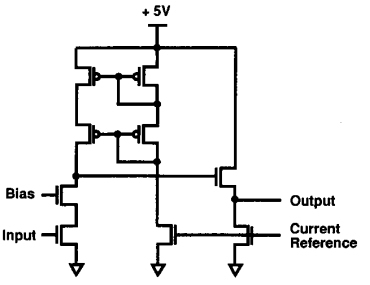

Fig. 8. Sample-and-hold Miller amplifier schematic.

C. Sample-and-Hold Circuit Design

In the Miller sample-and-hold circuit, the gain–bandwidth product of the amplifier is expected to be the principal limitation on acquisition time. Therefore a single-stage, moderate-gain amplifier is used to obtain the highest possible bandwidth. The Miller amplifier is a single-ended cascode stage with an output source follower, as shown in Fig. 8. It is designed to have a gain of 100. For the 1-μm CMOS technology in which the prototype circuit is integrated, the unity-gain bandwidth of this amplifier is greater than 1 GHz. Since second-order error terms (e.g., coupling between the two switches) are expected to govern the circuit's performance, a higher amplifier gain (and hence higher effective capacitance in the hold mode) will not contribute significantly to further reducing the input-dependent effects of charge injection from the sampling switch. Equation (2) indicates that the larger the value of C_1, the greater the attenuation of the input-dependent charge injection. C_2 adds directly to the hold capacitance in the sample mode and must be sized so that the loop gain attenuation by capacitor division at the input of the Miller amplifier does not significantly reduce the achievable precision. The effect of C_2 on reducing the coupling between $M1$ and $M2$ during turn-off must also be considered. In the prototype experimental implementation of the proposed sample-and-hold circuit, the capacitance values chosen were 0.7 pF for C_1 and 0.3 pF for C_2. The capacitors in this experimental design are metal to polycide and have a bottom-plate parasitic capacitance of approximately one third of the plate capacitance. The hold node capacitance is expected to be 1 pF during the sample mode and approxi-

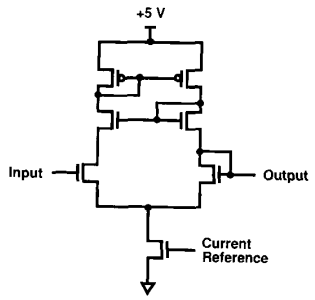

Fig. 9. Test unity-gain output buffer.

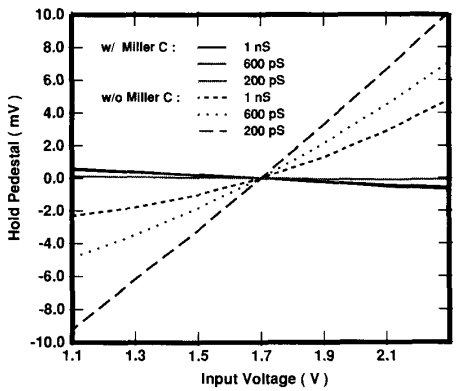

Fig. 10. Simulated hold pedestal versus input voltage level for varying clock slew rates.

mately 50 pF in the hold mode. The input sampling MOS switch has a drawn W/L ratio of 30 μm/1 μm.

The unity-gain buffer circuit designed for test purposes only is shown in Fig. 9. It has a linear range of 1 to 2.3 V. A precisely linear and accurate transfer function for this test buffer is not essential since the nonlinearity of this circuit can be compensated for in the experimental measurements.

Simulations of the Miller hold capacitance sample and hold were performed using SPICE, and a special effort was made to ensure charge conservation in the simulations. For comparison, the circuit of Fig. 1 was also simulated as a control case. For both circuits, the sampling switch dimensions were $W/L = 30$ μm/1 μm, and the hold capacitances were 1 pF during the sample mode. The effects of nonidealities in the unity-gain buffer were not included in the simulations, and only the voltage at hold node X was monitored. The clock signal swing was 5 V.

Since both sample-and-hold circuits have an ideal unity-gain transfer function during the sample mode owing to the inherent zero offset characteristic of the MOS switches, the hold pedestal is an accurate and sensitive indicator of the sample-and-hold transfer function. The simulated hold pedestal for the two sample-and-hold circuits is plotted in Fig. 10 as a function of the dc input voltage for varying clock transition times. In the Miller-feedback circuit, for a longer transition time there is more coupling between the turn-off of $M1$ and $M2$; thus, it is expected that the hold pedestal will depend more strongly on the input level. DC offsets are subtracted so as to show only the input dependence of the

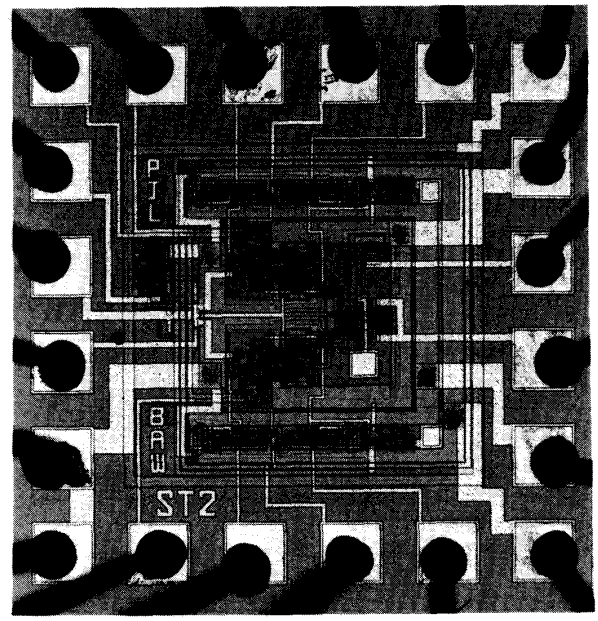

Fig. 11. Chip photograph.

pedestal. For the control case, without the Miller hold capacitance, and for a clock transition time of 1 ns, the hold pedestal is strongly dependent on the input level. For shorter clock transition times, this input dependence increases due to the increased amount of channel charge injection from the MOS switch $M1$. However, for the sample-and-hold circuit with the Miller hold capacitance, the input dependence of the hold pedestal is much reduced. Moreover, for shorter clock transition times, the input dependence decreases because coupling between $M1$ and $M2$ is reduced. For a clock transition time of 600 ps, the control case shows a 12-mV change in the hold pedestal for an input difference of 1 V, whereas the Miller-feedback sample-and-hold circuit shows only a 0.5-mV change. Thus, a more than an order-of-magnitude reduction in the effect of input-dependent charge injection from the fast turn-off of the sampling switch has been achieved.

One interesting point to note is that the slope of the hold pedestal as a function of input voltage is negative for the Miller sample-and-hold circuit. This phenomenon is a consequence of nonidealities in the circuit, particularly involving the coupling between $M1$ and $M2$ during turn-off. The rate of charge injection from the turn-off of $M1$ is lower for lower input voltages than for higher input voltages, and this has a small effect on the amount of charge injected from $M2$ during turn-off. This change in injected charge results in the negative slope of the dependence of the hold pedestal on the input level.

IV. Experimental Results

An integrated implementation of the proposed sample-and-hold circuit was designed and fabricated in a 1-μm CMOS technology [11]. A photograph of the experimental chip is shown in Fig. 11. The test chip contains two identical sample-and-hold circuits sharing a single unity-gain buffer,

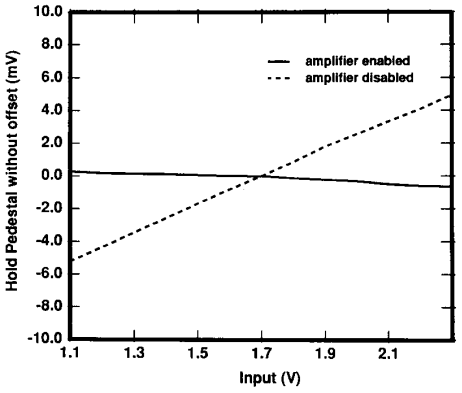

Fig. 12. Measured hold pedestal of sample-and-hold circuit as a function of the input voltage.

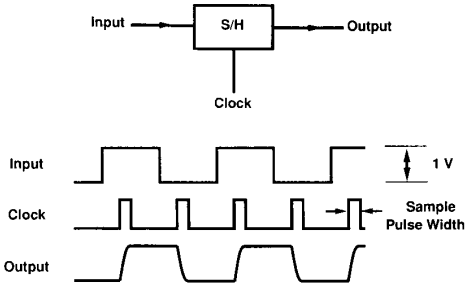

Fig. 13. Acquisition time test setup.

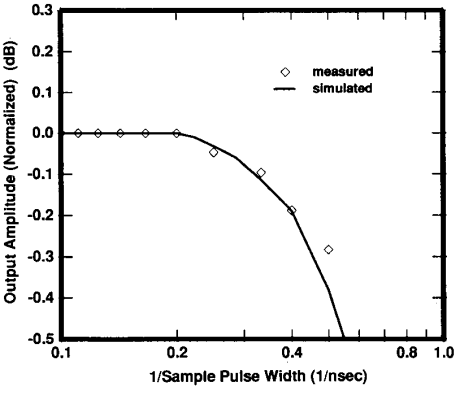

Fig. 14. Output attenuation versus 1/(acquisition time).

two separate clock drivers, and miscellaneous test and control circuitry. The clock transitions are generated on-chip by CMOS inverters with transition times of 0.4 ns.

The experimentally measured hold pedestal is plotted in Fig. 12 as a function of the dc input voltage. Two curves are shown—one for the hold pedestal obtained with the amplifier enabled and the other for the data collected with the amplifier disabled. For these measurements, the effect of the unity-gain buffer has been calibrated out so that the action of the Miller capacitance can be seen more clearly. A comparison of the two curves shows that the action of the Miller

Fig. 15. Input and output waveforms of sample-and-hold sampling 1-MHz full-scale (1-$V_{p\text{-}p}$) sinusoidal input at 10 MHz.

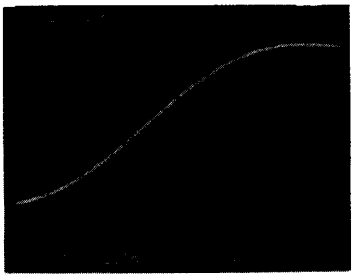

Fig. 16. Input and output waveforms of sample-and-hold sampling 10-MHz full-scale (1-$V_{p\text{-}p}$) sinusoidal input at 10.0625 MHz.

TABLE I

Technology	1-μm CMOS
Min. Acquisition Time for 8-b precision	5 ns
Input Capacitance during Sample Mode	1 pF
Full-Scale Input Range	1 V
Linearity	$\pm$0.1 mV
Power Supply	+5 V
Power Dissipation	
Miller Amplifier	6.5 mW
Unity-gain amplifier	20 mW
Total Power	26.5 mW

feedback in this circuit significantly reduces the total input dependence of the hold pedestal.

With a full-scale input voltage change of 1 V between two consecutive samples, the acquired output voltage levels were measured as the acquisition pulse width was varied. The test setup is shown in Fig. 13. The output level attenuation is shown as a function of the reciprocal of the acquisition pulse width in Fig. 14 along with the simulated behavior. Based on the data represented by Fig. 14, the sample-and-hold circuit is seen to be capable of sampling at a resolution of 8 b, for a full scale 1-V input change between consecutive acquisitions, with a minimum acquisition pulse width of 5 ns. The maximum sampling frequency was limited in the experimental sample-and-hold circuit by the speed of the unity-gain buffer, which was not designed for high-speed operation when driving off-chip capacitances. However, the buffer's performance does not affect the acquisition time.

Typical waveforms of the sample-and-hold circuit in operation are presented in Figs. 15 and 16. Fig. 15 shows the input and output waveforms when sampling a 1-MHz, 1-$V_{p\text{-}p}$

sinusoidal input at a sampling rate of 10 MHz. Results from a beat frequency test are shown in Fig. 16. A 10-MHz, 1-$V_{p\text{-}p}$ sinusoidal input was sampled at a rate of 10.0625 MHz.

The performance of the experimental sample-and-hold circuit is summarized in Table I.

V. Conclusions

A high-speed technique for increasing the precision of an open-loop sample-and-hold circuit without significantly reducing the sampling speed by using a Miller hold capacitance has been introduced. This technique has been found to be effective in a prototype sample-and-hold circuit fabricated in a 1-μm CMOS technology. A more than an order-of-magnitude reduction in the effect of the input-dependent charge injection from the fast turn-off of the sampling switch has been demonstrated. The experimental sample-and-hold circuit is capable of sampling at a resolution of 8 b with a minimum acquisition time of 5 ns.

Applications of this sampling technique to technologies other than VLSI CMOS are possible. Also, extension of the technique to a differential configuration so as to exploit its advantages is both feasible and straightforward.

Appendix

In open-loop sample-and-hold circuits using input sampling switches with clock signals that are not bootstrapped to the input, the finite slew rate of the clock transition creates an input-level-dependent sampling instant that gives rise to harmonic distortion of the sampled waveform. Consider the circuit configuration of Fig. 1 where the input sampling device is a single MOS transistor operated with a 5-V clock. The input MOS device switches off when the gate-to-source/drain voltage reaches the threshold voltage. Fig. 17 shows the gate voltage and the clock falling transitions. For the purposes of this analysis, the MOS transistor threshold voltage is assumed to be zero. The periodic clock has an amplitude of V_{CL} and a transition time t_{TR}. Since the threshold voltage is assumed to be zero, the sampling point in time t_S is defined as the instant that the falling clock transition reaches V_{AV}. If the input signal at time t_S were equal to V_{AV}, the actual sample would be taken at that time. However, if the input is not equal to V_{AV}, the finite slew rate of the falling transition causes the input to be sampled at time $t_{S'}$. Thus the sampling instant is dependent on the input level. Reconstruction of the sampled points shows a sinusoidal waveform with harmonic distortion. For a sinusoidal input given as $V_{\text{in}} = A \sin 2\pi ft$, the reconstructed output waveform is approximately

$$V_{\text{out}} = A \sin 2\pi f\left(t - \frac{A}{V_{CL}} * t_{TR} * \sin 2\pi ft\right). \quad (14)$$

To determine the signal-to-distortion ratio (SDR) degradation due to the input dependence of the sampling input, MIDAS, a general-purpose simulator for mixed analog and digital sampled-data systems [12], was used. The SDR for a sinusoidal input signal sampled by a MOS switch and capacitor circuit of Fig. 1 is dependent on a dimensionless composite parameter E given by the expression

$$E = \frac{A}{V_{CL}} * t_{TR} * f \quad (15)$$

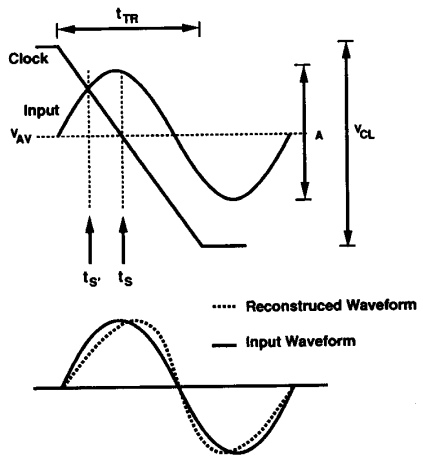

Fig. 17. Input-dependent sampling instant.

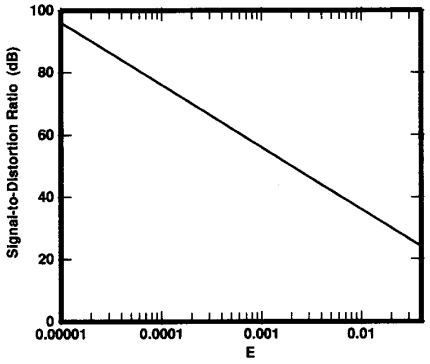

Fig. 18. Signal-to-distortion (SDR) as a function of composite variable E.

where A is the input sinusoidal amplitude, V_{CL} is the clock amplitude, f is the input frequency, and t_{TR} is the clock transition time. E gives an indication of the ratio of the relative slew rate of the sinusoidal input to that of the clock. An empirical relationship between the SDR and the composite variable E derived from simulation results is

$$\text{SDR(dB)} = 20 \log_{10}\left(\frac{1}{E}\right) - 4. \quad (16)$$

This relationship is plotted in Fig. 18.

For the sample-and-hold circuit presented in this paper, the appropriate parameters are: $A = 1$ V, $V_{CL} = 5$ V, and $t_{TR} = 0.4$ ns. The quantization noise in an ideal 8-b analog-to-digital converter results in a maximum SNR of approximately 50 dB. In order that the SDR of the sample-and-hold circuit be 6 dB above the quantization noise, the input signal frequency is limited to 12.5 MHz.

Although the closed-loop configuration of Fig. 2 does not suffer from the distortion that results from a sample instant that is dependent on the input level, its typically lower bandwidth can severely limit performance in many system applications. The low bandwidth results in significant amounts of frequency-dependent gain rolloff and delay, limiting the precision with which broad-band input waveforms can be sampled.

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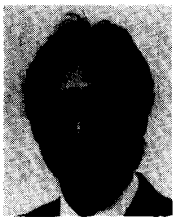

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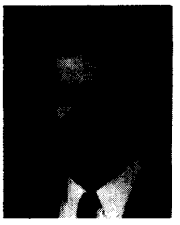

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