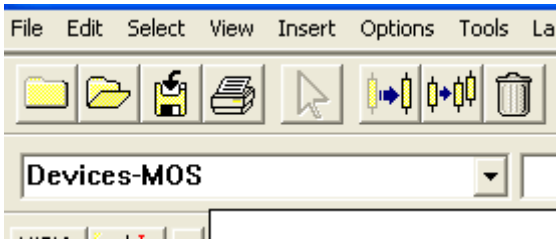
Setting up MOSFET Parameters for ADS simulation.

1. Using a MOS device in ADS requires that both the model and devices are included on the circuit schematic. Models for 0.18 um NMOS and PMOS devices were obtained from the MOSIS website (www.mosis.org) and imported into ADS. This can easily be done from the ADS Main Menu if the HSPICE formatted parameters on the MOSIS measurement files are saved as a text file. Open up a project then

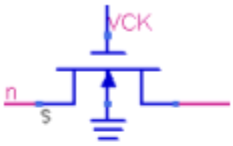
- File > Import
- Browse to find the file.
- More Options: identify the type of format (HSPICE) and indicate whether the first line is a comment.

Anyway, this has already been done, and you can obtain models for the NMOS and PMOS devices (cmosn018 and cmosp018) from an archived ADS file CT.zap found on the course web page. Copy these model icons and place them on your schematic.

2. Next, scroll down on the palette selector and use the Devices – MOS menu. Select the MOSFET_NMOS or MOSFET_PMOS device to place on your schematic.



- MOSFET1 This is the instance name. Can be whatever you want to call it. Each device requires a unique name.
- Model=cmosn018 (must agree with device model)
- Length= 1.8e-7 (gate length - nonadjustable; model does not scale)
- Width (channel width. W1 is defined in a VAR statement. Dimensions are in meters)
- Ad, As: area of source and drain. I assumed the contact length was 2 lambda.
- Pd, Ps: perimeter of source and drain. Same assumption.
- Temp: this defaults to 27C
- Trise: increase in temperature above Temp
- Mode=nonlinear. Default. Why else would you use this model?
- Noise: includes model for channel noise – useful in noise figure simulations.
- _M= Multiplication factor.



MOSFET_NMOS
MOSFET1
Model=cmosn018
Length=1.8e-7
Width=W1
Ad=W1*3.6e-7
As=W1*3.6e-7
Pd=W1+7.2e-7
Ps=W1+7.2e-7
Temp=
Trise=
Mode=nonlinear
Noise=yes
_M=

- The area and perimeter must be specified to produce the correct area and sidewall capacitances.
- The multiplication factor should be used whenever a large device is required. The actual performance at high frequencies will be quite different for one mosfet with a very long gate and one with the same total length but consisting of multiple instances of the device connected in parallel. The reason is that a long, very narrow gate behaves as a distributed RC line. Thus, there will be a phase shift or delay from one end of the gate to the other. This will degrade the performance of the device significantly.