

Phase Locked Loop Circuits

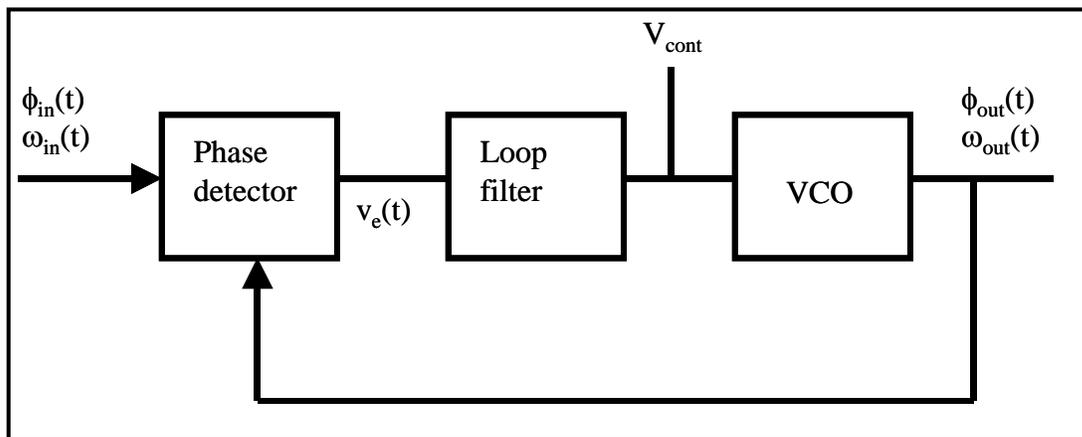
Reading: General PLL Description: T. H. Lee, Chap. 15. Gray and Meyer, 10.4
Clock generation: B. Razavi, *Design of Analog CMOS Integrated Circuits*, Chap. 15, McGraw-Hill, 2001.

1. **Definition.** A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

$$\phi_{out}(t) = \phi_{in}(t) + const.$$

$$\omega_{out}(t) = \omega_{in}(t)$$

The PLL output can be taken from either V_{cont} , the filtered (almost DC) VCO control voltage, or from the output of the VCO depending on the application. The former provides a baseband output that tracks the phase variation at the input. The VCO output can be used as a local oscillator or to generate a clock signal for a digital system. Either phase or frequency can be used as the input or output variables.



Of course, phase and frequency are interrelated by:

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t') dt'$$

Applications: There are many applications for the PLL, but we will study:

- Clock generation
- Frequency synthesizer
- Clock recovery in a serial data link

You should note that there will be different design criteria for each case, but you can still use the same basic loop topology and analysis methods.

2. Phase detector: compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs. K_D is the gain of the phase detector (V/rad).

$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

As one familiar circuit example, an analog multiplier or mixer can be used as a phase detector. Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$. If,

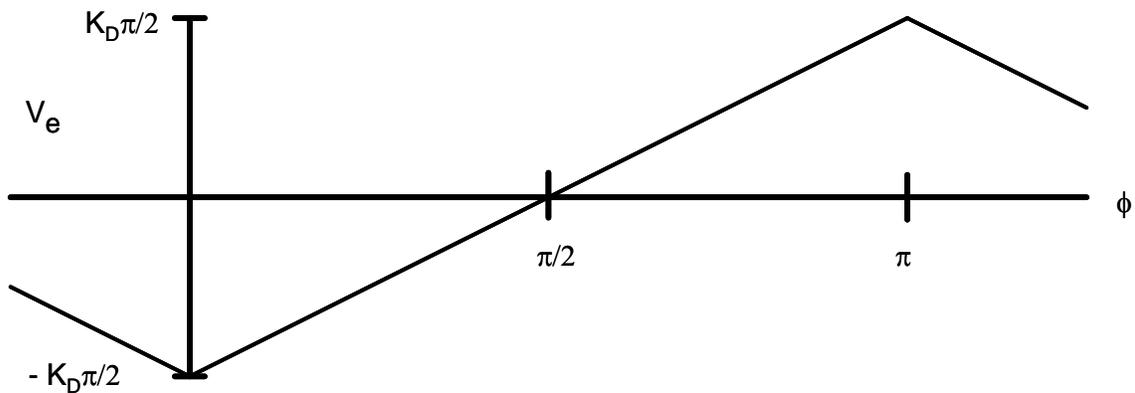
$$A(t) = A \cos(\omega_0 t + \phi_A)$$

$$B(t) = B \cos(\omega_0 t + \phi_B)$$

$$\text{Then, } A(t)B(t) = (AB/2)[\cos(2\omega_0 t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)]$$

Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The doubled frequency component must be removed by the lowpass loop filter. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

The averaged transfer characteristic of such a phase detector is shown below. Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).



If the phase difference is $\pi/2$, then the average or integrated output from the XOR-type phase detector will be zero (or $V_{DD}/2$ for single supply, digital XOR). The slope of the characteristic in either case is K_D .

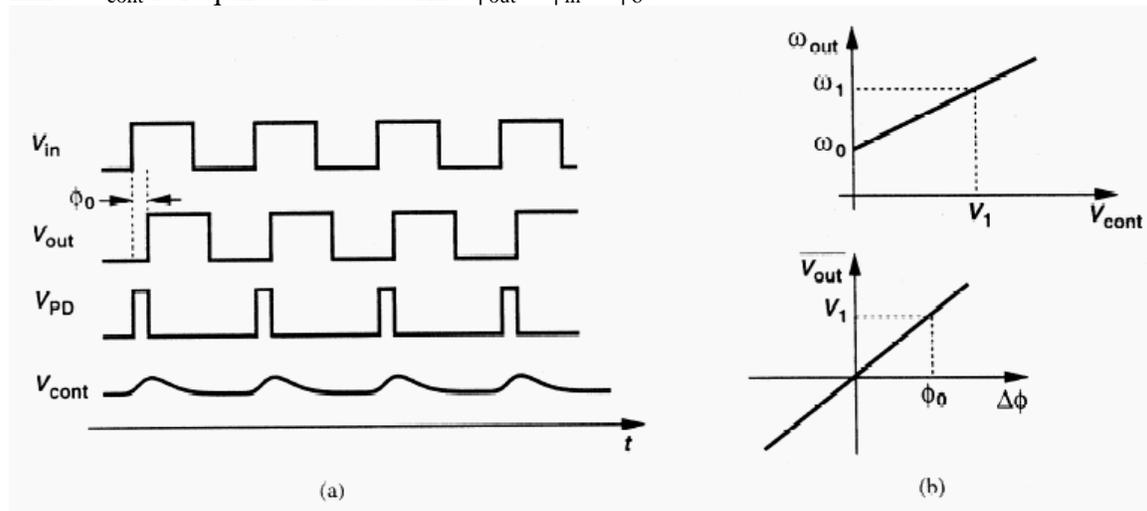
3. VCO. In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.

$$\phi_{out} = K_O \int_{-\infty}^t V_{cont} dt'$$

The VCO oscillates at an angular frequency, ω_{out} . Its frequency is set to a nominal ω_0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient K_O or K_{VCO} (rad/s/v).

$$\omega_{out} = \omega_0 + K_O V_{cont}$$

Thus, to obtain an arbitrary output frequency (within the VCO tuning range, of course), a finite V_{cont} is required. Let's define $\phi_{out} - \phi_{in} = \phi_0$.



(Figure from B. Razavi, Ch. 15, op. cit.)

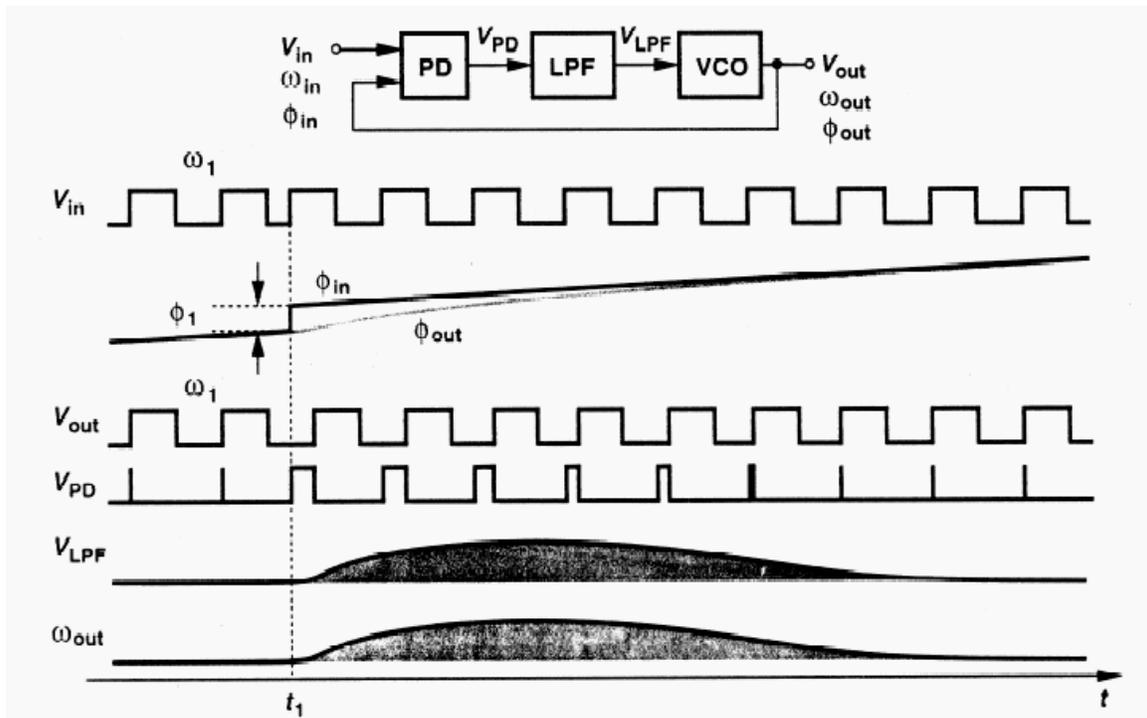
In the figure above, the two inputs to the phase detector are depicted as square waves. The XOR function produces an output pulse whenever there is a phase misalignment. Suppose that an output frequency ω_1 is needed. From the upper right figure, we see that a control voltage V_1 will be necessary to produce this output frequency. The phase detector can produce this V_1 only by maintaining a phase offset ϕ_0 at its input. In order to minimize the required phase offset or error, the PLL loop gain, $K_D K_O$, should be maximized, since

$$\phi_0 = \frac{V_1}{K_D} = \frac{\omega_1 - \omega_0}{K_D K_O}$$

Thus, a high loop gain is beneficial for reducing phase errors.

4. PLL dynamic response: To see how the PLL works, suppose that we introduce a phase step at the input at $t = t_1$.

$$\phi_{in} = \omega_1 t + \phi_0 + \phi_1 u(t - t_1)$$



(Figure from B. Razavi, Ch. 15, op. cit.)

Since we have a step in phase, it is clear that the initial and final frequencies must be identical: ω_1 . But, a temporary change in frequency is necessary to shift the phase by ϕ_1 . The area under ω_{out} gives the additional phase because V_{cont} is proportional to frequency.

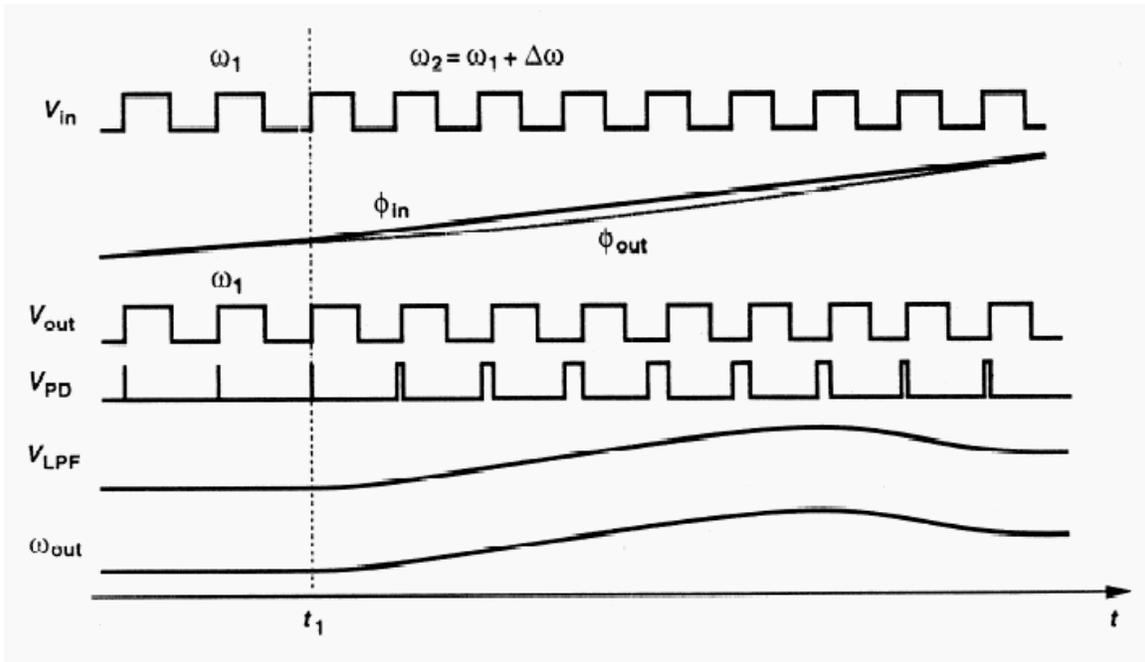
$$\phi_1 = \int_{t_1}^{\infty} \omega_{out} dt = \int_{t_1}^{\infty} K_O V_{cont}(t) dt$$

After settling, all parameters are as before since the initial and final frequencies are the same. This shows that $V_{cont}(t)$ [shown as $V_{LPF}(t)$ in the figure above] can be used to monitor the dynamic phase response of the PLL.

Now, let's investigate the behavior during a frequency step:

$$\omega_2 = \omega_1 + \Delta\omega$$

The frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp. This in turn causes the control voltage, V_{cont} , to increase, moving the VCO frequency up to catch up with the input reference signal. In this case, we have a permanent change in ω_{out} since a higher V_{cont} is required to sustain a higher ω_{out} .

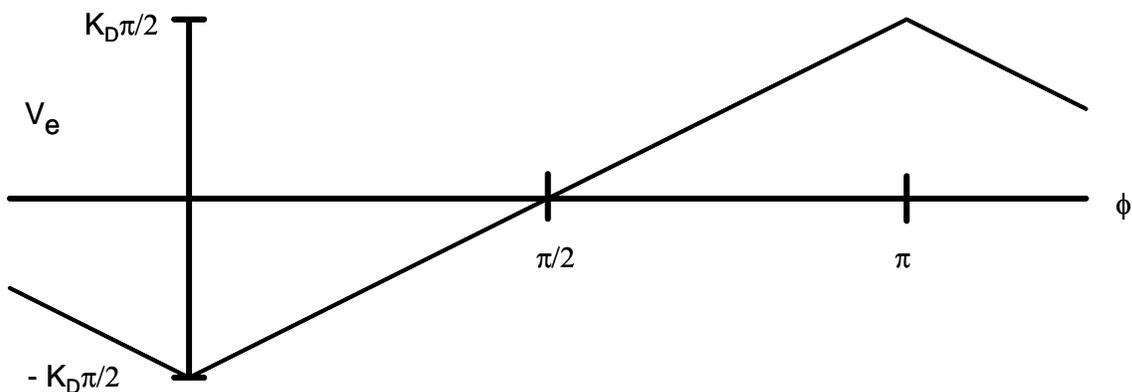


(Figure from B. Razavi, Ch. 15, op. cit.)

If the frequency step is too large, the PLL will lose lock.

5. Lock Range. Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

a. If limited by phase detector:



$0 < \phi < \pi$ is the active range where lock can be maintained. For the phase detector type shown (Gilbert multiplier or mixer), the voltage vs. phase slope reverses outside this range. Thus the frequency would change in the opposite direction to that required to maintain the locked condition.

$$V_{e-\max} = \pm K_D \pi/2$$

When the phase detector output voltage is applied through the loop filter to the VCO,

$$\Delta\omega_{\text{out-max}} = \pm K_V \pi/2 = \omega_L \text{ (lock range)}$$

where $K_V = K_O K_D$, the product of the phase detector and VCO gains.

This is the frequency range around the free running frequency that the loop can track.

Doesn't depend on the loop filter

Does depend on DC loop gain

b. The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is finite. In many cases, the VCO can set the maximum lock range.

6. Capture range: Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

You will see later that the loop filter bandwidth has an effect on the capture range.

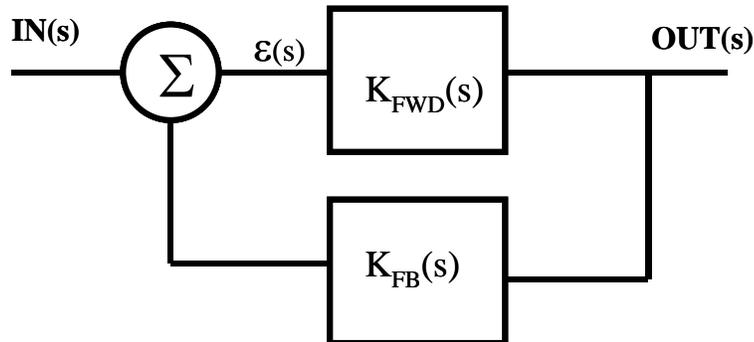
7. Approach: We will discuss the details of phase detectors and loop filters as we proceed. But, at this point, we will treat the PLL as a linear feedback system. We assume that it is already “locked” to the reference signal, and examine how the output varies with the loop transfer function and input. A frequency domain approach will be used, specifically describing transfer functions in the s-domain.

$$V_e(s)/\Delta\phi = K_D$$

$$\phi_{\text{out}}(s)/V_{\text{cont}}(s) = K_O/s$$

Note that the VCO performs an integration of the control voltage and thus provides a factor of $1/s$ in the loop transfer function. Because of this, a PLL is always at least a first order feedback system.

PLL is a feedback system



Loop Gain: $T(s) = K_{FWD}(s) K_{FB}(s)$

Transfer Function: $\frac{OUT(s)}{IN(s)} = H(s) = \frac{K_{FWD}(s)}{1 + T(s)}$

The Loop gain can be described as a polynomial:

$$T(s) = \frac{K' (s + a)(s + b) \cdots}{s^n (s + \alpha)(s + \beta) \cdots}$$

ORDER = the order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

PHASE ERROR = $\varepsilon(s) = \frac{IN(s)}{1 + T(s)}$

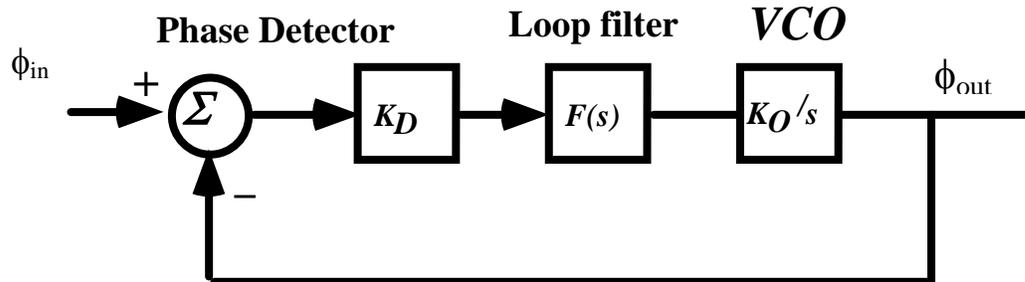
STEADY STATE ERROR = $\varepsilon_{SS} = \lim_{s \rightarrow 0} [s\varepsilon(s)] = \lim_{t \rightarrow \infty} \varepsilon(t)$

(this is the Laplace Transform final value theorem)

SS error is a characteristic of feedback control systems. This is the error remaining in the loop at the phase detector output after all transients have died out. Once again, you can see that a large loop gain $T(s)$ leads to a small phase error.

Frequency and phase tracking loop:

First we will consider the PLL with feedback = 1; therefore, input and output frequencies are identical. The input and output phase should track one another, but there may be a fixed offset depending on the phase detector implementation.



Transfer Function: $H(s) = \text{forward path gain} / [1 + T(s)]$.

With feedback = 1,

$$H(s) = T(s)/[1 + T(s)]$$

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s) / s}{1 + K_D K_O F(s) / s}$$

Phase error function:

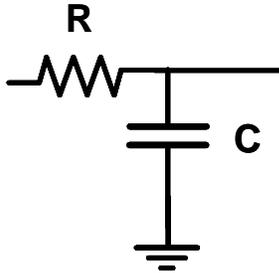
$$\varepsilon_s = \phi_{in} - \phi_{out} = \frac{s\phi_{in}}{s + K_D K_O F(s)}$$

For the frequency synthesis application, we want to have ideally perfect phase tracking for phase and frequency steps. When the synthesizer frequency is changed, it is a discontinuous step in modulus, and we want to have zero steady state phase error in this case.

We will start from the open loop gain, $T(s)$.

$$T(s) = K_D F(s) K_O / s$$

We know that the phase detector will be producing an output equal to or at twice the carrier frequency, thus some low pass filtering will be needed. Let's start with a simple RC lowpass network.



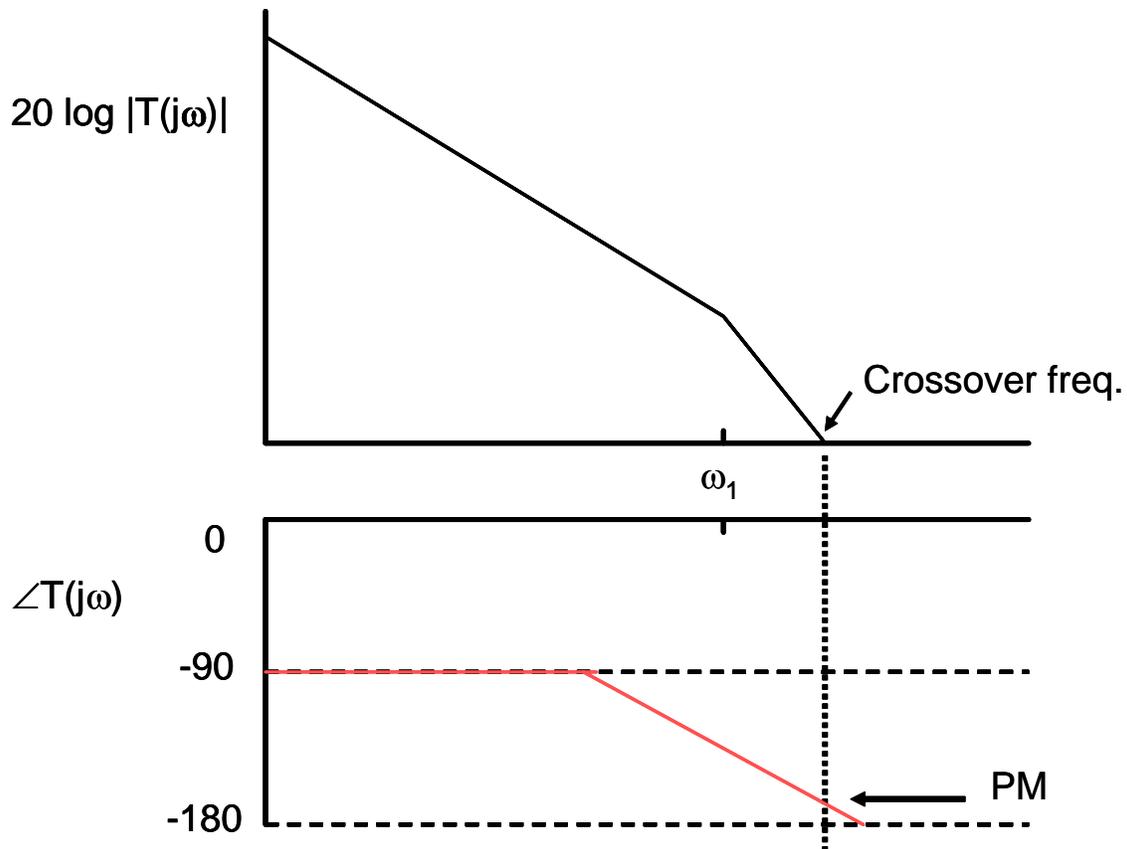
This network has a cutoff (3 dB) frequency $\omega_1 = 1/RC$. Thus, the filter transfer function is a simple lowpass,

$$F(s) = \frac{1}{1 + s/\omega_1} .$$

Then, $T(s)$ becomes second order, Type 1:

$$T(s) = \frac{K_O}{s} \frac{K_D}{1 + s/\omega_1} = \frac{K_V}{s(1 + s/\omega_1)}$$

Bode Plot: Now look at the Bode plot of $T(j\omega)$.



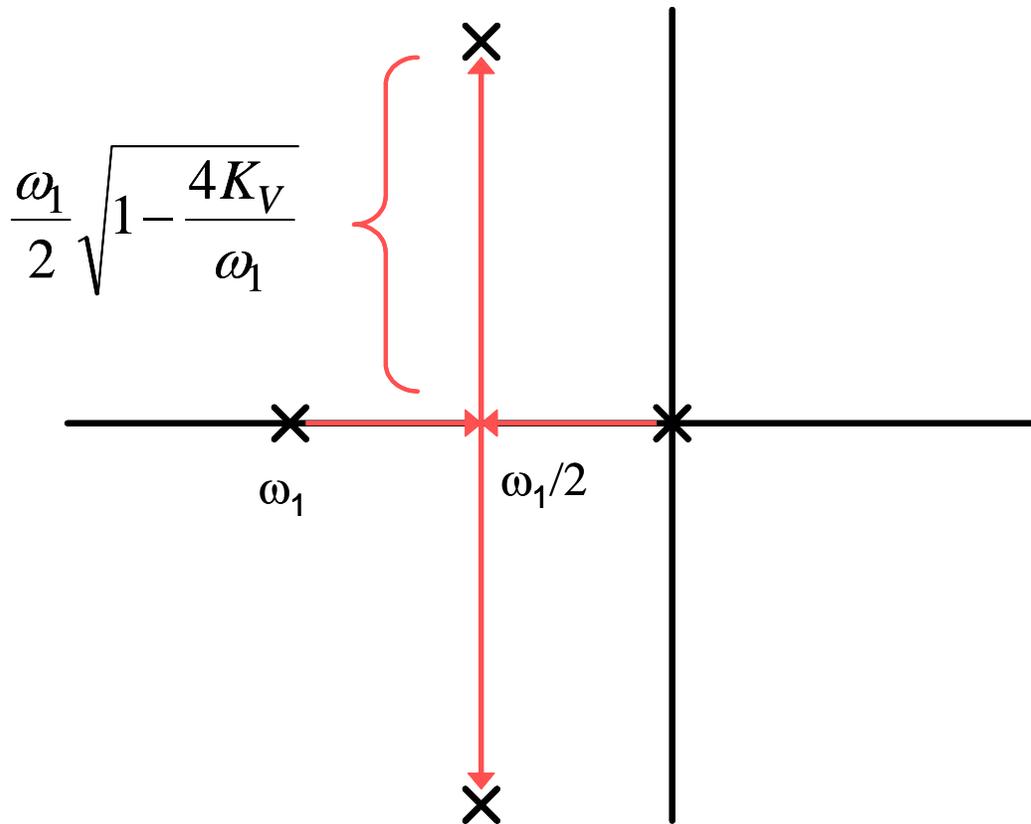
If the loop filter frequency is lower than the crossover frequency, which you might want to do to attenuate the high frequency ripple from the phase detector, then the phase margin can become unacceptably small. And, if we increase the loop gain, $K_V = K_D K_O$, to reduce the residual phase error, we get even smaller phase margin. Thus, we have a conflict between stability of the loop and minimizing the phase error. However, the loop can be made to work if $\omega_1 > \omega_{\text{crossover}}$. But, then we may have insufficient filtering of the phase detector output.

Before we fix this problem, let's look at the root locus and then the closed loop response of this PLL.

Root Locus: Since there are no zeros, the root locus represents the roots of the denominator of the closed loop transfer function. Set $1 + T(s) = 0$ and solve for s as a function of K_V .

$$s = -\frac{\omega_1}{2} \left(1 \pm \sqrt{1 - \frac{4K_V}{\omega_1}} \right)$$

We see that as K_V is increased, the roots approach one another then become complex conjugates.



We can have a very underdamped response when $\omega_1 \ll K_v$. Think about the inverse Laplace transform of the complex conjugate pole pair.

$$e^{-\omega_1 t/2} \sin\left(\frac{\omega_1}{2} \sqrt{1 - \frac{4K_v}{\omega_1}} t\right)$$

There is an exponentially decaying term determined by the real part of the roots that shows how long it takes the system to settle after a phase or frequency step and a ringing frequency dictated by the imaginary part of the pole pair. Again, when $\omega_1 \ll K_v$, we have a high ringing frequency and a long settling time, characteristic of a system that is not very useful.

It is sometimes useful to define a natural frequency, ω_n , and a damping factor, ζ . This is standard control system terminology for a second order system. The key is to put the denominator of the closed loop transfer function, $1 + T(s)$, into a “standard” form: either

$$s^2 + 2\zeta\omega_n s + \omega_n^2$$

or

$$\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n}s + 1 \ .$$

Taking the first formula, $1 + T(s)$ can be written as:

$$s^2 + \omega_1 s + K_V \omega_1$$

so, we can associate ω_n and ζ with:

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2} \sqrt{\frac{\omega_1}{K_V}}$$

This form allows you to use standard equations and normalized plots to describe the frequency and transient response of the system. As we saw with the other ways of representing the frequency response of the system, a large K_V , which we like for reducing phase error, leads to a small ζ , which is bad for stability and settling time.

For example, the transient response for a Type 1, second order lowpass system such as this is plotted in the next figure taken from Motorola App. Note AN-535. It is clear that damping factors less than 0.5 produce severe overshoot and ringing.

In the frequency domain, the closed loop transfer function will also exhibit gain peaking when the system is underdamped. This is the same effect that we see with feedback amplifiers.

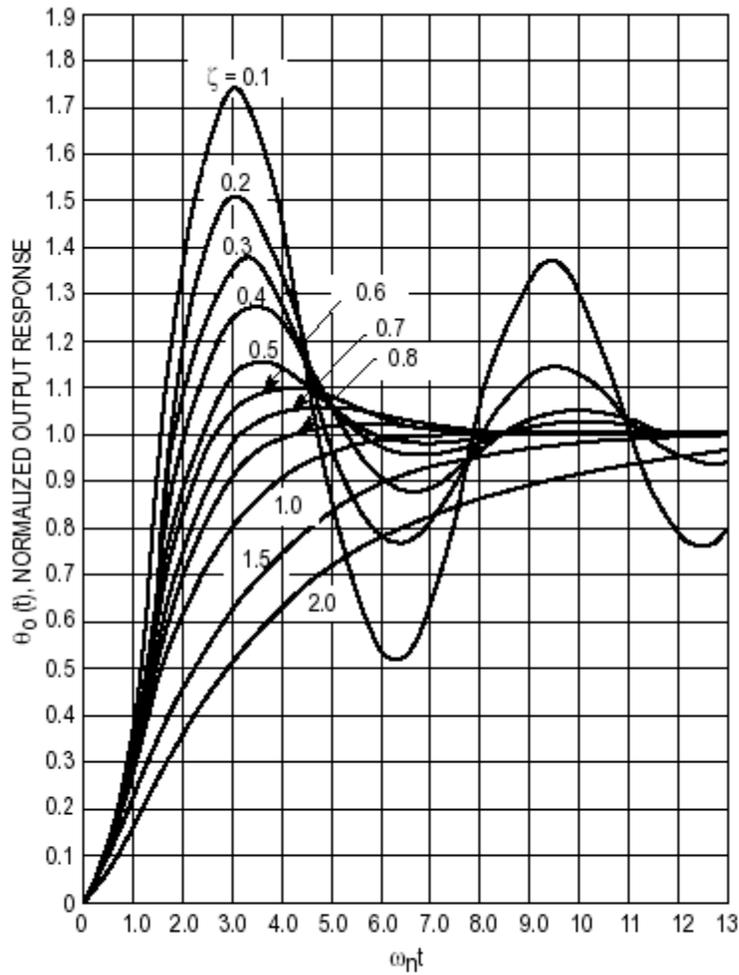


Figure 4. Type 1 Second Order Step Response

So, it is clear that we need a better transfer function that gives us more flexibility in determining the bandwidth of the filter and the stability of the system. You can't obtain a narrow loop bandwidth without reducing the phase margin/damping factor.

Add a zero to the loop filter transfer function to manipulate the root locus and improve stability.

These parameters will have a strong effect on the loop dynamics which control overshoot and settling time. From the system design perspective, overshoot can be quite harmful, since it will cause the frequency to temporarily exceed the steady state value. Thus, the output of the synthesizer might land in an adjacent channel during part of the transient response. Settling time can also be critical since many TDM applications use different receive and transmit frequencies. The settling time determines how long you must wait until transmitting or receiving after a hop in frequency.

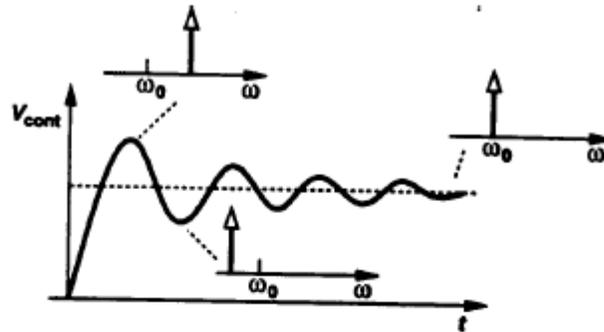


Figure 8.33 Variation of VCO frequency during synthesizer settling.

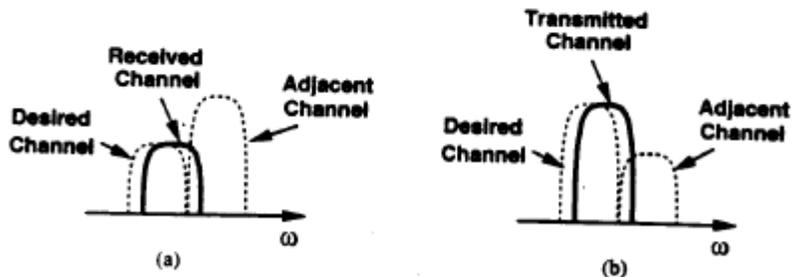
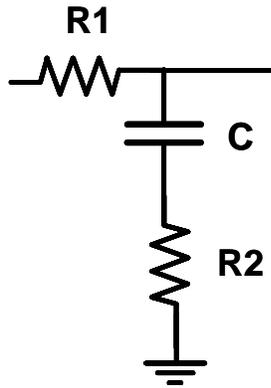


Figure 8.34 Effect of synthesizer settling on received and transmitted channels.

Ref. B. Razavi, RF Microelectronics, Prentice-Hall, 1998.

Here you see the consequences of PLL settling time if the PLL is being used as a local oscillator for a receiver or transmitter.

Adding a resistor to the lowpass loop filter contributes a zero to its transfer function.



$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$

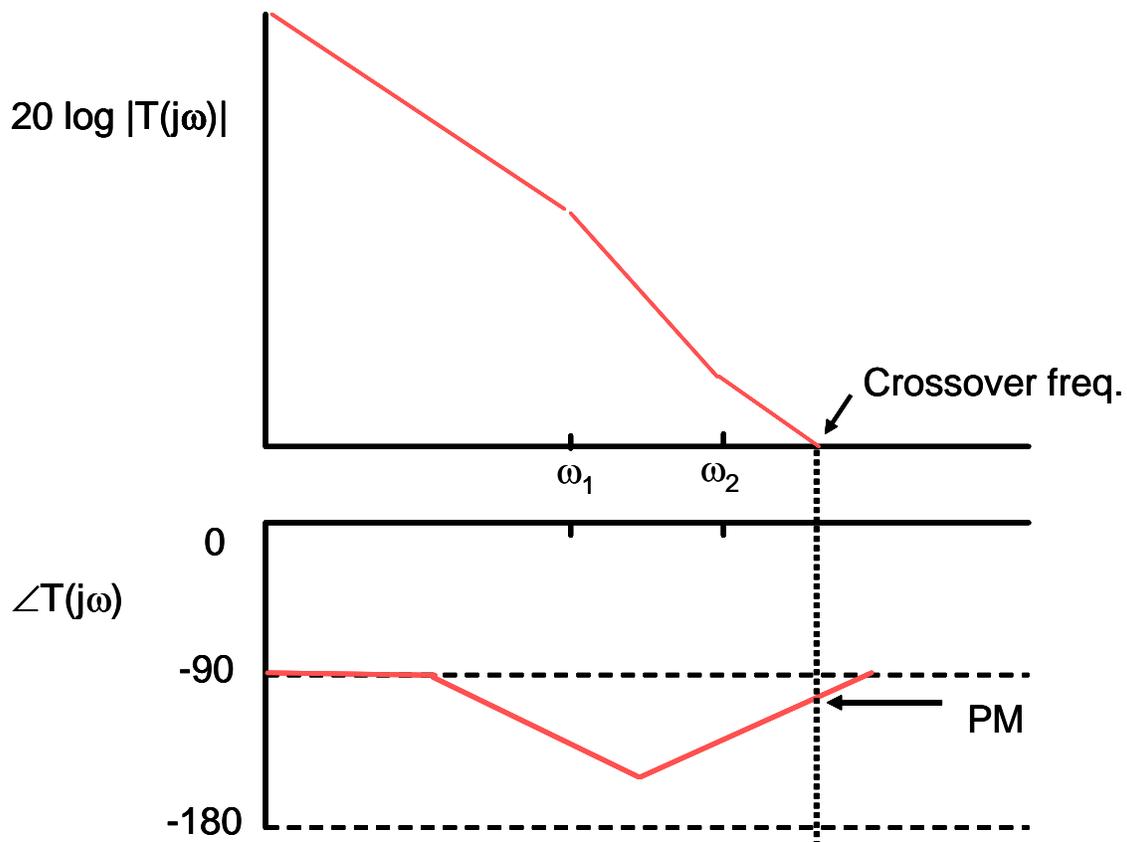
where

$$\omega_1 = \frac{1}{(R_1 + R_2)C}$$

$$\omega_2 = \frac{1}{R_2C}$$

Thus, the zero frequency is always higher than the pole frequency.

Check out the Bode plot, root locus and transient response again.



Note that the phase margin has increased. Now, small values of ω_1 can be used for narrower filter bandwidth, or higher K_V values can be used for lower phase error without sacrificing phase margin. Note how phase margin now improves when the crossover frequency is increased due to higher gain.

Root Locus: Calculate the closed loop transfer function for this PLL with the pole-zero loop filter.

$$\frac{\phi_o}{\phi_{in}} = \frac{(1 + s/\omega_2)}{\frac{s^2}{K_V \omega_1} + s \left(\frac{1}{K_V} + \frac{1}{\omega_2} \right) + 1}$$

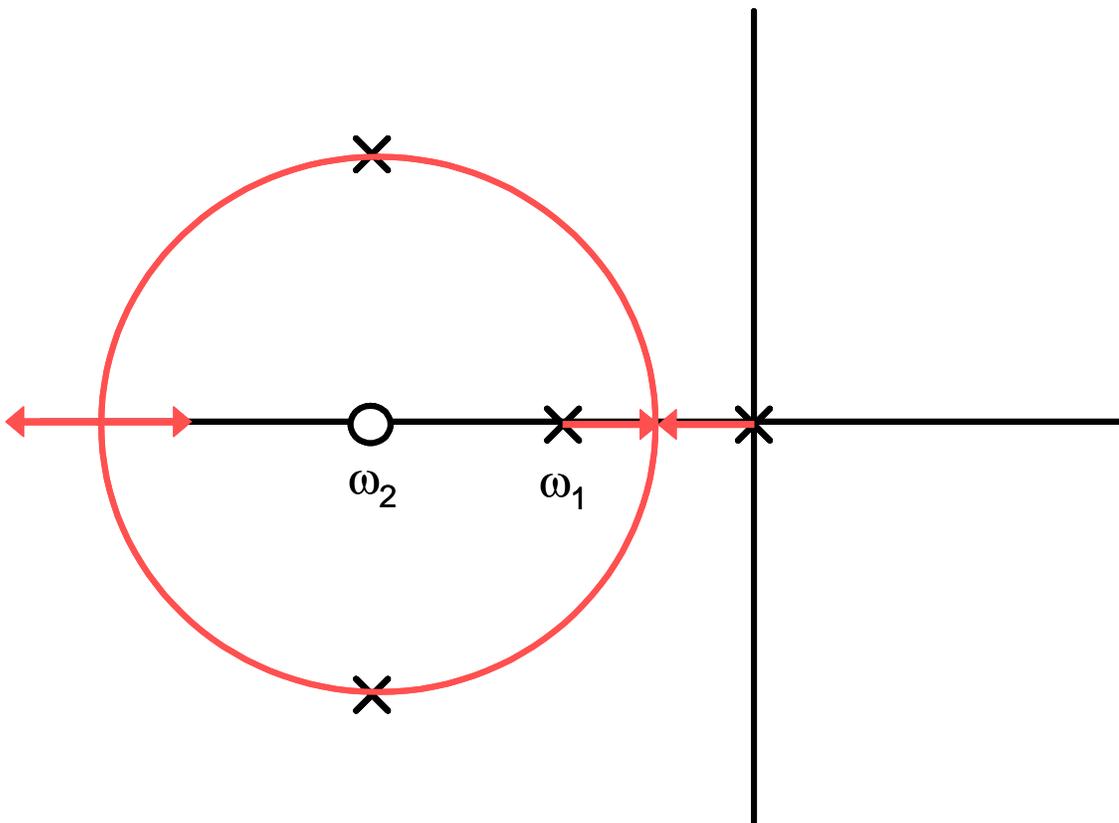
The denominator is of the form $1 + T(s)$. We can also extract ω_n and ζ from the closed loop transfer function since the denominator is in one of the standard forms.

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2} \sqrt{\frac{\omega_1}{K_V}} + \frac{1}{2} \frac{\omega_n}{\omega_2}$$

Then, solve for s; these are the poles.

$$s = -\zeta \omega_n \pm \omega_n \sqrt{\zeta^2 - 1}$$



We see that ω_n is the same as with the simple RC filter, but the damping factor has an added term. The first term is quite small in most cases, but the second term can be made large by increasing K_V or reducing ω_2 . We still have a type 1 system, but we have an added term that we can use to improve stability, the zero frequency. Note that the zero is in the forward path and therefore shows up in the closed loop transfer function. It will affect the frequency and transient response.

FREQUENCY RESPONSE

According to Gardner¹, the loop bandwidth for this Type 1, second-order loop with a forward path zero is given by:

$$\omega_h = \omega_n \left[1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2) + 1} \right]^{1/2}$$

According to this, we have a bandwidth of about $2\omega_n$ for $\zeta = 0.707$.

Refer to Fig. 2.3 from Gardner. This is a plot of the closed loop frequency response of a high gain second order PLL: $20 \log |H(j\omega)|$. A high gain PLL is defined by $K_V/\omega_2 \gg 1$.

F.M. Gardner, Phase Lock Techniques, Wiley 1979.

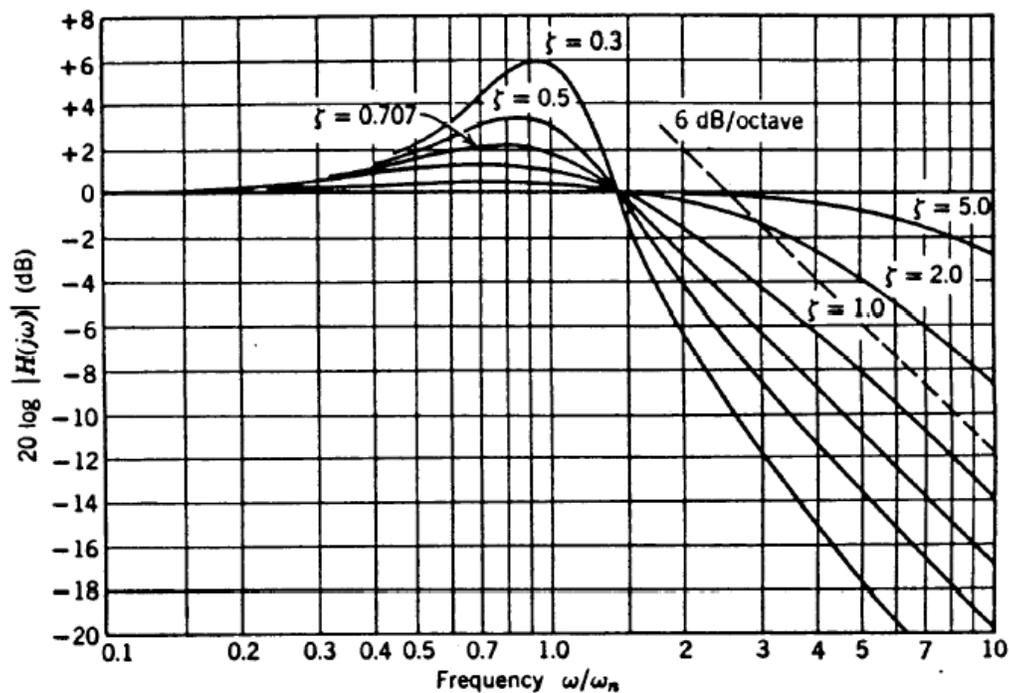


Figure 2.3 Frequency response of a high-gain second-order loop.

¹ F. M. Gardner, Phase Lock Techniques, Second ed., Wiley, 1979.

From this plot, we can see how the 3 dB frequency and gain flatness varies with ζ . Also, we see that the natural frequency must be significantly greater than the maximum frequency of phase variation for the reference (ϕ_{in}) when $\zeta < 1$ in order to avoid gain peaking. This is a consequence of the zero added to the transfer function. For applications that require very small gain peaking (such as clock recovery), $\zeta > 2$ is often employed.

PHASE ERROR

There is no frequency error when the loop is locked

- Input frequency = output frequency

But, it is possible to have a phase error for some input transient phase conditions. The phase error must remain bounded in order to keep the loop locked. To analyze in the frequency domain, we assume a sinusoidal phase variation at the input.

$$\text{PHASE ERROR} = \varepsilon(s) = \frac{IN(s)}{1 + T(s)}$$

$$\text{STEADY STATE ERROR} = \varepsilon_{SS} = \lim_{s \rightarrow 0} [s\varepsilon(s)] = \lim_{t \rightarrow \infty} \varepsilon(t)$$

Fig. 2.4 from Gardner's book illustrates how the phase error, expressed as

$$\varepsilon(s) = 20 \log (\phi_{out}/\phi_{in}) \text{ dB}$$

increases as the input frequency approaches the natural loop frequency for the case with $\zeta = 0.707$. For input phase variations well below the loop bandwidth, the loop tracks very well. This is because $|T(j\omega)|$ is large at low frequency.

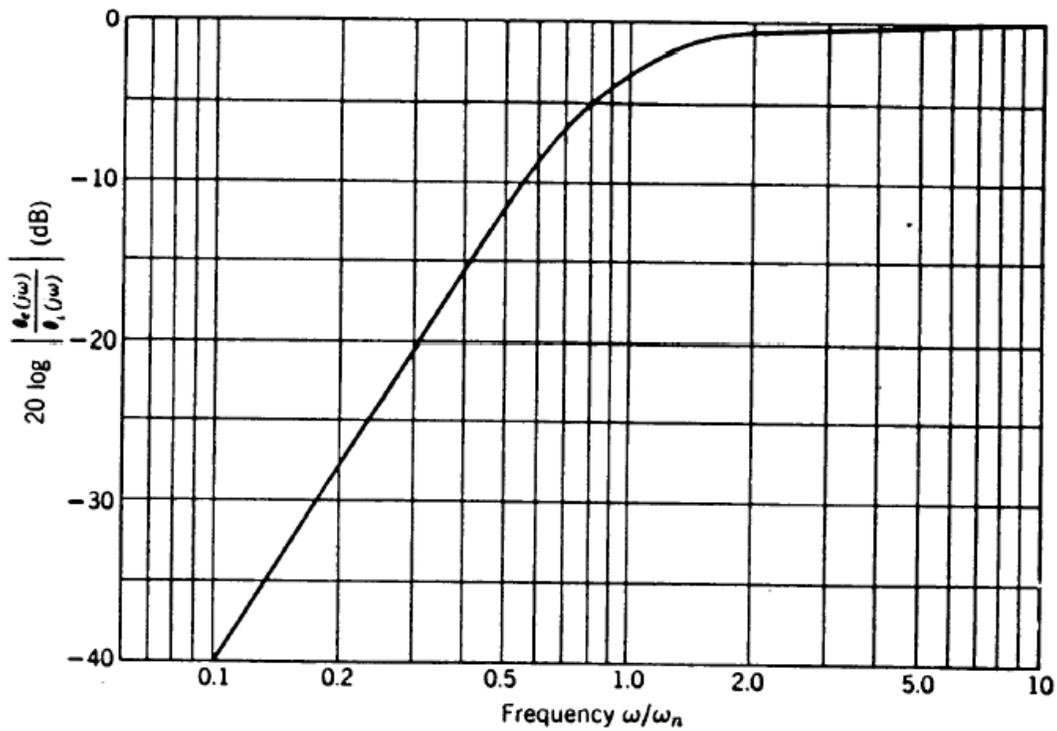


Figure 2.4 Error response of high-gain loop, $\zeta = 0.707$.

TRANSIENT PHASE ERROR

- Inverse Laplace transform of $\varepsilon(s)$

Now, let's look more closely at how the phase error is affected by the type of transient phase signal at the input of the Type I PLL.

1. Phase step. Because $\phi_{in}(t) = \Delta\theta u(t)$, in the frequency domain,

$$\phi_{in}(s) = \frac{\Delta\theta}{s}$$

The steady-state phase error can be calculated from $\varepsilon(s)$ and ε_{ss} above.

$$\varepsilon_{ss} = \lim_{s \rightarrow 0} \frac{s \frac{\Delta\theta}{s}}{1 + \frac{K_V}{s} \left(\frac{1 + s/\omega_2}{1 + s/\omega_1} \right)} = 0$$

Thus, there is only a transient phase error for a phase step. This is reasonable, because the control voltage must return to the same value after the phase step is completed. The frequency will be the same before and after the step.

2. Frequency step.

$$\epsilon_{ss} = \lim_{s \rightarrow 0} \frac{s \frac{\Delta\omega}{s^2}}{1 + \frac{K_V}{s} \left(\frac{1 + s/\omega_2}{1 + s/\omega_1} \right)} = \lim_{s \rightarrow 0} \frac{\Delta\omega}{s + K_V \left(\frac{1 + s/\omega_2}{1 + s/\omega_1} \right)} = \frac{\Delta\omega}{K_V}$$

There is a static “error”, but it can be made small by increasing K_V . This is consistent with the idea that a shift in control voltage is needed to give a step in frequency. The phase error needed to generate this control voltage step varies inversely with the loop gain.

3. Frequency ramp. We could do the same exercise for a frequency ramp (Doppler shift). This gives an unlimited steady state error. So, a type I loop is not suitable for tracking a moving source.

Summarizing:

Type I; second order: $F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$

Input	$\phi_{in}(s)$	ϵ_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	$\Delta\omega/K_V$
Freq. ramp	A/s^3	infinite

For the frequency synthesis application, we want to have ideally perfect phase tracking for phase and frequency steps. When the synthesizer frequency is changed, it is a discontinuous step in modulus, and we want to have zero steady state phase error in this case.

In the phase error analysis for the type 1 passive pole-zero lag filter, we found that there was a static phase error for a frequency step. To eliminate this phase error, we need a TYPE = 2 loop gain function. This requires an ideal integrator rather than a passive lead-lag filter.

Type 2; second order:

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

Input	$\phi_{\text{ref}}(s)$	ϵ_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	0
Freq. ramp	A/s^3	kA

Placing an opamp RC integrator or charge pump in the loop will give a filter transfer function of the form:

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

where providing a pole at $s = 0$ and a zero at ω_2 . Then, the loop gain $T(s)$ will be that of a type 2 control system:

$$T(s) = \frac{K_D K_O (1 + s/\omega_2)}{s^2 / \omega_1}$$

Details regarding the implementation of these filters will be presented later.

Now find the closed loop transfer function by inserting $F(s)$.

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

$$H(s) = \frac{(1 + s/\omega_2)}{\frac{s^2}{K_D K_O \omega_1} + \frac{s}{\omega_2} + 1}$$

Thus, we can see that

$$\omega_n = \sqrt{K_D K_O \omega_1}$$

$$\zeta = \frac{\omega_n}{2\omega_2}$$

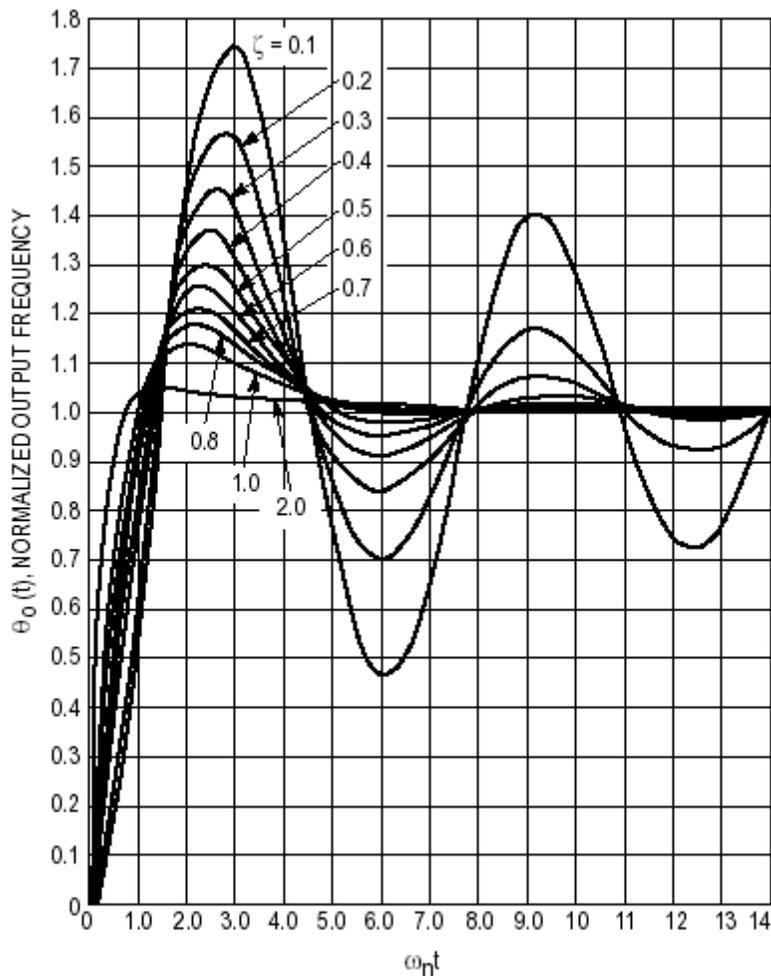


Figure 6. Type 2 Second Order Step Response

Ref. Motorola AN535

Here we see the phase and frequency step response for a type 2 PLL in terms of the key loop parameters. The settling time can be determined by setting an error tolerance around $\theta_o(t) = 1$. For example, if settling to 5% were the criteria and if $\zeta = 1$, the response first falls within the boundary of 0.95 or 1.05 for $\omega_n t = 4.5$. Then settling time t can be determined since natural frequency ω_n will also be known.

Root Locus:

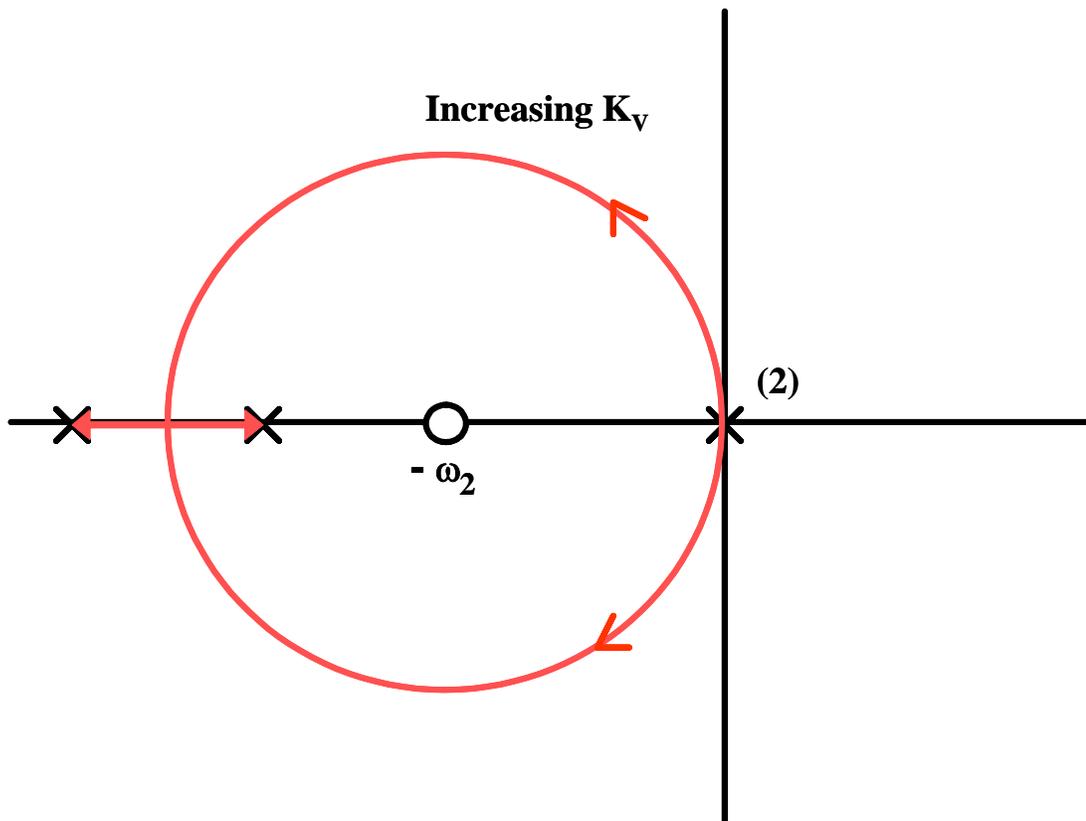
Now, find the poles of $1 + T(s) = 0$

Let $K_V = K_O K_D$

$$\frac{s^2}{K_V \omega_1} + \frac{s}{\omega_2} + 1 = 0$$

$$s = -\zeta \omega_n \pm \omega_n \sqrt{\zeta^2 - 1}$$

Now examine the root locus. As the loop gain K_V increases, both real and imaginary parts grow. The locus follows a circle centered around the zero. The poles become real again when $\zeta = 1$. This happens when $K_V = 4\omega_2^2/\omega_1$. We have the same geometric interpretation that was discussed in the FMD notes.



Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ω_n and ζ , so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zero as opposed to the feedback zero case that we discussed in the feedback lectures.

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1)^2 + 1} \right]^{1/2}$$

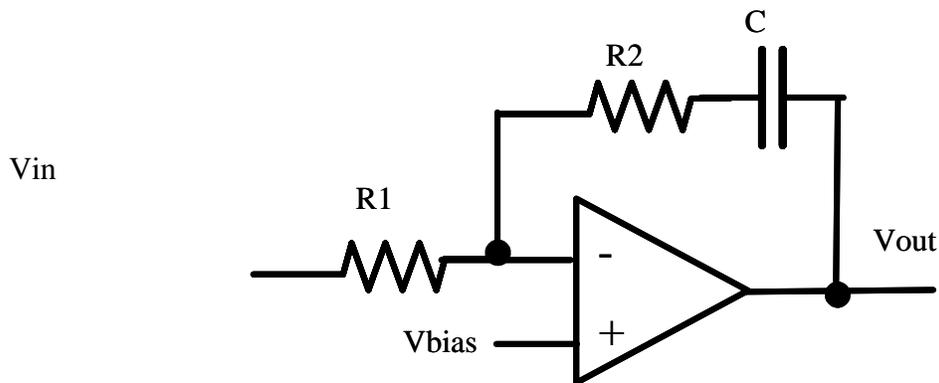
$$\omega_{3dB} = 2 \omega_n \quad \text{for } \zeta = 0.707$$

$$\omega_{3dB} = 2.5 \omega_n \quad \text{for } \zeta = 1$$

Since the loop gain peaking and overshoot is greater when the zero is present, we also expect bandwidth to be higher as this shows.

The effect of bandwidth on the synthesizer noise performance will be discussed later.

Loop Filter – OpAmp



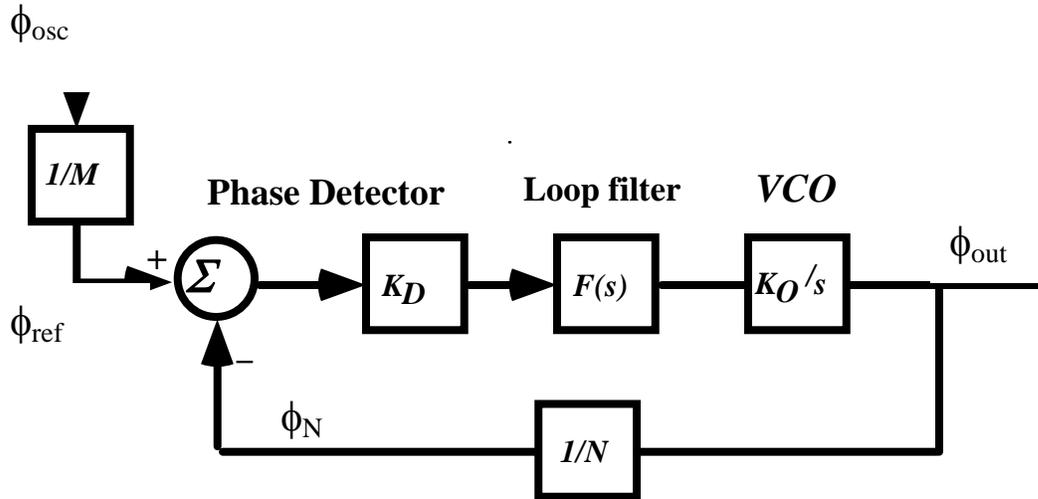
An op amp can be used to form a filter that includes a pole at $s = 0$ and a finite zero. For example, the circuit above can be analyzed using the virtual ground approximation to obtain $F(s)$.

$$F(s) = \frac{V_{out}}{V_{in}} = \frac{1 + sR_2C}{sR_1C}$$

V_{bias} can be used to level shift between the phase detector and the VCO.

Synthesizer PLL

We will now add the divider $1/N$ to the feedback path. This architecture is called an “integer- N ” synthesizer.



Thus,

$$\frac{\phi_N}{\phi_{out}} = \frac{1}{N}$$

and also, $N = \frac{\omega_{out}}{\omega_{ref}}$

We can calculate the loop gain, $T(s)$:

$$T(s) = \frac{K_D K_O F(s)}{N s}$$

- We see that the loop gain is reduced by a factor of N .
- Also, in most applications, N is not constant, so
- $K_V = K_D K_O$ is not a constant – varies with frequency according to the choice of N

Using the $F(s)$ determined for the opamp pole-zero loop filter:

$$F(s) = \frac{1 + s/\omega_2}{s/\omega_1}$$

where $\omega_1 = 1/R_1C$ and $\omega_2 = 1/R_2C$,

$$1 + T(s) = 1 + \frac{K_V}{Ns} \left(\frac{1 + s/\omega_2}{s/\omega_1} \right) = 0$$

$$1 + T(s) = \frac{Ns^2}{K_V\omega_1} + \frac{s}{\omega_2} + 1 = 0$$

We can now determine how the natural frequency and damping are affected by N:

$$\omega_n = \sqrt{\frac{K_V\omega_1}{N}} = \sqrt{\frac{K_V}{R_1CN}}$$

$$\zeta = \frac{\omega_n}{2\omega_2} = \frac{R_2}{2} \sqrt{\frac{K_VC}{R_1N}}$$

Phase Frequency Detector

The phase-frequency detector shown below is a widely used architecture in frequency synthesizers. As opposed to the XOR phase detector that we first considered, this one produces two outputs: Q_A and Q_B , or as is customary, UP and DOWN respectively.

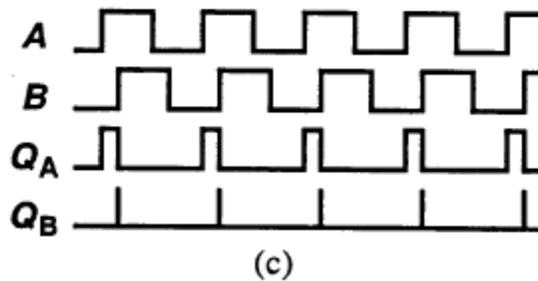
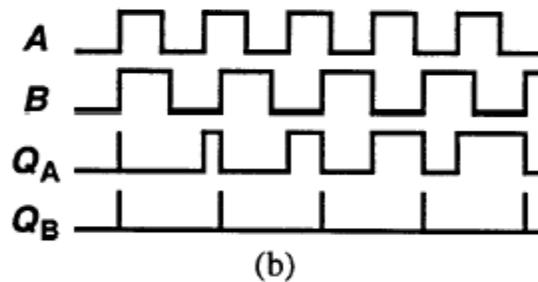
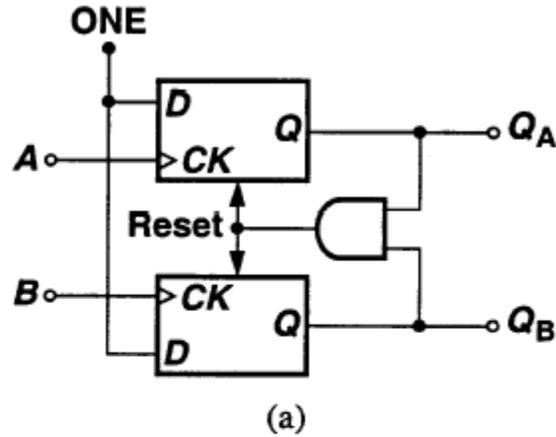
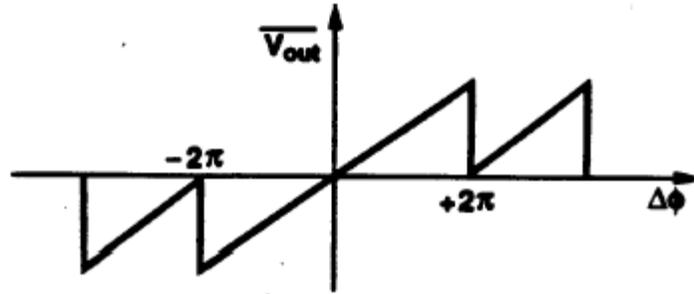


Figure 3.26. (a) Phase/frequency detector. Circuit response with (b) $\omega_A \geq \omega_B$, (A leading B).

Ref. J. Savoj and B. Razavi, High Speed CMOS for Optical Receivers, Kluwer Academic Publishing, 2001. (and many other books)

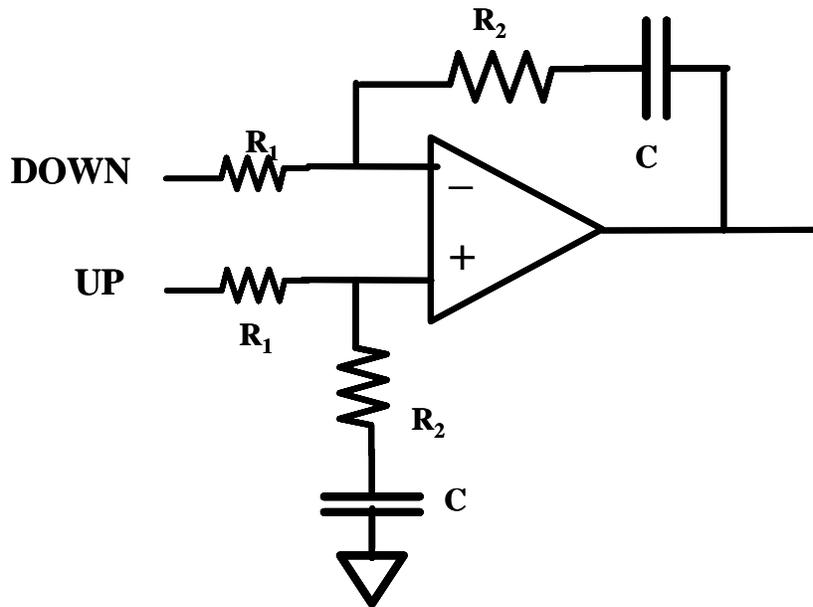
This phase detector has a much larger phase range (4π) of operation, and it will produce an output that drives the frequency in the right direction when it is out of lock. It also has zero offset when the phases are aligned and is insensitive to the duty cycle of the inputs since edge-triggered flip-flops are used.



PFD characteristic.

When the phases coincide, both outputs produce minimum width pulses. When there is a phase or frequency error, the width of the UP or DOWN pulses increases. When integrated by the loop filter, this causes the control voltage of the VCO to move toward the locked condition of equal frequency and phase.

Because both outputs must be combined to obtain the desired output, the loop filter must be modified for differential inputs as shown below. $F(s)$ is the same as that of the single ended version.



Charge Pump Loop Filter

An alternative loop filter implementation called the charge pump is widely used for many applications. It is very convenient to implement in CMOS.

- The PFD output produces UP (Q_A) and DOWN (Q_B) pulses whose width is proportional to the phase error.
- Charge pump current sources I_1 and I_2 must produce exactly equal currents. They charge and discharge the capacitor, C_P , in discrete steps.
- If there is a static phase error $\Delta\phi$ at the PFD input, the capacitor, C , will be charged indefinitely – therefore, the DC gain is infinite: an ideal integrator. So, we expect to have zero static phase error. This is unlike the type I loop which gave $\Delta\phi = \Delta\omega/K_V$ steady state phase error.
- The CP PLL will detect small phase errors and correct them as long as the frequency of the phase error (jitter frequency) is within the loop 3 dB bandwidth. This phase comparison occurs on every cycle.

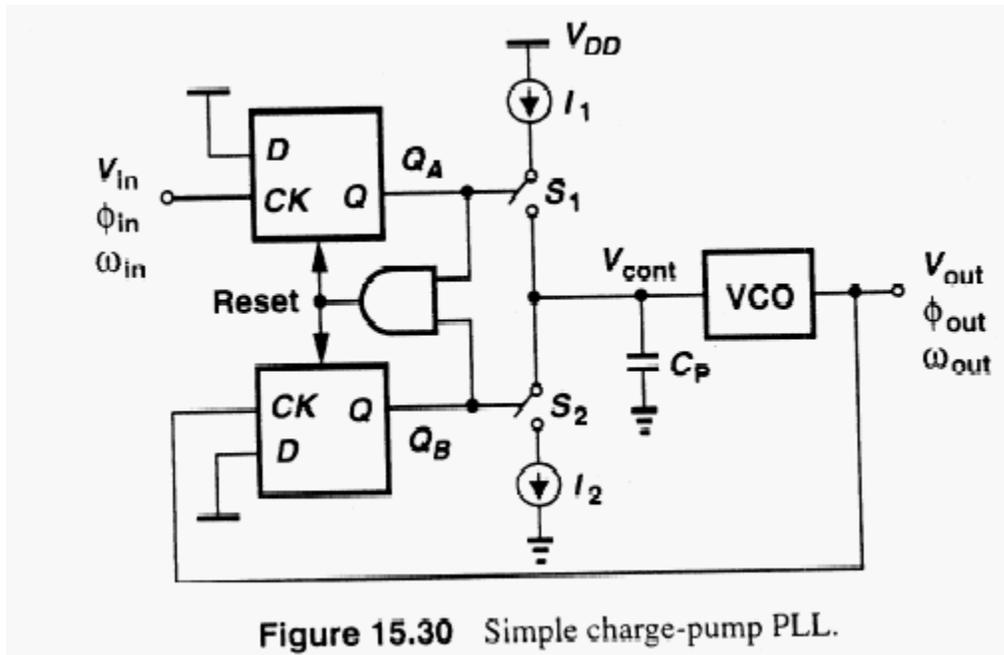


Figure 15.30 Simple charge-pump PLL.

(from B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.)

To illustrate how the charge pump works and how it might be analyzed in a linearized model, refer to Fig. 15.32. Here we assume that $I_1 = I_2 = I_P$ and that a phase step $\Delta\phi$ occurs at $t = 0$.

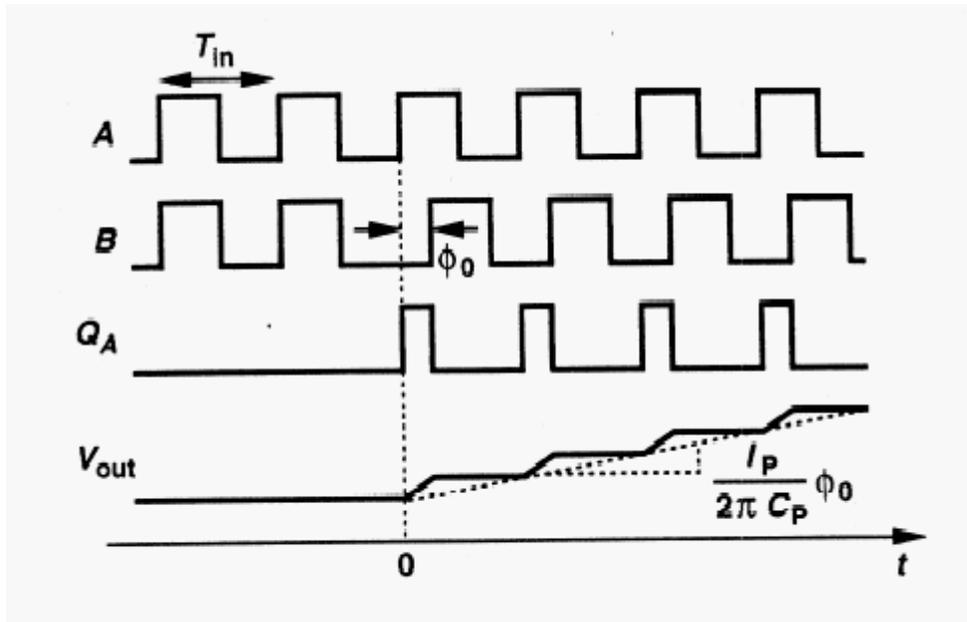


Figure 15.32 Step response of PFD/CP/LPF combination.

(from B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.)

First consider the time domain picture above. $\Delta\phi = \phi_0 u(t)$

Q_A produces pulses that are of width

$$\frac{\Delta\phi}{2\pi} T_{in} = \Delta t .$$

I_P charges C_P by

$$\Delta V = \frac{I_P}{C_P} \Delta t = \frac{I_P}{C_P} \frac{\phi_0}{2\pi} T_{in}$$

in every period. We can approximate this as a linear ramp with slope

$$slope = \frac{I_P}{2\pi C_P} \phi_0$$

Thus, the output voltage from the charge pump can be described by

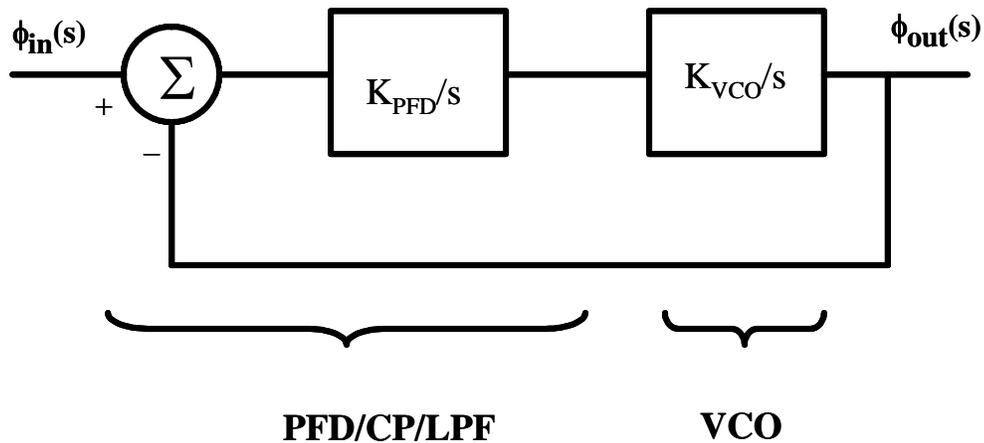
$$V_{out}(t) = \frac{I_P \phi_0}{2\pi C_P} t u(t)$$

The derivative of the step response is the impulse response, so we can determine the frequency domain transfer function.

$$h(t) = \frac{dV_{out}}{dt} = \frac{I_P}{2\pi C_P} u(t)$$

Take the Laplace transform to obtain the frequency domain transfer function.

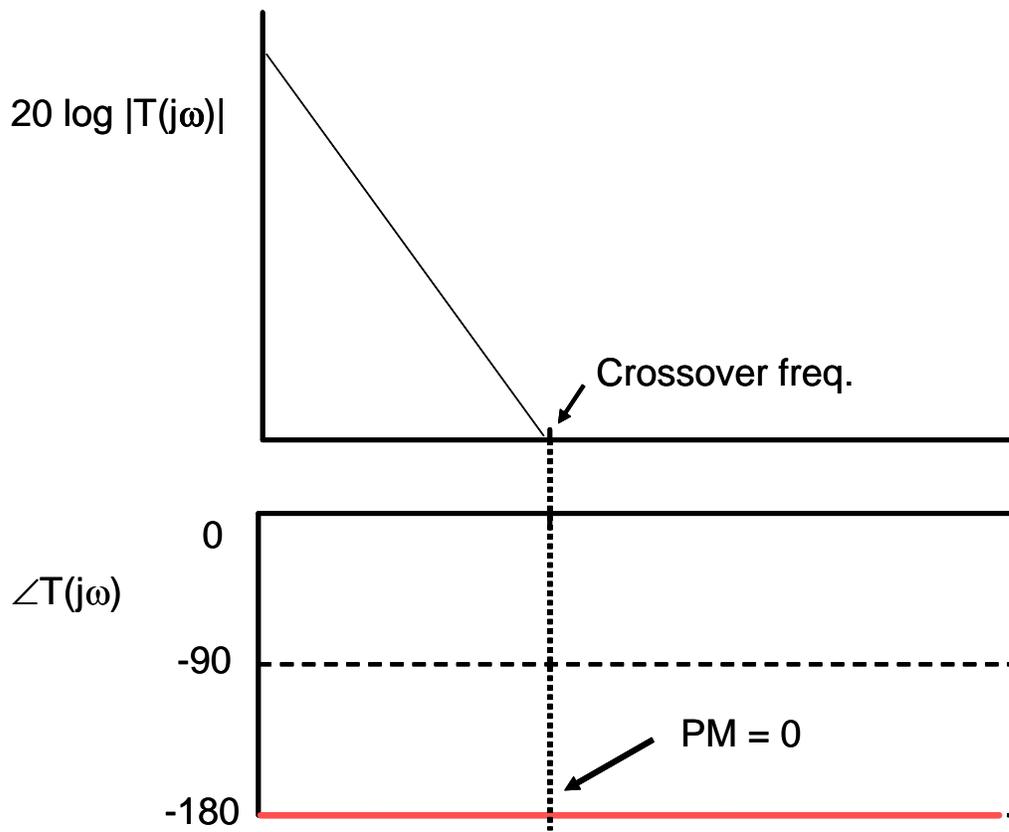
$$H(s) = \frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi C_P} \frac{1}{s} = \frac{K_{PFD}}{s}$$



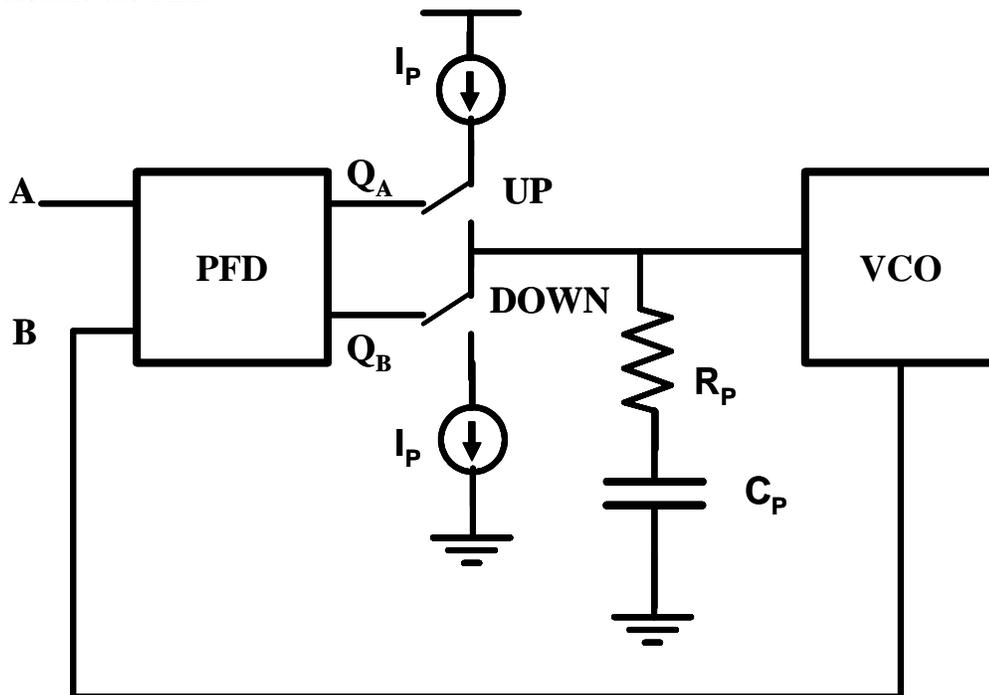
Here is the block diagram of the CP PLL. We see that the loop gain function $T(s)$ has a factor of s^2 in the denominator. Thus, it is a type II loop.

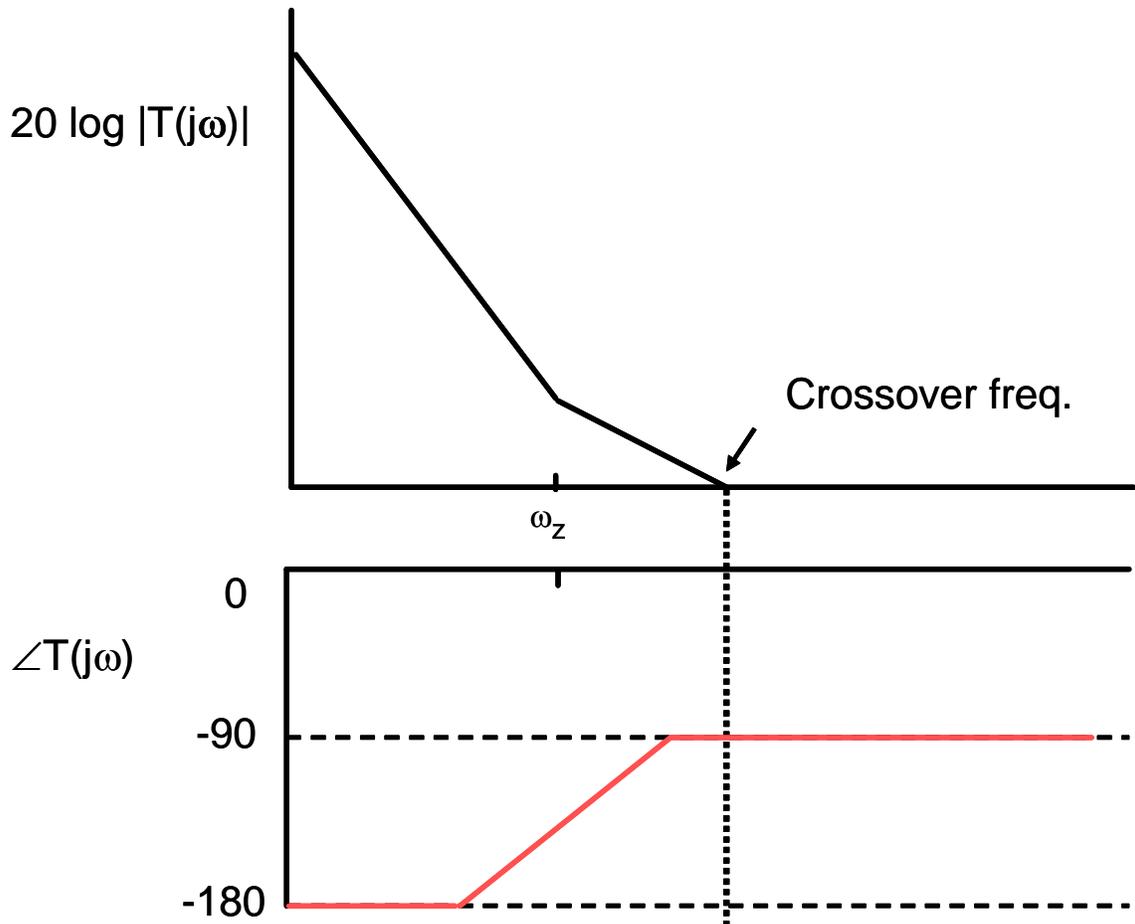
$$T(s) = \frac{K_{PFD}}{s} \frac{K_{VCO}}{s}$$

But, because of that, we have a big problem. The phase margin is always zero as shown by the Bode plot below.



Therefore, we must add a zero to the loop filter transfer function to provide some phase lead to stabilize the PLL.

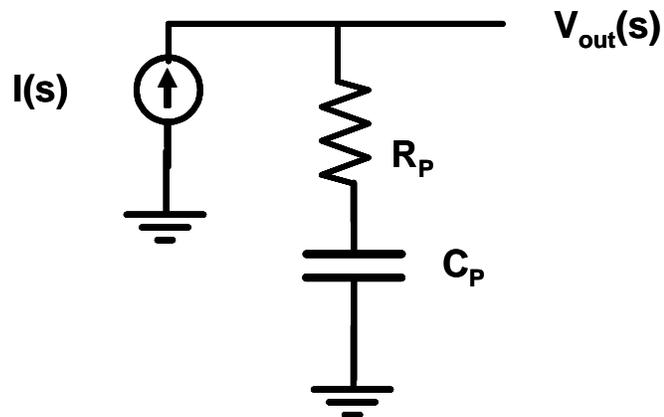




Now, we can see that an increase in the loop gain will improve phase margin.

To determine $T(s)$ for this case, we want to calculate $V_{out}(s)/\Delta\phi$ again, adding the resistor to the charge pump filter.

New filter:



The phase frequency detector (PFD) with single capacitor C_P has

$$H(s) = \frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi C_P} \frac{1}{s} = \frac{K_{PFD}}{s}$$

To find the frequency response of the input current, we note that,

$$I(s) = V_{out}(s)/Z(s) = V_{out}(s)/(1/sC_P)$$

where $Z(s)$ is the complex impedance. So, the current source can be modeled as:

$$\frac{I(s)}{\Delta\phi} = \frac{I_P}{2\pi}$$

Now, let's use this to modify $H(s)$ for the series RC loop filter. To do this, just replace the impedance $1/sC_P$ with $Z(s) = R_P + 1/sC_P$.

$$\frac{V_{out}(s)}{\Delta\phi} = \frac{I_P}{2\pi} \left(R_P + \frac{1}{sC_P} \right)$$

The loop gain $T(s)$ is therefore

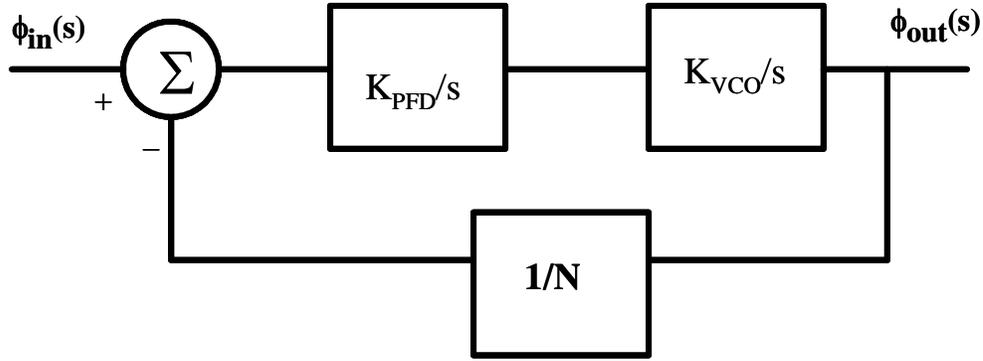
$$\begin{aligned} T(s) &= \frac{\phi_{out}(s)}{\phi_{in}} = \frac{I_P}{2\pi} \left(R_P + \frac{1}{sC_P} \right) \frac{K_{VCO}}{s} \\ &= \frac{I_P K_{VCO}}{2\pi C_P} \frac{(R_P C_P s + 1)}{s^2} \end{aligned}$$

We see that a zero at $\omega = 1/R_P C_P$ has been added to the transfer function. This provides the necessary phase lead to achieve stability.

Of course a frequency divider can be placed in the feedback path if the output frequency is to be multiplied by the PLL. Divide by N gives

$$\begin{aligned} \phi_{out} &= N\phi_{in} \\ \omega_{out} &= N\omega_{in} \end{aligned}$$

This added divider would be needed in a frequency synthesizer application or clock multiplier application.



$T(s)$ is then modified by a factor of $1/N$.

$$T(s) = \frac{I_P K_{VCO}}{2\pi N C_P} \frac{(R_P C_P s + 1)}{s^2}$$

Now, let's retain the factor of $1/N$ for completeness, and derive the closed loop transfer function. Define $K_V = I_P K_{VCO} / 2\pi C_P$ and zero frequency $\omega_z = 1/R_P C_P$.

$$\begin{aligned} \frac{\phi_{out}(s)}{\phi_{in}} &= \frac{K_V (s/\omega_z + 1) / s^2}{1 + K_V (s/\omega_z + 1) / N s^2} \\ &= \frac{N(s/\omega_z + 1)}{\frac{N}{K_V} s^2 + \frac{s}{\omega_z} + 1} \end{aligned}$$

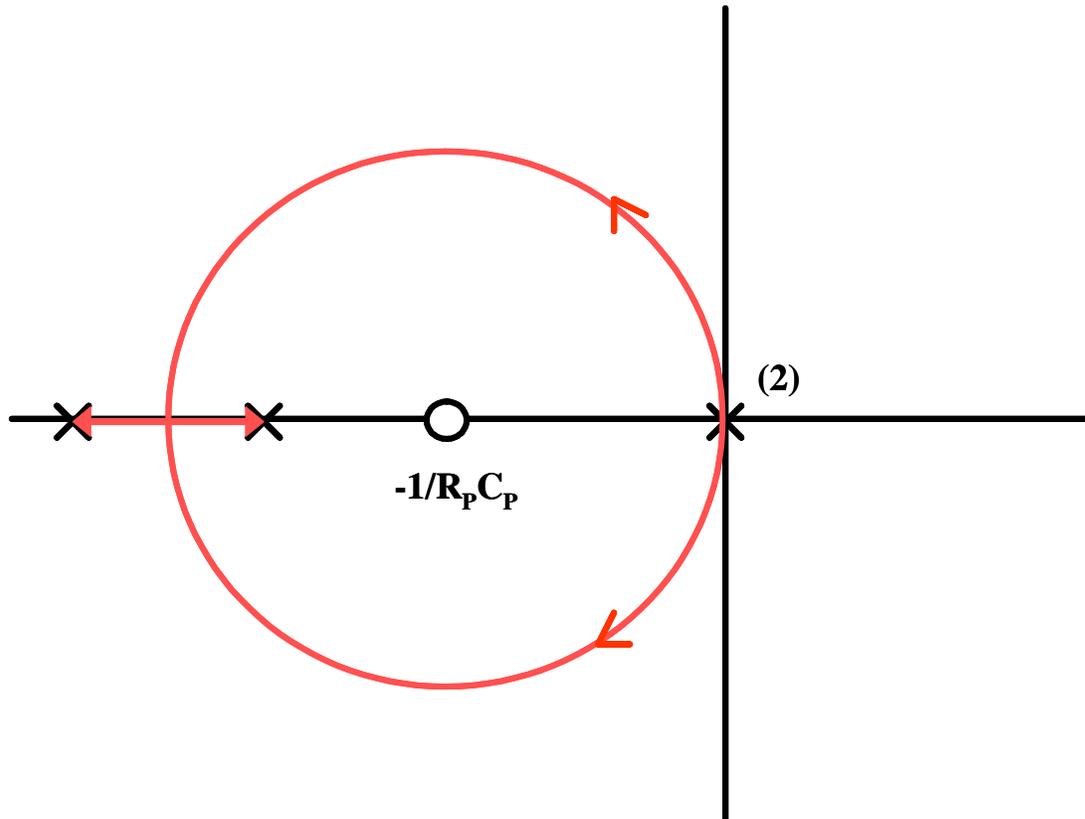
Having put this in one of the standard forms, we can extract ω_n and ζ from the denominator.

$$\begin{aligned} \omega_n &= \sqrt{\frac{K_V}{N}} = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P N}} \\ \zeta &= \frac{\omega_n}{2\omega_z} = \frac{R_P}{2} \sqrt{\frac{I_P K_{VCO} C_P}{2\pi N}} \end{aligned}$$

We can see now with $R_P = 0$, $\zeta = 0$, therefore there is no phase margin and the system is unstable as expected. With added R_P , the damping factor can be increased. Also note

that stability will decrease with increasing N . Loop gain must be increased to compensate for this.

The root locus of the modified charge pump PLL is shown below. It is the same as was obtained for the opamp loop filter.



As loop gain is increased by increasing $I_P K_{VCO}$, the dual poles at $s = 0$ split and form a circular locus, rejoining the real axis at $-1/2R_P C_P$.

The pole locations are found at

$$s = -\zeta\omega_n \pm \omega_n \sqrt{\zeta^2 - 1}$$

Closed Loop Frequency Response

The closed loop frequency response can be evaluated from $H(j\omega)$. In Fig. 2-3, Gardner has plotted the magnitude as a function of ω/ω_n .

Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ω_n and ζ , so bandwidth must be determined in conjunction with the overshoot and settling time specifications. We find again that the formula is different for the case with a forward path zero as opposed to the feedback zero case that we discussed in the feedback lectures.

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1)^2 + 1} \right]^{1/2}$$

$$\omega_{3dB} = 2 \omega_n \quad \text{for } \zeta = 0.707$$

$$\omega_{3dB} = 2.5 \omega_n \quad \text{for } \zeta = 1$$

Since the loop gain peaking and overshoot is greater when the zero is present, we also expect bandwidth to be higher as this shows.

We see that the frequency response is a low pass to ϕ_{in} . Thus, the phase noise of the reference source passes through the PLL and is filtered as shown in Fig. 2-3. Below the 3 dB frequency, we have little attenuation of input noise. Above, noise is reduced by 40 dB/decade.

Also note that for $\zeta < 2$, there is gain peaking. Actually there is always some gain peaking for the Type II CP PLL or the opamp filter PLL because the zero frequency is always less than the pole frequency in the strongly damped case. For some applications, this is inconsequential. However, for clock and data recovery (CDR) use, the SONET specification is very strict: less than 0.1 dB of gain peaking is allowed. This is because in an optical fiber link, the signal may pass through several repeaters that include CDR units. Cascaded transfer functions with gain peaking leads to amplification of jitter (phase noise) close to the 3 dB frequency.

F.M. Gardner, Phase Lock Techniques, Wiley 1979.

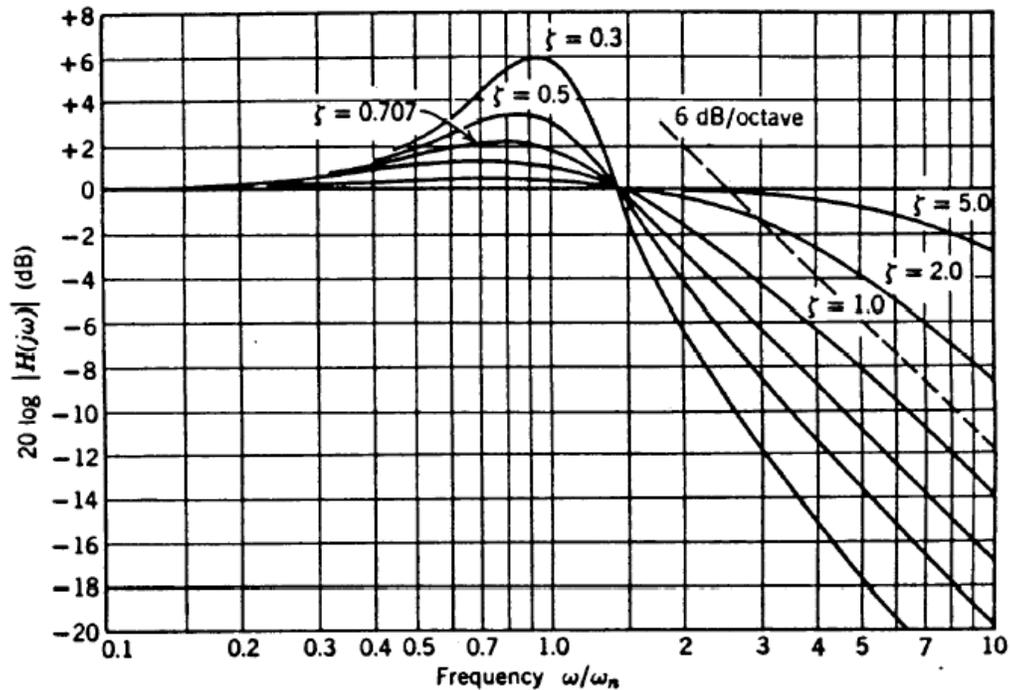


Figure 2.3 Frequency response of a high-gain second-order loop.

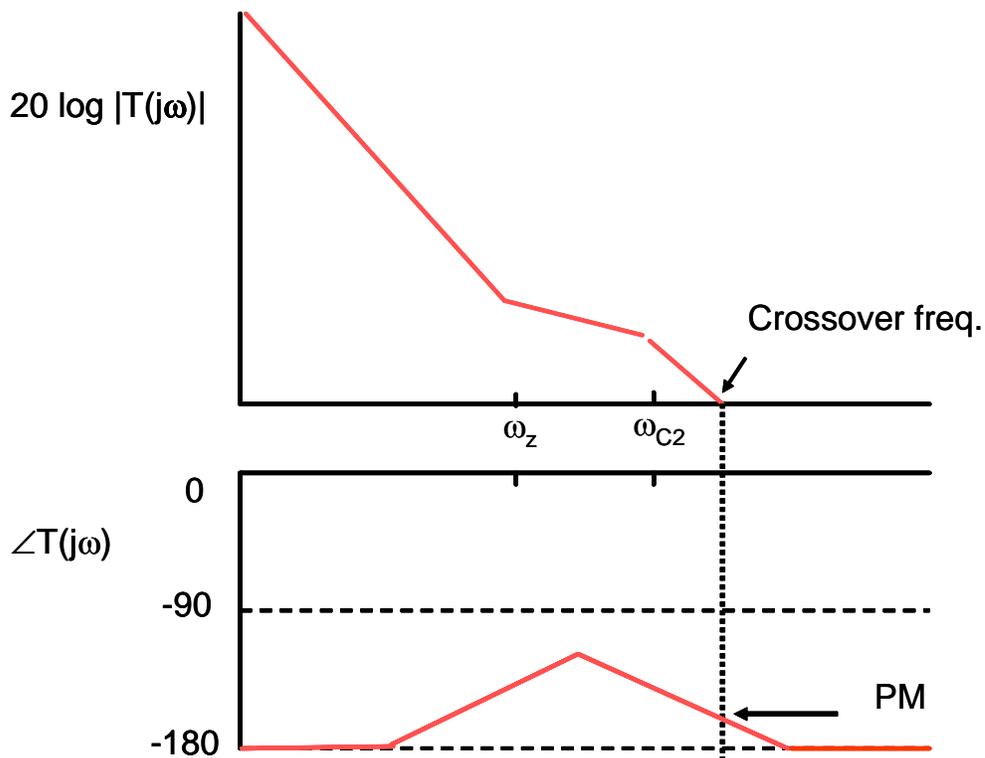
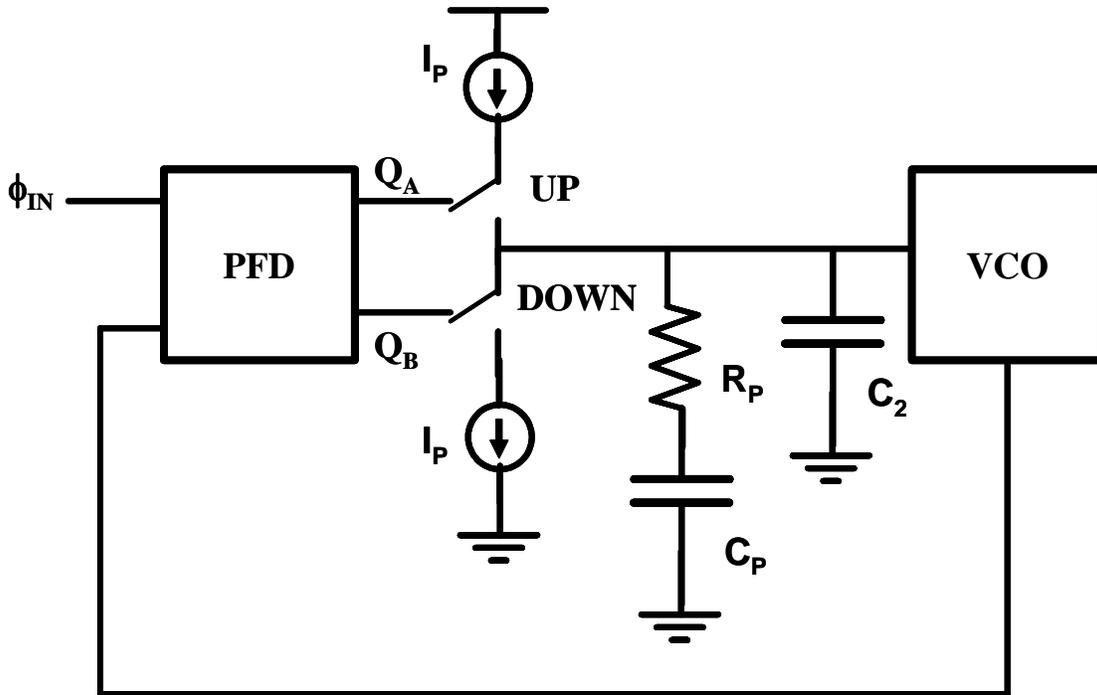
Third-order CP PLL

There is still one residual problem that we have overlooked. The phase detector produces pulses of variable width that activate the switches to either charge or discharge the capacitor C_p . Now that we have added the resistor, however, we find that the control voltage coming out of the charge pump will jump up or down before settling to its steady state value. This occurs because you cannot change the voltage across a capacitor instantaneously, so the initial voltage drop occurs across R_p , which then charges C_p exponentially. This jumpy control voltage frequency modulates the VCO at the reference frequency, creating reference spurs. This is not such a big problem if $N = 1$ because the jump will be at the same frequency as the VCO. But, at larger N values, it creates sidebands and jitter.

So, we need to fix this by adding a second capacitor, C_2 , whose function is to filter out the jumpy response of the series RC network. The magnitude of the reference spur sidebands is reduced by a factor of ω_{REF}/ω_{C2} . Unfortunately, however, C_2 adds a third

pole of finite frequency that will reduce the stability of the PLL. A look at the Bode plot verifies this.

$$\omega_{C2} = \frac{C_P + C_2}{R_P C_P C_2}$$



The pole frequency is given by R_p in parallel with the series combination of C_p and C_2 . Thus, the pole is always higher in frequency than the zero. We can see that the added pole reduces the phase margin. In fact, now when the loop gain is increased, phase margin is reduced. So, we must be careful that the pole frequency added by C_2 is much higher than the loop bandwidth.

$$\omega_{C_2} \gg 10 \omega_C$$

More on this later.....

PLL Phase Noise

We have considered how the bandwidth of the loop affects things like settling time and capture range. But it also plays a role in the PLL noise behavior.

For frequency synthesis, we are interested in low phase noise. There are at least 2 main sources:

1. reference noise – usually small since we frequently use a crystal oscillator
2. VCO noise – often high. We hope that the PLL will suppress most of the noise, at least close to the carrier.

The effect caused by each of these noise sources can be seen from the closed loop transfer functions.

Phase noise filtering by the PLL:

Reference Noise:

$$\begin{aligned}\frac{\phi_{out}}{\phi_{ref}} &= \frac{\text{Forward Path}}{1 + T(s)} = \frac{K_V F(s) / s}{1 + K_V F(s) / N s} \\ &= \frac{N(1 + s / \omega_2)}{N s^2 / K_V + s / \omega_2 + 1}\end{aligned}$$

This is a low pass transfer function. Its magnitude approaches N as s becomes small. Thus, reference phase noise is low pass filtered by the loop. Reference phase noise can be quite low when a crystal oscillator is used to generate the reference frequency. However, the phase noise gets multiplied by a factor of N for the integer N PLL.

$$\frac{\phi_{out}}{\phi_{ref}} = N$$

This is a serious limitation for large N values. There are better architectures to be used when small step size and low phase noise are both required.

VCO Noise:

$$\begin{aligned}\frac{\phi_{out}}{\phi_{vco}} &= \frac{\text{Forward Path}}{1 + T(s)} = \frac{1}{1 + K_V F(s) / N s} \\ &= \frac{N s^2 / K_V}{N s^2 / K_V + s / \omega_2 + 1}\end{aligned}$$

This is a high pass closed loop transfer function. It approaches a magnitude of 1 as s becomes large.

While LC VCOs can have low phase noise, they generally have smaller tuning range. RC or ring oscillator VCOs can be built with very wide tuning range but poor phase noise. The PLL can be used to clean up the VCO phase noise within the loop bandwidth. VCO phase noise is unattenuated at offset frequencies beyond the loop bandwidth.

Conclusions:

1. Reference input noise (reference source noise, data jitter, phase noise on FM input signal, etc.) sees a low-pass transfer function. It is passed through and multiplied by N . All we can do is try to avoid making it worse with our loop. A narrow bandwidth loop filter will help to suppress high frequency noise coming into the PLL from the reference port.
2. VCO jitter is suppressed by the PLL within the loop bandwidth. It has a high-pass transfer function. Thus, to suppress VCO noise, we want a large loop bandwidth.

Reference Spurs.

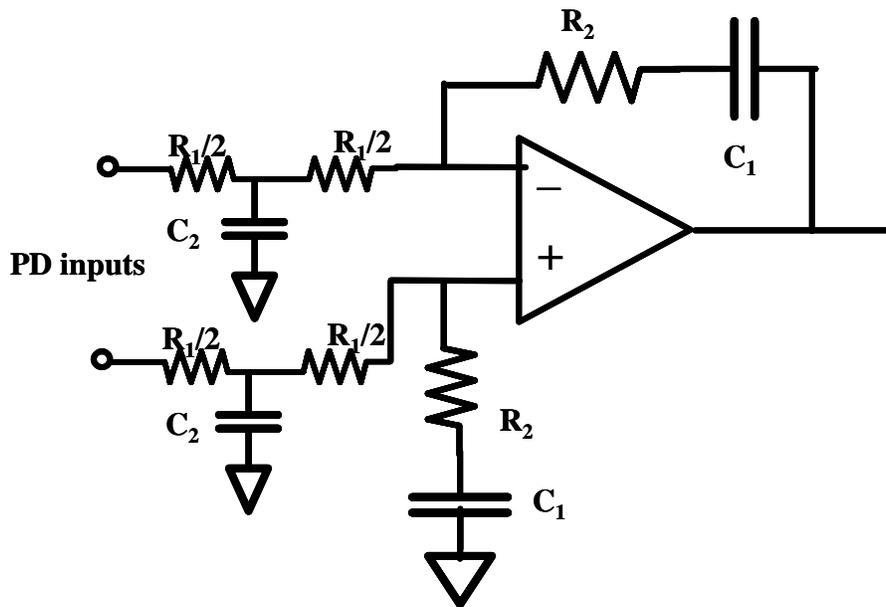
The Integer N PLL has an inherent conflict between the frequency step size (increment) and the settling time/bandwidth. The phase detector produces pulses that are at the reference frequency, f_R . These pulses are filtered by the loop lowpass filter, but not completely. Any residual reference frequency component on the VCO tuning voltage produces frequency modulation. Sidebands called reference spurs appear on both sides of the desired output spectral line spaced by f_R .

The natural frequency of the loop must be well below the reference frequency so that the reference frequency component is well attenuated by the loop filter.

$$\omega_n \leq \omega_R / 10$$

Since the settling time and loop bandwidth are directly affected by ω_n , we have conflicting requirements. Compromises must be made.

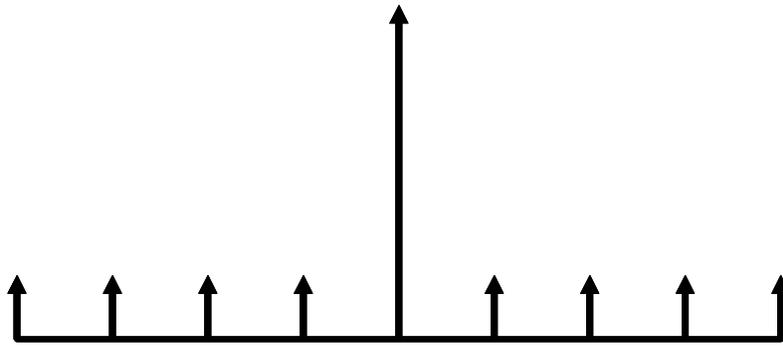
One approach to further reducing reference sidebands is to create a third order loop by adding another pole to the loop filter.



Resistor R1 has been split in half and capacitor C2 added to produce a finite pole at

$$\omega_{C2} = 4 / R_1 C_2.$$

This suppresses the reference spurs by a factor of ω_R / ω_{C2} at the expense of stability.



Reference sidebands (spurs)