A 21-mW 8-b 125-MSample/s ADC in 0.09-mm^2 0.13-μm CMOS

Jan Mulder, Christopher M. Ward, Chi-Hung Lin, David Kruse, Jan R. Westra, Marcel Lugthart, Erol Arslan, Rudy J. van de Plassche, *Fellow, IEEE*, Klaas Bult, *Member, IEEE*, and Frank M. L. van der Goes

***Abstract*—This paper presents an 8-b two-step subranging analog-to-digital (ADC) using interpolation, averaging, offset compensation, and pipelining techniques to accomplish an effective number of bits of 7.6 b at 125 MSample/s. The 0.13-μm CMOS ADC occupies 0.09 mm^2 and consumes 21 mW.**

***Index Terms*—Analog-to-digital conversion, CMOS analog integrated circuits (ICs), subranging analog-to-digital converter (ADC).**

I. Introduction

AREA and power are important parameters for analog-to-digital converters (ADCs) integrated on large digital ICs. This is especially true if several ADCs have to be implemented on the same die. These embedded ADCs necessarily have to be designed in state-of-the-art digital CMOS processes and, therefore, have to work at low supply voltages, while special process options, such as low-threshold devices, are often not available.

The ADC presented in this paper has 8-b resolution and samples at a rate of 125 MSample/s. Several ADC architectures are capable of achieving these specifications, e.g., flash ADCs [1], [2], pipeline ADCs [3]–[9], folding ADCs [10]–[17], and subranging ADCs [18]–[23]. However, when small die area and low-power and low-voltage operation are of primary importance, the two-step subranging architecture has proven to be a very suitable choice. A key advantage of this architecture is that the two-step approach allows for an area- and power-efficient design. Additionally, it can use simple differential-pair amplifiers, which are very well fit for low-voltage operation.

The basic architecture of the two-step subranging ADC, comprising a coarse ADC (CADC) and a fine ADC (FADC), is explained in Section II. The design of the CADC is described in Section III. Section IV first gives an overview of the FADC design, followed in Sections V–VIII by a detailed discussion of the techniques used in the FADC: offset compensation, pipelining, interpolation, and averaging, respectively. Section IX discusses the timing of the ADC. Finally, experimental results of the ADC, implemented in a 0.13-μm CMOS technology, are presented in Section X.

II. ADC Architecture

The ADC presented in this paper uses a two-step subranging architecture [24]–[28], shown in Fig. 1, comprising two flash ADCs, a reference ladder, a switch matrix, and an encoder. The subranging ADC is preceded by an on-chip track-and-hold (T/H). Each conversion cycle, the CADC first performs a rough quantization of the ADC input voltage. The switch matrix then connects the FADC to the appropriate subrange of the reference ladder, determined by the CADC. The FADC compares the ADC input voltage against the selected reference voltages and quantizes the input voltage at 8-b resolution. The digital encoder combines the CADC and FADC thermometer output code data into the final 8-b digital output code. Note that both the CADC and the FADC use the same reference ladder and the same T/H output signal. This guarantees matching of input and reference voltages between the two ADCs and saves chip area. A clock generator produces a nonoverlapping two-phase clock, used to clock the switches inside the T/H and the ADC. The two clock phases are denoted by ϕ_1 and ϕ_2, respectively.

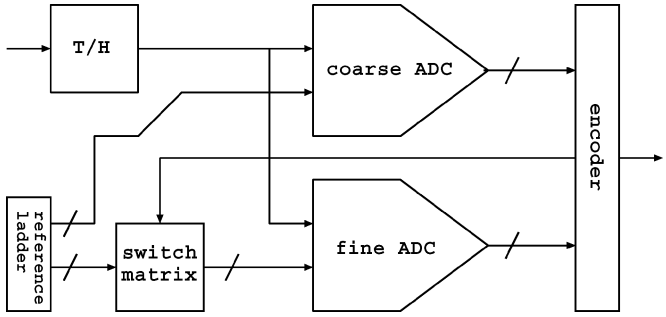


Fig. 1. Two-step subranging ADC architecture.

A minimum number of comparators is obtained when using both a 4-b CADC and a 4-b FADC. However, this requires the errors made by the CADC to be smaller than one least significant bit (LSB) of the FADC ($\mathrm{LSB_{FADC}}$).[1] It is not possible to accomplish this without excessive power consumption inside the CADC. It is, therefore, common practice to use some amount of over-range [18], [19], [25]–[27], [29], which allows the FADC to correct for errors of the CADC. If the CADC errors are smaller than the overrange, the overall ADC performance is only determined by the accuracy of the FADC and not by the CADC performance.

Overrange can be obtained by increasing the number of bits either in the CADC or in the FADC. An important restriction of the CADC is that its latency has to be low, because the CADC decision has to be available before the FADC can start to convert the input signal. In the FADC, latency is less important and

Manuscript received April 16, 2004; revised July 19, 2004.

The authors are with Broadcom Netherlands, 3981 AJ Bunnik, The Netherlands (e-mail: jmulder@broadcom.com).

Digital Object Identifier 10.1109/JSSC.2004.836235

[1]Note that this does not apply to the CADC quantization errors.

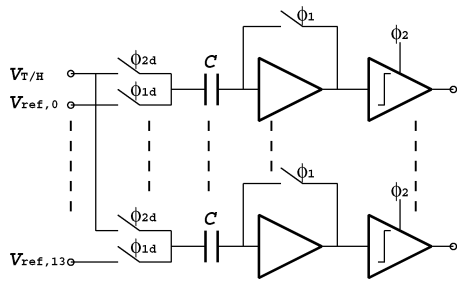


Fig. 2. Architecture of the CADC.

pipelining techniques can be used to decrease power consumption. Therefore, we preferred to increase the number of bits in the FADC.

The ADC presented here uses a 5-b FADC. On both sides of the 16 $\mathrm{LSB_{FADC}}$ nominal range, 8 $\mathrm{LSB_{FADC}}$ of overrange are available. The FADC can thus correct for CADC errors up to 8 $\mathrm{LSB_{FADC}}$, which is equivalent to 0.5 LSB of the CADC ($\mathrm{LSB_{CADC}}$).

III. Coarse ADC

The subranging ADC uses 15 subranges of 32 $\mathrm{LSB_{FADC}}$ to cover the complete 8 b output range. This requires 14 comparators in the CADC, which has been implemented as a full flash ADC. The offset requirements for the CADC are greatly relaxed by the 50% overrange implemented in the FADC. Therefore, only a single amplifier preceding each comparator is sufficient to reduce the impact of random comparator offsets. This is illustrated in Fig. 2. The amplifiers are auto-zeroed to reduce their offset contribution.

The amplifier used in the CADC is implemented using a cascoded differential pair with resistive load, as shown in Fig. 3. A fully differential implementation is used to achieve low sensitivity to substrate noise and achieve sufficient power supply rejection. The gates of the cascode transistors are connected directly to the positive supply V_{dd}. The reset switch, denoted by ϕ_1 in Fig. 2, is implemented by two single transistors. Since these transistors are applied in a feedback loop, they can be relatively small, thus introducing only a small amount of charge injection mismatch.

The input capacitors C of the CADC amplifiers serve several purposes. First of all, they are used to subtract the T/H output signal $V_{\mathrm{T/H}}$ from the reference voltages $V_{\mathrm{ref},i}$, where $i \in [0 \ldots 13]$. During clock phase ϕ_1, the capacitors are connected to $V_{\mathrm{ref},i}$; during the next half clock phase ϕ_2, they are connected to $V_{\mathrm{T/H}}$. As a result, the amplifier output voltages are proportional to $(V_{\mathrm{T/H}} - V_{\mathrm{ref},i})$. The charge injection from the reset switches (ϕ_1) is signal-*independent*. Since the charge injection from the switches connecting to the T/H and the reference ladder, denoted by $\phi_{1\mathrm{d}}$ and $\phi_{2\mathrm{d}}$ in Fig. 2, is signal-*dependent*, bottom-plate sampling is used in the CADC to improve performance [21]. That is, at the end of the reset phase, switch ϕ_1 opens slightly before $\phi_{1\mathrm{d}}$ opens.

Second, the input capacitors are used for offset compensation of the amplifiers. This allows the use of relatively small active devices, reducing the power consumption of the amplifiers. To auto-zero an amplifier, the reset switch is closed for half a clock cycle. During this time, (most of) the amplifier offset is stored on the input capacitor. The amplifier offset is reduced by approximately a factor $A_v = g_{\mathrm{m}} R_{\mathrm{load}}$, where g_{m} is the transconductance of the differential-pair transistors and R_{load} is the value of the load resistors. To increase the voltage gain A_v of the amplifier, current sources are used in parallel to the load resistors (Fig. 3). Note that the higher gain also decreases the offset contribution of the comparators.

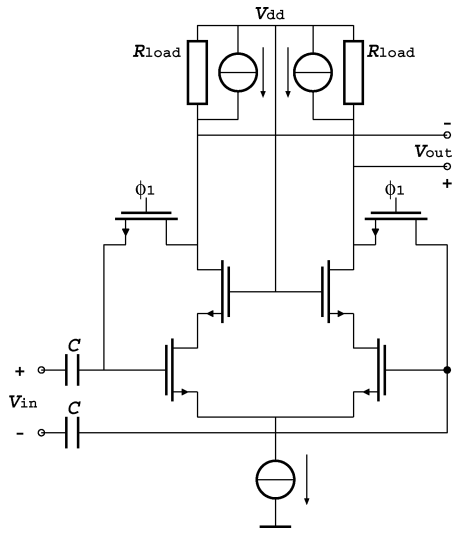


Fig. 3. Schematic of the amplifier used in the CADC.

Finally, the input capacitors allow the independent optimization of the T/H common-mode output voltage and the differential-pair common-mode input voltages.

IV. Fine ADC

The FADC, shown in Fig. 4, is a 5-b flash ADC comprising of an array of 33 comparators. It provides 50% of overrange, which enables the ADC to correct for inaccuracies of the CADC of up to 8 $\mathrm{LSB_{FADC}}$ without any impact on the overall ADC performance. The comparators are preceded by three arrays of differential-pair amplifiers, denoted by A, B, and C, respectively, which are required to suppress the random offsets of the comparators.

Fig. 5 illustrates the operation principle of the FADC. The input capacitors of stage A are used to subtract $V_{\mathrm{T/H}}$ from the reference voltages $V_{\mathrm{ref},i}$. Bottom-plate sampling is used to improve the accuracy of the FADC, as in the CADC. Further, the dc-level shift provided by these capacitors allows the independent optimization of the T/H common-mode output voltage and the differential-pair common-mode input voltages.

To improve the performance and reduce the area and power consumption, the FADC employs offset compensation, pipelining, interpolation, and averaging. The application of these techniques is discussed in the following four sections.

V. Offset Compensation

The FADC uses offset compensation in all three amplifier arrays. As a consequence, small devices can be used in the differential-pair amplifiers, allowing the use of lower bias currents, which helps to reduce the power consumption of the FADC.

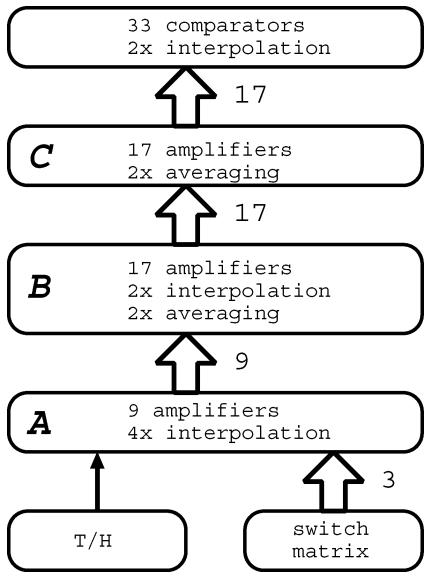


Fig. 4. Block diagram of the FADC.

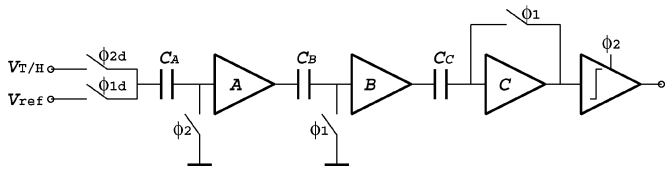


Fig. 5. Operation principle of the FADC.

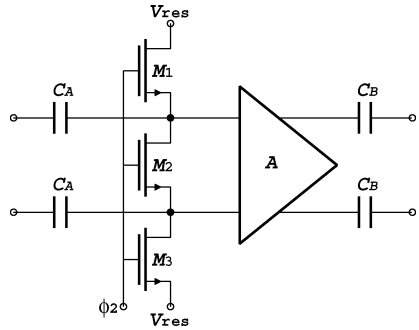


Fig. 6. Simplified schematic of the reset switches in array A and B of the FADC.

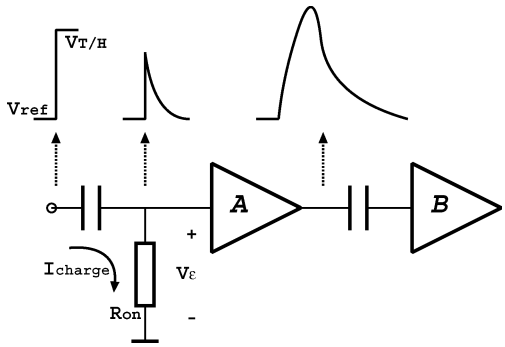


Fig. 7. Effect of finite on-resistance of the reset switches at high conversion rates.

The amplifiers in stage C use a *closed-loop* auto-zero technique, identical to the one used in the CADC. In contrast, array A and B use an *open-loop* auto-zero technique [25], [30]. Fig. 6 shows the basic implementation of the reset switches in array A and B. When an amplifier in row A is being reset during clock phase ϕ_2, switch M_2 shorts the inputs of the differential pair, while switches M_1 and M_3 connect them to a dc bias voltage $V_{\rm res}$. The output-referred offset voltage $V_{{\rm out},\phi_2} = V_{\rm offset}$ is then stored on the input capacitors C_B of the following stage B. During the next clock phase ϕ_1, the output voltage $V_{{\rm out},\phi_1}$ is a superposition of a signal voltage $V_{\rm signal}$ and the offset voltage, i.e., $V_{{\rm out},\phi_1} = V_{\rm signal} + V_{\rm offset}$. The input capacitor of stage B subtracts the two output voltages $V_{{\rm out},\phi_1}$ and $V_{{\rm out},\phi_2}$, thus eliminating $V_{\rm offset}$. In stages A and B, the differential-pair input signals are sufficiently small to allow this open-loop auto-zero technique, which heavily relies on amplifier linearity, to be used. Note that the switches involved in auto-zeroing the amplifiers introduce another source of mismatch: charge-injection mismatch. Averaging is used to minimize this offset contribution, as will be explained in Section VIII.

VI. Pipelining

In ADCs comprising cascaded arrays of amplifiers, pipelining is often used to improve conversion speed [15], [20], [26], [31], [32]. In effect, conversion latency is traded against amplifier speed and, hence, power consumption. Since, in this design, coupling capacitors between the amplifier arrays are already implemented in the FADC for auto-zeroing purposes, they can be reused for pipelining.

It is not necessarily optimal to operate all three amplifier arrays in alternating clock phases, because the capacitive loading of an amplifier depends on the clock phase of the subsequent amplifier. If the subsequent stage is in reset mode, the coupling capacitor between the stages is (virtually) grounded. Hence, the capacitive loading is high, and the amplifier speed low. If the next stage is in amplify mode, the interstage capacitor is floating, resulting in lower output capacitance and, hence, higher amplifier speed. In this design, row A is auto-zeroed in clock phase ϕ_2, while B and C are auto-zeroed during clock phase ϕ_1, as shown in Fig. 5.

The finite on-resistance of switches M_1, M_2, and M_3, shown in Fig. 6, is a major problem at high sampling rates. This is illustrated in Fig. 7. During clock phase ϕ_2, amplifier A is in reset mode and samples $V_{\rm T/H}$. The current $I_{\rm charge}$ charging the input capacitor gives rise to a nonzero voltage V_ϵ at the input of A that settles exponentially down to zero. This error voltage is amplified by amplifier A and spread out in time, because of the finite speed of A. Because the FADC uses pipelining, amplifier B is in amplify mode and therefore further amplifies the error voltage. As a consequence, the error ripples through the complete FADC. Eventually, all error voltages settle to zero, but they considerably limit the maximum conversion speed of the FADC.

Fig. 8 shows an implementation of the reset switches in row A and B that significantly improves the pipelining operation in the FADC at high conversion rates. In reset mode, when all switches are turned on, the on-resistance of switches M_4–M_7 is equal. Switches M_4 and M_6 form a resistive divider, the output of which is a *common-mode* voltage. The same applies to M_5 and M_7. As a consequence, the *differential-mode* error

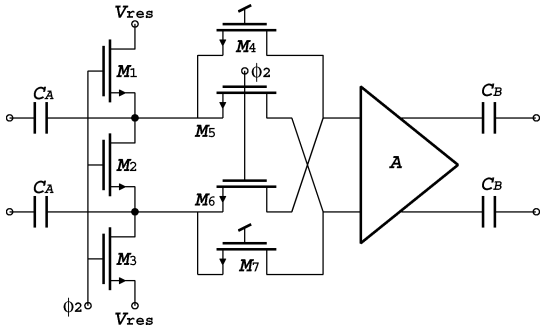


Fig. 8. Implementation of the reset switches in array A and B of the FADC.

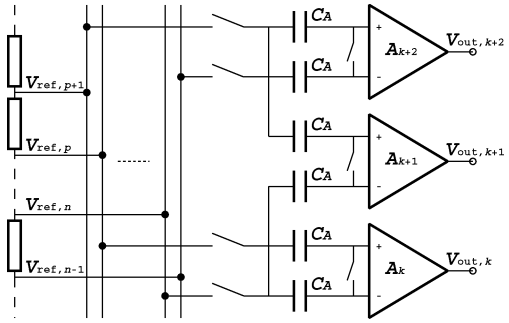


Fig. 9. Implementation of 2× interpolation of the reference ladder voltages.

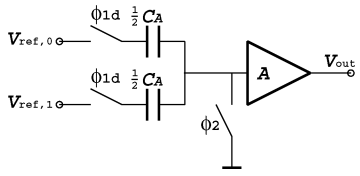


Fig. 10. Implementation of another 2× capacitive interpolation of the reference ladder voltages.

voltage developing across the drain and source terminal of M_2 is not transferred to the gates of the differential-pair amplifier. In other words, the differential-mode transfer function of these cross-coupled switches equals zero in reset mode. During amplify mode, when only M_4 and M_7 are turned on, the differential-mode transfer function equals one. The fact that the error voltage no longer ripples through the complete FADC significantly improves the maximum conversion rate of the ADC.

The cross-coupled switches introduce some additional noise and charge-injection mismatch, which have only a small influence on the FADC performance in this design.

VII. Interpolation

Interpolation is generally used to reduce the number of amplifiers required in an ADC [10], [12]–[17], [20], [21], [27]–[29], [33]–[37], thus decreasing layout complexity, which is imperative for achieving small die area and low-power operation. Moreover, interpolation reduces the number of reference voltages required, so less signals have to be routed in the layout. This helps to achieve a small area, and, because of less parasitic capacitance, it also reduces the power consumption of the ADC. Additionally, in subranging ADCs, interpolation reduces the number of switches required in the switch matrix [27]. Since the switch matrix represents a significant capacitive load to the T/H (through switch $\phi_{2\mathrm{d}}$, shown in Fig. 5) and the reference ladder, interpolation indirectly helps to reduce the power consumption of the T/H and the reference ladder.

The subranging ADC presented here not only applies interpolation in the FADC amplifier arrays, but also introduces *interpolation of the reference ladder*, which allows for a further reduction of the number of reference voltages and switches. The 4× interpolation implemented in the FADC (see Fig. 4) reduces the required number of taps on the reference ladder by 4×, from 256 to 64 taps. Routing 64 reference voltages, however, is still quite impractical in a small layout. Furthermore, although the number of switches needed in the switch matrix has also been reduced by 4×, it is still rather high. By introducing interpolation of the reference ladder, both the number of reference taps and the number of switches can be further reduced. This design implements a 4× interpolation of the reference ladder voltages. As a result, only 17 reference voltages are required. In addition, the number of switches reduces by another factor of 4× as well, allowing for a much more area-efficient layout of the switch matrix.

The implementation of the interpolation of the reference ladder is discussed first in Section VII-A. Next, the interpolation implemented in the FADC is described in Section VII-B.

A. Reference Ladder Interpolation

The ADC uses two different capacitive interpolation techniques, each providing 2× interpolation of the reference ladder voltages.

The first interpolation technique, illustrated in Fig. 9, provides 2× interpolation of the reference ladder. The bottom amplifier A_k uses reference taps $V_{\mathrm{ref},p}$ and $V_{\mathrm{ref},n}$ to create a differential reference voltage equal to $(V_{\mathrm{ref},p} - V_{\mathrm{ref},n})$. Likewise, the differential reference voltage of the top amplifier A_{k+2} equals $(V_{\mathrm{ref},p+1} - V_{\mathrm{ref},n-1})$. Now, the middle amplifier A_{k+1} can reuse the same reference taps to create an interpolated differential reference voltage. This can be done in two ways: either $(V_{\mathrm{ref},p+1} - V_{\mathrm{ref},n})$, which is depicted in Fig. 9, or $(V_{\mathrm{ref},p} - V_{\mathrm{ref},n-1})$ can be used, both resulting in the same differential reference voltage. Note that the common-mode voltages of these interpolated reference voltages are not equal to the common-mode voltage of noninterpolated reference voltages. Fortunately, the common-mode differences are sufficiently small, i.e., $\pm 2\mathrm{LSB}_{\mathrm{FADC}}$ in this design, to be handled by the amplifiers in row A.

The second interpolation technique is shown in Fig. 10, where the input capacitors in row A are reused to implement another 2× capacitive interpolation. Each original capacitor C_A is replaced by two capacitors with half the size. During clock phase ϕ_1, when array A is in amplify mode, the two capacitors are connected to reference voltages $V_{\mathrm{ref},0}$ and $V_{\mathrm{ref},1}$. As a result, after redistribution of the charge on the two capacitors, an intermediate reference voltage V'_{ref} equal to $(1/2)(V_{\mathrm{ref},0} + V_{\mathrm{ref},1})$ is applied to the amplifier.

B. FADC Interpolation

The FADC uses active interpolation, implemented by the circuit shown in Fig. 11. By combining the output currents of two

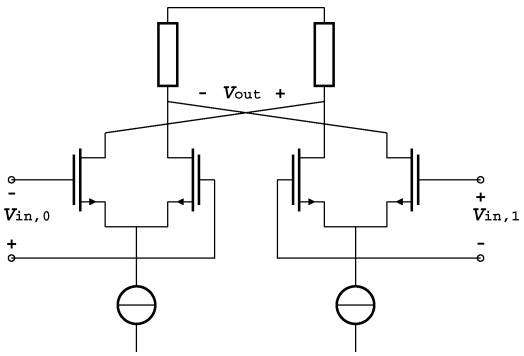


Fig. 11. Simplified schematic of a differential-pair amplifier providing 2× interpolation.

differential pairs, with input voltages $V_{\mathrm{in},0}$ and $V_{\mathrm{in},1}$, respectively, an output voltage V_{out} is obtained that is proportional to the average of $V_{\mathrm{in},0}$ and $V_{\mathrm{in},1}$, i.e., $V_{\mathrm{out}} \sim (1/2)(V_{\mathrm{in},0} + V_{\mathrm{in},1})$.

In this design, a total of 4× active interpolation is used in the FADC. The first 2× interpolation is implemented in the amplifiers of row B. Since it is difficult to implement active interpolation in row C, because of the closed-loop auto-zero method used in that array, the second 2× is implemented in the differential-pair input stage of the FADC comparators. This brings the total number of amplifiers in each array to 9, 17, and 17, respectively (see Fig. 4).

VIII. Averaging

Averaging is widely used in flash ADCs [38]–[40], folding ADCs [16], [17], [35], [41]–[43], and subranging ADCs [26] to improve ADC performance. In an array of amplifiers, the contributions of random mismatch and noise to the output signals of neighboring amplifiers are mostly uncorrelated. Hence, when averaging the outputs of several amplifiers, the average output signal has a higher signal-to-noise ratio (SNR) than the individual output signals.

Although this subranging ADC design already implements offset compensation, averaging still has a beneficial influence on the performance. First of all, averaging helps to decrease the influence of noise generated in the amplifiers and switches. Secondly, the switches, required for auto-zeroing and pipelining, introduce random mismatches themselves, which cannot be auto-zeroed. Averaging decreases this charge-injection mismatch. As a result, amplifier bias levels and capacitor sizes can be reduced, which reduces both power consumption and chip area.

A potential drawback of averaging is the sensitivity to gain mismatches of the amplifiers in an array. In practice, gain mismatch is mainly due to mismatch of the tail current sources used in the differential-pair amplifiers. Fortunately, the transistor used to implement the tail current source does not have significant influence on the amplifier speed. Hence, a relatively large active area can be used for this transistor to improve gain matching [32].

The capacitors already present between arrays A, B, and C can be reused to implement 2× capacitive averaging. As shown in Fig. 12, the input capacitors of row B and C are split into two equal halves, connecting to two different input voltages $V_{\mathrm{in},0}$ and $V_{\mathrm{in},1}$. When the amplifier is in reset mode, the capacitors are

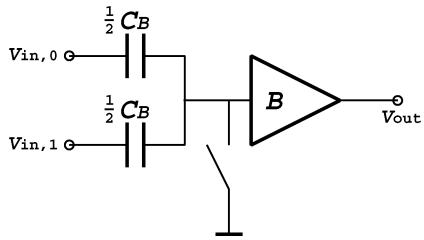


Fig. 12. Implementation of 2× capacitive averaging.

charged to $V_{\mathrm{in},0}$ and $V_{\mathrm{in},1}$, respectively. During amplify mode, the charges on the capacitors are redistributed and an output voltage V_{out} results that is proportional to the average value of $V_{\mathrm{in},0}$ and $V_{\mathrm{in},1}$, i.e., $V_{\mathrm{out}} \sim (1/2)(V_{\mathrm{in},0} + V_{\mathrm{in},1})$. A key advantage of this averaging implementation is that the resulting "averaging window" covers a finite number of amplifiers. This reduces the edge effects that usually occur due to the necessarily limited number of amplifiers in each array [40]. Further, the inaccuracies of amplifiers outside this averaging window do not affect the accuracy of the signal.

Note that, in this implementation of averaging, 2× averaging is essentially the same as 2× interpolation. The only difference is that it is not used here to decrease the number of amplifiers in the FADC, as described in Section VII-B, but merely to increase the SNR of the signals inside the FADC.

Of all three amplifier arrays, the amplifiers in A are most important with respect to the ADC performance. Therefore, it would be beneficial if, e.g., 4× averaging of the A amplifiers could be achieved, instead of the 2× provided by the circuit shown in Fig. 12. One possible implementation is to split the input capacitors of row B into four equal parts, instead of two, and connect them to the outputs of four consecutive amplifiers in row A. This approach has some major disadvantages. First of all, the input capacitors in row B would become inconveniently small, resulting in an increase of parasitic capacitance. Second, quite some signal routing would be required at the output of array A, again introducing more parasitic capacitance.

A solution was found in the distributed averaging topology shown in Fig. 13. Although using only two capacitors at each differential-pair input, instead of four, 4× averaging of the A amplifiers is achieved. This is accomplished by "skipping" one A amplifier when connecting the two inputs of an amplifier in B to the outputs of two amplifiers in A. The black-colored amplifiers demonstrate that this topology can indeed achieve 4× averaging of the A amplifiers. Suppose that the FADC input signal, after quantization, is located halfway between the inputs of amplifiers A_1 and A_2, then the "zero-crossing" at the output of C_1 is determined by amplifiers A_0, A_1, A_2, and A_3 in array A, amplifiers B_1 and B_2 in array B, and amplifier C_1 in array C. It can be easily derived that all amplifiers within the averaging window of array A are equally weighted. The same applies to row B.

IX. Timing

A crucial point in the design of a subranging ADC is the timing between the CADC and the FADC. The FADC needs to wait for the digital output of the CADC to become available before it can start to convert the input signal. Because it is difficult

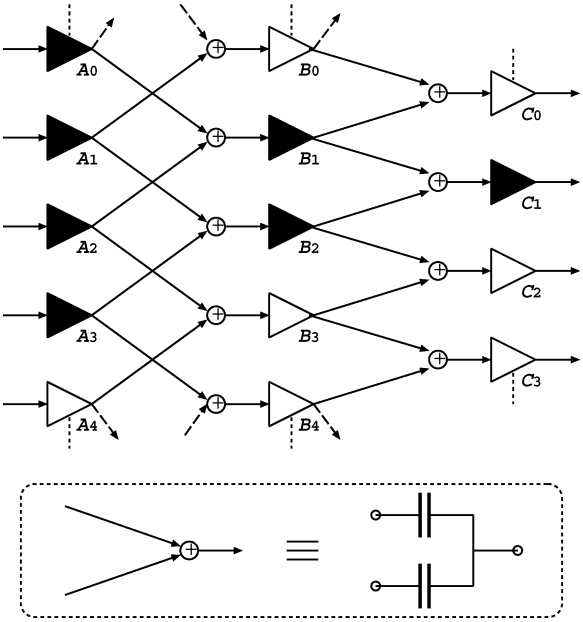


Fig. 13. Distributed averaging topology, providing 4× and 2× averaging of the amplifiers in array A and B, respectively.

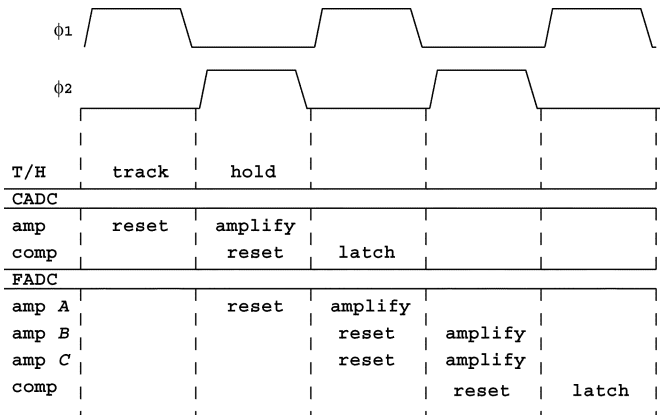


Fig. 14. Timing diagram of the ADC.

to delay the input signal going to the FADC, the CADC needs to have low latency.

Fig. 14 illustrates the timing of the CADC and the FADC in this design. The CADC amplifiers and the FADC amplifiers in row A are being reset during different clock phases ϕ_1 and ϕ_2, respectively. Consequently, the latency of the FADC is increased by half a clock cycle with respect to the CADC. This half clock cycle is now available for the CADC to quantize the input signal.

A conversion starts during clock phase ϕ_1 when the CADC amplifiers are in reset mode and store the reference voltages on their input capacitors. Meanwhile, the T/H is in track mode.

Next, during phase ϕ_2, the T/H is in hold mode and the CADC amplifiers connect to the T/H output. Since the amplifiers are in amplify mode, they directly amplify the residue voltages $(V_{\mathrm{T/H}} - V_{\mathrm{ref},i})$. At the same time, the amplifiers in array A of the FADC are in reset mode and store the T/H output signal on their input capacitors. Note that, since the T/H output signal is only available for half a clock cycle, both the CADC and the FADC have to connect to the T/H during the same clock phase ϕ_2.

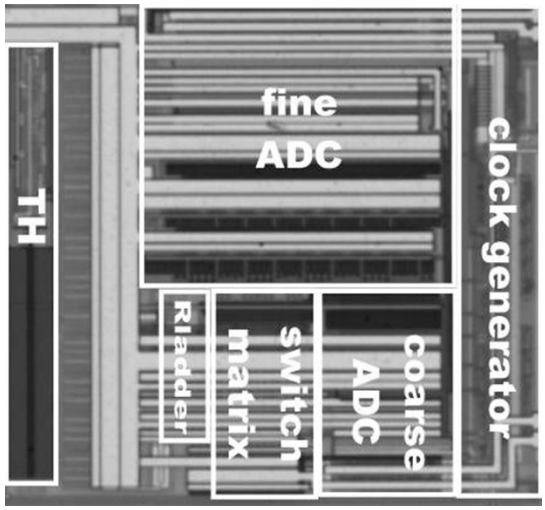


Fig. 15. Microphotograph of the ADC.

At an early version of the falling edge of phase ϕ_2, the comparators in the CADC start to latch, so the digital output of the CADC will be available during the following clock phase ϕ_1, where it is needed to connect the FADC amplifiers in row A to the correct subset of reference voltages. Note that the time available for the comparators in the CADC to latch is much shorter than half a clock cycle. Simulations were used to verify that the comparators in the CADC are fast enough to have finished latching before the start of phase ϕ_1. Further, if, due to metastability, a CADC comparator needs more time to latch, this does not directly lead to a bit error, but just eats into the available settling time for the FADC.

During phase ϕ_1, the amplifiers in array A are in amplify mode and process the residue voltages. The FADC uses pipelining, as described in Section VI, so the amplifiers in row B and C process the signal during the next clock phase ϕ_2.

The FADC comparators finally quantize the signal in the subsequent phase ϕ_1. Next, the encoder combines the output data from the FADC and the delayed output data from the CADC to construct the 8-b digital output signal.

X. Experimental Results

The ADC was fabricated in a 0.13-μm CMOS process. A die microphotograph is shown in Fig. 15. The ADC occupies only 290 μm × 316 μm = 0.09 mm^2, including the on-chip T/H and clock generator circuit.

The reference ladder is implemented as a 390-μm-long continuous strip of poly silicon. In order to fit in the layout, the reference resistor had to be folded at least once. For symmetry with respect to the 17 reference taps, it was folded eight times. An additional benefit is that the routing of the reference voltages to the CADC and switch matrix can be shorter, which reduces parasitic capacitance [14].

Table I summarizes the ADC performance, measured at a clock frequency f_{clk} of 125 MS/s, at 90% ADC output loading, and using a single-tone input signal f_{in} of 8 MHz.

The performance of the CADC does not influence the performance of the overall ADC, under the condition that the errors made by the CADC are smaller than 0.5 $\mathrm{LSB}_{\mathrm{CADC}}$. Fig. 16

TABLE I
PERFORMANCE SUMMARY

Resolution	8bit
Conversion rate	125MSample/s
Process	0.13μm CMOS
Power supplies	1.2V / 2.5V
Power	21mW
Area	0.09mm^2
ENOB	7.6bits
SNR	7.7bits
THD	9.7bits
ERBW	$>$ 100MHz
INL	$<$ 0.25LSB
DNL	$<$ 0.15LSB

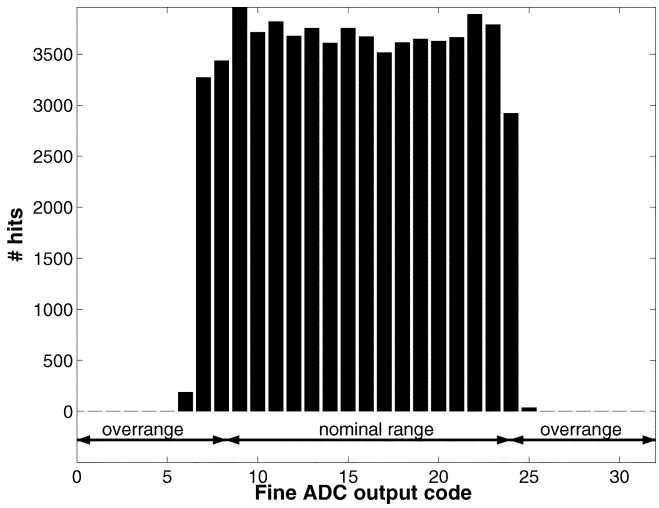


Fig. 16. Measured histogram of FADC output codes.

shows that this condition is easily met in this design. The histogram of FADC output codes, available in a special test mode, shows that only codes 6–25 occur. Therefore, the ADC has a margin of 6 and 7 $\mathrm{LSB_{FADC}}$ on the low end and high end of the FADC range, respectively, out of the 8 $\mathrm{LSB_{FADC}}$ available at each end.

Fig. 17 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) curves of the ADC, measured at $f_{\mathrm{clk}} = 125$ MS/s. The INL is smaller than ± 0.25 b and the DNL is smaller than ± 0.15 b.

Fig. 18 shows a clock sweep using an 8-MHz input signal. The effective number of bits (ENOB) of the ADC equals 7.6 b at 125 MS/s, dropping half a bit to 7.1 b at 220 MS/s. At 125 MS/s, the SNR equals 7.7 b and the total harmonic distortion (THD) (including the second through tenth harmonic) is 9.7 b.

Fig. 19 shows an input signal frequency sweep at 125 MS/s. The effective resolution bandwidth (ERBW) exceeds 100 MHz.

Fig. 20 shows the ADC output spectrum. The spurious-free dynamic range (SFDR) is 68 dB.

The total power consumption P equals 21 mW, including T/H and clock generator, but excluding the digital output buffers. The power consumption is approximately equally divided between the T/H, the clock generator, and the ADC. The energy per conversion step is often used as a figure of merit (FOM) F, defined as $F = P/(2^{\mathrm{ENOB}} \times 2\,\mathrm{ERBW})$, and, for this design,

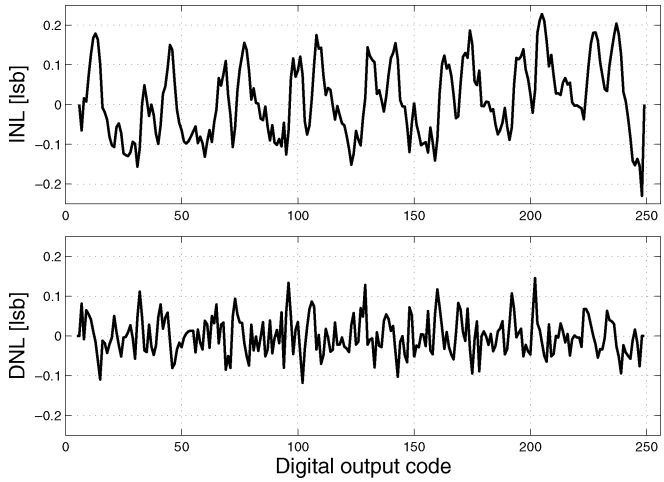


Fig. 17. Measured INL and DNL.

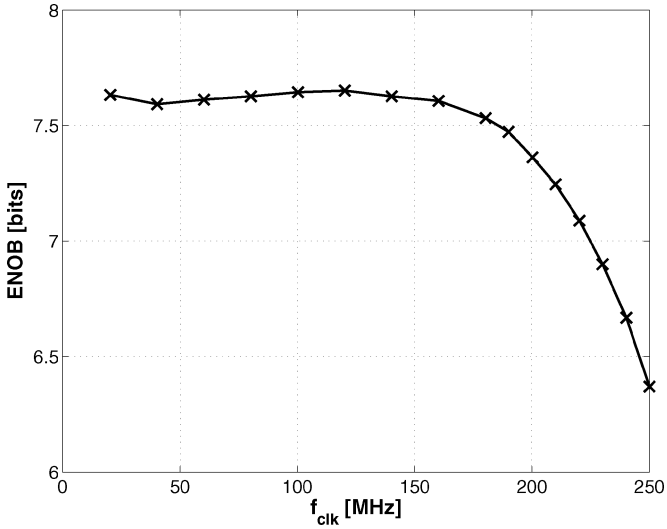


Fig. 18. Measured ADC performance versus f_{clk} at $f_{\mathrm{in}} = 8$ MHz.

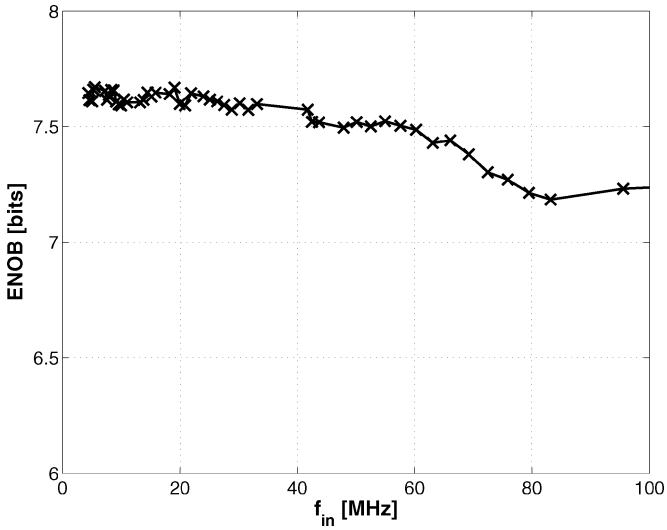


Fig. 19. Measured ADC performance versus f_{in} at $f_{\mathrm{clk}} = 125$ MSample/s.

equals 0.54 pJ/conversion at 125 MS/s. For comparison, Table II lists the area and FOM of this design together with a number of

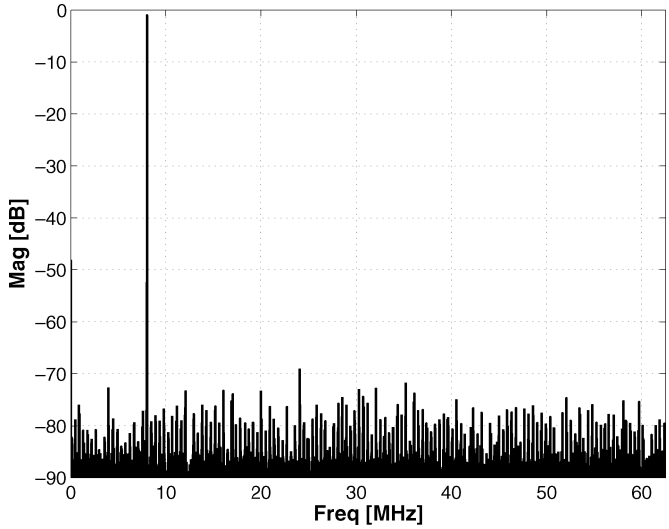


Fig. 20. Measured output spectrum of the ADC.

TABLE II
PERFORMANCE COMPARISON

Ref.	Technology	area [mm^2]	F [pJ/conv]
[20]	0.6μm	1.8	88
[15]	0.5μm	1.7	794
[6]	0.5μm	10	7934
[14]	0.35μm	0.8	529
[21]	0.35μm	0.9	30
[9]	0.18μm	1.8	2.5
This work.	0.13μm	0.09	0.54

recently published 8-b Nyquist CMOS ADCs running at comparable sampling frequencies. This shows that this design achieves best results for both area and FOM.

XI. CONCLUSION

The subranging ADC architecture uses simple differential-pair amplifiers, which makes it very suitable for low-voltage operation, required in state-of-the-art CMOS processes. The application of several techniques, such as active interpolation, pipelining, auto-zero offset compensation, and distributed capacitive averaging, resulted in an 8-b ADC design consuming only 21 mW, while sampling at 125 MS/s, and requiring no more than 0.09 mm^2 of area in a 0.13-μm CMOS process. The measured performance was 7.6 ENOB, with an effective resolution bandwidth greater than 100 MHz.

REFERENCES

[1] Y. Yoshii, K. Asano, M. Nakamura, and C. Yamada, "An 8 bit, 100 MS/s flash ADC," *IEEE J. Solid-State Circuits*, vol. SSC-19, pp. 842–846, Dec. 1984.

[2] A. Matsuzawa, Y. Kitagawa, I. Hidaka, S. Sawada, M. Kagawa, and M. Kanoh, "An 8 b 600 MHz flash A/D with multistage duplex Gray coding," in *Proc. VLSI Circuits Symp.*, 1991, pp. 113–113.

[3] C. S. G. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85-MS/s parallel pipeline A/D converter in 1-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 28, pp. 447–454, Apr. 1993.

[4] W. Bright, "8 b 75 MSample/s 70 mW parallel pipelined ADC incorporating double sampling," in *ISSCC Dig. Tech. Papers*, 1998, pp. 146–147.

[5] K. Irie, N. Kusayanagi, T. Kawachi, T. Nishibu, and Y. Matsumori, "An 8 b 500 MS/s full Nyquist cascade A/D converter," in *Proc. VLSI Circuits Symp.*, 1999, pp. 77–78.

[6] J. Ming and S. H. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1489–1497, Oct. 2001.

[7] K. Poulton, R. Neff, A. Muto, W. Liu, A. Burstein, and M. Heshami, "A 4 GSample/s 8 b ADC in 0.35 μm CMOS," in *ISSCC Dig. Tech. Papers*, 2002, pp. 166–167.

[8] K. Poulton, R. Neff, N. Setterberg, B. Wuppermann, T. Kopley, R. Jewett, J. Pernillo, C. Tan, and A. Montijo, "A 20 GSample/s 8 b ADC with 1 MB memory in 0.18 μm CMOS," in *ISSCC Dig. Tech. Papers*, 2003, pp. 318–319.

[9] S. Limotyrakis, S. D. Kulchycki, D. Su, and B. A. Wooley, "A 150 MS/s 8 b 71 mW time-interleaved ADC in 0.18 μm CMOS," in *ISSCC Dig. Tech. Papers*, 2004, pp. 258–259.

[10] B. Nauta and A. G. W. Venes, "An 70-MS/s 110-mW 8-b CMOS folding and interpolating A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1302–1308, Dec. 1995.

[11] C. W. Moreland, "An 8 b 150 MSample/s serial ADC," in *ISSCC Dig. Tech. Papers*, 1995, pp. 272–273.

[12] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1846–1853, Dec. 1996.

[13] M. P. Flynn and D. J. Allstot, "CMOS folding A/D converters with current-mode interpolation," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1248–1257, Sept. 1996.

[14] K. Yoon, J. Lee, D.-K. Jeong, and W. Kim, "An 8-bit 125 MS/s CMOS folding ADC for Gigabit Ethernet LSI," in *Proc. VLSI Circuits Symp.*, 2000, pp. 212–213.

[15] M.-J. Choe, B.-S. Song, and K. Bacrania, "An 8-b 100-MSample/s CMOS pipelined folding ADC," *IEEE J. Solid-State Circuits*, vol. 36, pp. 184–194, Feb. 2001.

[16] G. Geelen and E. Paulus, "An 8 b 600 MS/s 200 mW CMOS folding A/D converter using an amplifier preset technique," in *ISSCC Dig. Tech. Papers*, 2004, pp. 254–255.

[17] R. Taft, C. Menkus, M. R. Tursi, O. Hidri, and V. Pons, "A 1.8 V 1.6 GS/s 8 b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," in *ISSCC Dig. Tech. Papers*, 2004, pp. 252–253.

[18] Y. Nishida, K. Sone, K. Amano, S. Matsuba, and A. Yukawa, "An 8-bit 200 MS/s 500 mW BiCMOS ADC," in *Proc. Custom Integrated Circuits Conf.*, 1995, pp. 207–210.

[19] M. Sugawara, Y. Yoshida, M. Mitsuishi, S. Nakamura, S. Nakaigawa, Y. Kunisaki, and H. Suzuki, "A 2.5 V 100 MS/s 8 bit ADC using prelinearization input buffer and level up DAC/subtractor," in *Proc. VLSI Circuits Symp.*, 1998, pp. 170–173.

[20] Y.-T. Wang and B. Razavi, "An 8-bit 150-MHz CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. 35, pp. 308–317, Mar. 2000.

[21] R. C. Taft and M. R. Tursi, "A 100-MS/s 8-b CMOS subranging ADC with sustained parametric performance from 3.8 V down to 2.2 V," *IEEE J. Solid-State Circuits*, vol. 36, pp. 331–338, Mar. 2001.

[22] R. C. Taft, M. R. Tursi, and A. Glenny, "Design techniques for very low power ADC's," in *Proc. Custom Integrated Circuits Conf.*, 2001, pp. 141–144.

[23] J. Mulder, C. M. Ward, C.-H. Lin, D. Kruse, J. R. Westra, M. L. Lugthart, E. Arslan, R. van de Plassche, K. Bult, and F. M. L. van der Goes, "A 21 mW 8 b 125 MS/s ADC occupying 0.09 mm^2 in 0.13 μm CMOS," in *ISSCC Dig. Tech. Papers*, 2004, pp. 260–261.

[24] A. G. F. Dingwall and V. Zazzu, "An 8-MHz CMOS subranging 8-bit A/D converter," *IEEE J. Solid-State Circuits*, vol. SSC-20, pp. 1138–1143, Dec. 1985.

[25] T. Matsuura, H. Kojima, E. Imaizumi, K. Usui, and S. Ueda, "An 8-b 50-MHz 225-mW submicron CMOS ADC using saturation eliminated comparators," in *Proc. Custom Integrated Circuits Conf.*, 1990, pp. 641–644.

[26] K. Kusumoto, A. Matsuzawa, and K. Murata, "A 10-b 20-MHz 30-mW pipelined interpolating CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1200–1206, Dec. 1993.

[27] B. P. Brandt and J. Lutsky, "A 75-mW, 10-b, 20-MSPS CMOS subranging ADC with 9.5 effective bits at Nyquist," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1788–1795, Dec. 1999.

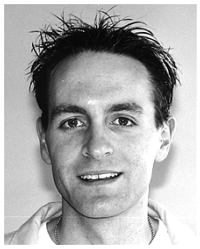
[28] H. van der Ploeg, G. Hoogzaad, H. A. H. Termeer, M. Vertregt, and R. L. J. Roovers, "A 2.5-V 12-b 54-Msample/s 0.25-μm CMOS ADC in 1-mm^2 with mixed-signal chopping and calibration," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1859–1867, Dec. 2001.

[29] M. Clara, A. Wiesbauer, and F. Kuttner, "A 1.8 V fully embedded 10 b 160 MS/s two-step ADC in 0.18 μm CMOS," in *Proc. Custom Integrated Circuits Conf.*, 2002, pp. 437–440.

[30] K. Nagaraj, F. Chen, T. Le, and T. R. Viswanathan, "Efficient 6-bit A/D converter using a 1-bit folding front end," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1056–1062, Aug. 1999.
[31] M.-J. Choe, B.-S. Song, and K. Bacrania, "A 13-b 40-MSaples/s CMOS pipelined folding ADC with background offset trimming," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1781–1790, Dec. 2000.
[32] T. Sigenobu, M. Ito, and T. Miki, "An 8-bit 30 MS/s 18 mW ADC with 1.8 V single power supply," in *Proc. VLSI Circuits Symp.*, 2001, pp. 209–210.
[33] P. Vorenkamp and R. Roovers, "A 12-b, 60-MSample/s cascaded folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1876–1886, Dec. 1997.
[34] M. P. Flynn and B. Sheahan, "A 400-Msample/s, 6-b CMOS folding and interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1932–1938, Dec. 1998.
[35] G. Hoogzaad and R. Roovers, "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm^2," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1796–1802, Dec. 1999.
[36] H. van der Ploeg and R. Remmers, "A 3.3-V, 10-b, 250 MSample/s two-step ADC in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1803–1811, Dec. 1999.
[37] K. Sushihara and A. Matsuzawa, "A 7 b 450 MSample/s 50 mW CMOS ADC in 0.3 mm^2," in *ISSCC Dig. Tech. Papers*, 2002, pp. 170–171.
[38] K. Kattmann and J. Barrow, "A technique for reducing differential non-linearity errors in flash A/D converters," in *ISSCC Dig. Tech. Papers*, 1991, pp. 170–171.
[39] K. Yoon, S. Park, and W. Kim, "A 6 b 500 MSample/s CMOS flash ADC with a background interpolated auto-zeroing technique," in *ISSCC Dig. Tech. Papers*, 1999, pp. 326–327.
[40] P. Scholtens and M. Vertregt, "A 6 b 1.6 GSample/s flash ADC in 0.18 μm CMOS using averaging termination," in *ISSCC Dig. Tech. Papers*, 2002, pp. 168–169.
[41] K. Bult and A. Buchwald, "An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1887–1895, Dec. 1997.
[42] H. Pan, M. Segami, M. Choi, J. Cao, and A. A. Abidi, "A 3.3-V 12-b 50-MS/s A/D converter in 0.6-μm CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1769–1780, Dec. 2000.
[43] M. Choi and A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1847–1858, Dec. 2001.

Jan Mulder received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1994 and 1998, respectively.

From 1998 to 2000, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom Netherlands, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He has published over 50 papers in technical journals and conference proceedings, and he holds 13 U.S. patents in circuit design. He is also the author of the book *Dynamic Translinear and Log-Domain Circuits* (Kluwer, 1999) and co-editor of the book *Research Perspectives on Dynamic Translinear and Log-Domain Circuits* (Kluwer, 2000).



Christopher M. Ward was born in Los Angeles, CA, in 1972. He received the B.S. degree from the California Institute of Technology, Pasadena, in 1994 and the M.S. degree from the University of California, Los Angeles, in 1996, both in electrical engineering.

He joined Broadcom Corporation, Irvine, CA, in 1996 and is currently a Senior Staff Design Engineer at Broadcom Netherlands, Bunnik, The Netherlands. His research interests are in analog and mixed-signal circuit design for communication and signal processing, as well as RF circuit design.

Chi-Hung Lin was born in Keelung, Taiwan, R.O.C., in 1967. He received the B.S. degree from National Taiwan University, Taipei, in 1989 and the M.S. and Ph.D. degrees from the University of California, Los Angeles, in 1994 and 1998, respectively, all in electrical engineering.

From 1989 to 1991, he served in the Chinese Army Missile Corps as a Maintenance Officer. From 1991 to 1994, he was involved in the study of CMOS device physics and reliability. In 1994, he joined Broadcom Corporation, Bunnik, The Netherlands, where he has been involved in the research and development of high-speed data converters.

Dr. Lin was the recipient of the Best Personnel Award in 1991 while serving in the Chinese Army.

David Kruse was born in Pasadena, CA, in 1966. He received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1989 and 1998, respectively.

In 1993, he joined Broadcom Corporation, Bunnik, The Netherlands, where he has been involved in analog and digital CMOS IC design for networking applications.

Jan R. Westra received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1993 and 1998, respectively.

From 1997 to 1999, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom Netherlands, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He is the author of the book *Oscillators and Oscillator Systems—Classification, Analysis and Synthesis* (Kluwer, 1999) and holds several U.S. patents in circuit design.

Marcel Lugthart received the M.S. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1993.

Afterwards, he joined Philips Research Laboratories, Eindhoven, The Netherlands, and worked on ICs for hard disk drives. In 1999, he joined Broadcom Netherlands, Bunnik, The Netherlands, and is currently involved in analog CMOS design.

Erol Arslan received the Ing./M.S. degree from the Katholieke Hogeschool Antwerpen (Karel De Grote Hogeschool), Antwerp, Belgium, in 1995.

He joined Alcatel Bell, Antwerp, in the same year, where he worked on integrated low-noise amplifiers for ADSL and integrated multiple access optical receivers. In 1998, he joined Xemics, Neuchatel, Switzerland, where he worked on low-power wireless transceivers. In 1999, he joined Sipex, Zaventem, Belgium, where he worked on optical receivers and laser drivers. Since 2002, he has been with Broadcom Corporation, Bunnik, The Netherlands, where he is involved in high-speed high-resolution ADC designs.

Rudy J. van de Plassche (M'83–SM'83–F'89) received the Ir. and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1964 and 1989, respectively.

In 1964 he joined Philips Research Laboratories, Eindhoven, The Netherlands, working in the field of instrumentation and control systems. Later on, the activity expanded into the area of electronic instrumentation and integrated circuits technology, in particular for data conversion with applications in measurement instruments, digital audio, and digital video systems. In 1983, he joined Philips Research Laboratories, Sunnyvale, CA, where he became a Group Manager for the Advanced Circuit Design Group. Returning to Eindhoven in 1986, he became involved in high-speed circuit design for optical communications using high-speed bipolar and GaAs technologies. In 1988, he became a member of the Radio and Data Transmission Group involved in the design of digital receiver architectures. He joined Eindhoven University of Technology, Eindhoven, as a part-time Professor in 1989, where he became a full-time Professor in 1998. In 1999, he joined Broadcom Corporation, Bunnik, The Netherlands, working on advanced circuits for data converters in CMOS technology. His research activities resulted in at least 50 publications and more than 65 issued U.S. patents.

Prof. van de Plassche was the recipient of the Solid-State Circuit Award and the "Veder" Award of the Dutch Stichting Wetenschappelijk Radiofonds Veder.

Klaas Bult (M'90) was born in Marienberg, The Netherlands. He received the M.Sc. and Ph.D. degrees from Twente University, Enschede, The Netherlands, in 1984 and 1988, respectively.

From 1988 to 1994, he worked as a Research Scientist at Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on analog CMOS building blocks, mainly for application in video and audio systems. From 1993 to 1994, he was also a part-time Professor at Twente University. From 1994 to 1996, he was an Associate Professor at the University of California, Los Angeles, where he worked on analog and RF circuits for mixed-signal applications. In the same period, he also was a consultant with Broadcom Corporation, Los Angeles, CA, and later in Irvine, CA. During this period, he started the Analog Design Group at Broadcom. In 1996, he joined Broadcom full-time as a Director, mainly focusing on analog amd RF circuits for embedded applications in broadband communication systems. In 1999, he became a Senior Director, heading Broadcom's Design Center in Bunnik, The Netherlands. He is a Broadcom Fellow and an author of many international publications and holds more than 25 patents.

Prof. Bult was the recipient of the Lewis Winner Award for Outstanding Conference Paper at ISSCC in 1990, 1992, and 1997.

Frank M. L. van der Goes was born in Delft, The Netherlands, in 1966. He received the Ph.D. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1996.

From 1996 to 1999, he worked on analog signal processing circuitry for digital TV/radio receivers at Philips Research Laboratories, Eindhoven, The Netherlands. He joined Broadcom Corporation, Bunnik, The Netherlands, as a Staff Scientist in the Analog and RF Microelectronics Department in 1999. He is currently an Engineering Manager and is involved in analog electronics for communication applications.