Analysis of Timing Jitter in CMOS Ring Oscillators

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Abstract

In this paper the effects of thermal noise in transistors on timing jitter in CMOS ring-oscillators composed of source-coupled differential resistively-loaded delay cells is investigated. The relationship between delay element design parameters and the inherent thermal noise-induced jitter of the generated waveform are analyzed. These results are compared with simulated results from a Monte-carlo analysis with good agreement. The analysis shows that timing jitter is inversely proportional to the square root of the total capacitance at the output of each inverter, and inversely proportional to the gate-source bias voltage above threshold of the source-coupled devices in the balanced state. Furthermore, these dependencies imply an inverse relationship between jitter and power consumption for an oscillator with fixed output period. Phase noise and timing jitter performance are predicted to improve at a rate of 10 dB per decade increase in power consumption.[1]

I. Introduction

Ring oscillators are widely used in phase-locked-loops (PLL) for clock and data recovery, frequency synthesis, clock synchronization in microprocessors, and many applications which require multi-phase sampling [1] [2]. In many such applications, clock signals are generated to drive mixers or sampling circuits in which the random variation of the sampling instant, or jitter, is a critical performance parameter. In some applications the frequency domain equivalent of jitter, called phase noise, is important. A block diagram of a typical PLL using a ring-oscillator for multi-phase clock generation is shown in figure 1. Jitter requirements in typical applications range from on the order of 100 picoseconds r.m.s. down to less than 5 picoseconds in very high-speed communications receivers, for example.

Jitter can arise from many sources, including inadvertent injection of signals from other parts of the circuit through the power supply. However, interfering sources like these can often be minimized by the use of circuit techniques such as differential implementations. In a fully optimized design the main source of timing jitter is the inherent thermal and/or shot noise of the active and passive devices that make up the inverter cell. 1/f noise is usually not of practical importance since it is rejected by the PLL loop filter, and does not effect the stage-to-stage delay in a DLL. Therefore minimizing the impacts of thermal and shot noise in the basic inverter cells becomes the key to attaining low timing jitter.

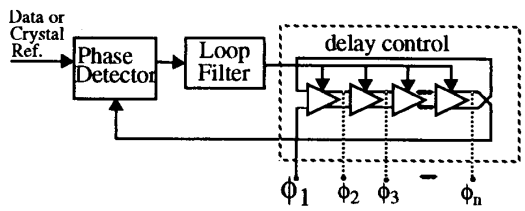

Figure 1. Ring-oscillator phase-locked-loop with multi-phase sampling

This paper attempts to determine analytically and through simulation the relationship between the design parameters of the inverter cell used in the ring-oscillator and the resulting noise-induced jitter. The class of circuits analyzed is source-coupled differential delay cells with resistive loads, implemented in CMOS technology, where the loads are realized by PMOS transistors in the triode region (figure 2). This particular implementation has proven useful in practical applications because of its high speed and rejection of supply noise [1]. In this paper we will first consider jitter for the individual delay stages in a ring-oscillator, and then look at the implications for design of the overall ring-oscillator phase-locked-loop.

II. First Order Timing Jitter Analysis

The period of a ring-oscillator is determined by the number of stages in the ring and the delay for each stage. Accompanying each cycle of oscillation is a random timing error due to noise. The goal of this section is to determine the contribution of thermal noise sources in an ECL type inverter circuit, like that shown in figure 2, to the timing jitter of the ring-oscillator.

In this analysis, each inverter stage in a ring-oscillator is assumed to contribute a nominal time delay, t_d, and a timing error, $\Delta\tau$, to each cycle of oscillation. The timing error has a mean of zero and a variance denoted by $\overline{\Delta\tau_1^2}$. To first order, the delay per stage is measured from the time when the outputs begin switching to the time when the differential output reaches zero, as illustrated in figure 3. With this assumption the nominal delay per stage is given by

$$t_d \cong V_{PP}\left(\frac{C_L}{I_{SS}}\right) \tag{1}$$

where I_{SS} / C_L is the output slew rate and V_{PP} is one half the full differential output swing. The load capacitance, C_L , is the total capacitance at the output of each inverter.

The random component of the timing delay is estimated using the first crossing approximation ([3]), illustrated in figure 4. Here, the simplifying assumption is made that the next stage begins switch-

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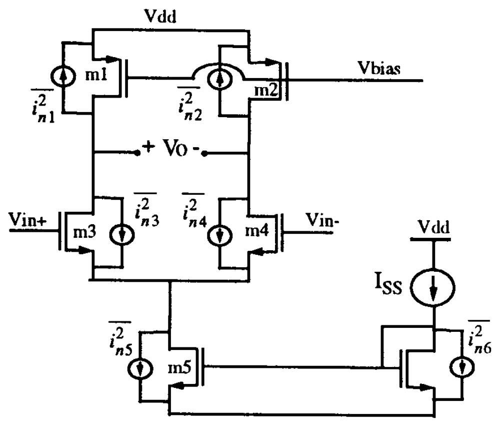


Figure 2. Differential delay cell with noise sources

ing when the differential output voltage crosses zero, and the error in the actual time of crossing is the timing error passed on to future stages in the delay chain. Figure 4 shows that an error voltage at the nominal time of crossing shifts the actual time by an amount proportional to the voltage error divided by the slew rate of the output. Using this approximation, the timing error variance is given by :

$$\overline{\Delta\tau_1^{\ 2}} \cong \overline{\Delta v_n^{\ 2}} \times \left(\frac{C_L}{I_{SS}}\right)^2 \qquad (2)$$

The voltage noise variance in equation (2) is the sum of contributions of each of the thermal noise sources in figure 2. The contribution of these noise sources to the differential output voltage is actually time varying in nature since they change as the circuit switches. In this section the simplifying assumption is made that the voltage noise variance will be the same as if the circuit where in equilibrium. In this case traditional noise analysis techniques [4] apply and the output referred voltage noise can be determined by integrating the noise spectral density over the bandwidth of the low-pass filter formed by the load resistor and the gate capacitance of the next stage. If this result is combined with (2) and (1), the r.m.s. timing jitter error for one stage normalized to the time delay per stage can be shown to be :

$$\frac{\Delta\tau_{1rms}}{t_d} \cong \frac{\Delta v_{rms}}{V_{PP}} = \sqrt{\frac{2kT}{C_L}} \bullet \left(\sqrt{1+\frac{2}{3}a_v}\right) \bullet \frac{1}{V_{PP}} \qquad (3)$$

Interestingly, the ratio of the timing error to the time delay per stage is just given by the ratio of the r.m.s. voltage noise to the voltage swing, V_{PP}. The voltage noise has the familiar *kT/C* dependence, and is proportional to another term called the noise contribution factor, ξ. In this case $\xi = \sqrt{1 + (2/3)\,a_v}$ where a_v is the small-signal gain of the inverter. The NMOS noise contribution is given by the second term in this expression and is proportional to the gain since, for a fixed output bandwidth, higher gain implies higher transconductance and hence a larger noise contribution. The PMOS contribution is the first term which in this case is just one.

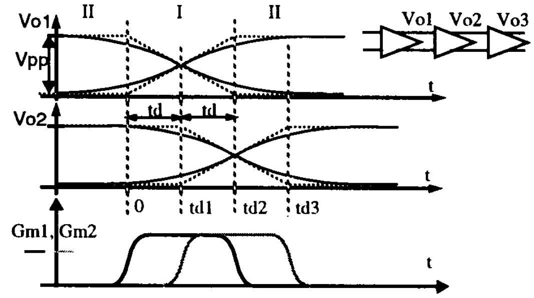
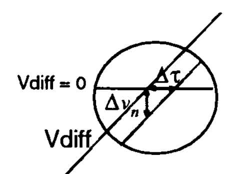


Figure 3. Output waveforms for CMOS inverter chain



$$\overline{\Delta\tau^2} = \frac{\overline{\Delta v_n^{\ 2}}}{(\text{Slew Rate})^2}$$

Figure 4. First crossing approximation for timing jitter

III . Second Order Analysis

The first order analysis neglects many important contributions to noise. A more thorough analysis must consider the time varying nature of the noise sources, the effects of the tail current noise sources, and interactions between stages.

Time varying noise sources

The assumption that the voltage noise variance is the same as its equilibrium value is not valid for the NMOS differential pair transistors since each side switches from fully on to fully off, during which the transconductance, and hence the noise contribution changes dramatically. Furthermore the tail current noise, although rejected by the circuit when balanced, contributes to the output voltage noise during other parts of the switching transient.

To simplify the analysis we break up the noise contributions into two piecewise constant regions of operation, as shown in figure 3. The tail current noise seen at the output is assumed zero while in balanced mode (I), and fully on during the unbalanced mode (II). The NMOS differential pair noise source contribution is approximately zero for the unbalanced mode[1], and is approximated as constant for the balanced region of operation. The contribution of the triode-region PMOS noise sources is nearly constant for both. To find the voltage noise at the output as a function the current noise sources, analysis is carried out in the time domain using autocorrelation functions and convolution. The result is a new noise contribution factor which captures the time dependence of the output voltage noise.

$$\xi = \sqrt{1+\frac{2}{3}a_v\left(1-e^{-t/\tau}\right)+\frac{2\sqrt{2}}{3}a_v e^{-t/\tau}} \qquad (4)$$

This equation shows that as the circuit begins switching (t=0), the diff. pair noise contribution (second term) rises exponentially from

1. In the unbalanced mode, one side of the differential pair is off, and the other side's contribution is reduced by emitter degeneration.

zero to its equilibrium value considered previously. The third component of the noise contribution factor is due to the tail current noise source and decays exponentially from its equilibrium value in the unbalanced mode (II) towards zero when switching begins. It can be shown that the time constant τ is approximately equal to the time delay of the stage, in which case the exponentials in this expression reduce to constants at the time of interest, t_d. This means that the noise contribution factor is relatively insensitive to most design parameters except gain.

Inter-stage Interaction

Figure 4 shows that for a typical CMOS inverter chain the switching times of adjacent stages overlap and there are times when more than one stage is in the active region of amplification. In this case it is not sufficient to consider the noise contribution of a single inverter alone since noise from one inverter may be amplified and filtered by the next stage, contributing to the jitter in the subsequent stages in that manner. A better model is to consider two successive stages, and determine the voltage noise at the output of the second stage directly from the thermal noise current sources in the first stage.

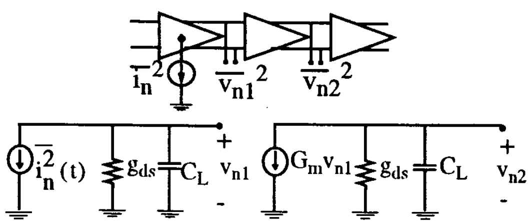


Figure 5. Extended circuit model for inter-stage interaction

Analysis for this case yields a slightly different noise contribution factor ξ than before, and an increase in the voltage noise variance by a factor of 1/2 $(a_v)^2$. With some re-arrangement, the new normalized timing jitter expression can be shown to be :

$$\frac{\Delta\tau_{1\ \mathrm{rms}}}{t_d} = \sqrt{\frac{kT}{C_L}} \bullet \frac{1}{(V_{GS} - V_T)} \bullet \xi \qquad (5)$$

This means the normalized r.m.s. timing jitter is actually given by the ratio of the *kT/C* noise level to the gate bias voltage above threshold for the balanced state, $(V_{GS} - V_T)$. If the second term is brought under the radical, then it is apparent that this fundamental timing error can also be expressed as the ratio of the thermal noise energy level to the electrical energy stored on the gate capacitance of the next stage.

IV. Simulations

A monte-carlo approach to transient noise analysis was taken to simulate the jitter performance of ring-oscillators in SPICE. This approach includes the effects of time-varying transconductances and inter-stage interaction. Figure 6 shows that, as expected, the normalized timing jitter improves with the square root of C_L. In the graph, C_L is scaled by changing the gate width. The gate width and current are scaled proportionally so as to keep $(V_{GS}\text{-}V_T)$ constant and fix the delay per stage. Since the static power consumption is proportional to I_{SS}, jitter improves with the square root of power consumption, as indicated by the top axes.

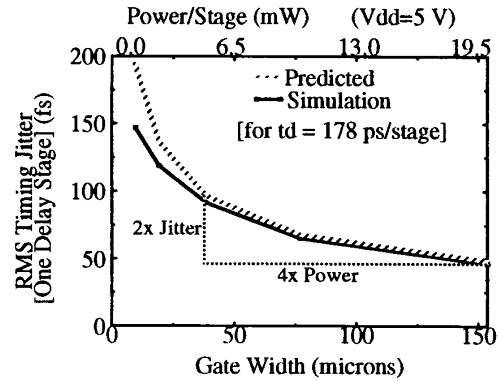


Figure 6. RMS timing jitter versus inverter size / power per stage

V. Design Implications

When designing a ring-oscillator, the parameter of interest is the jitter per cycle of oscillation. The analysis to this point has investigated the intrinsic jitter per delay stage, and we now extend these results to consider the jitter of the overall ring-oscillator. The jitter per cycle of oscillation can be used to determine the total PLL jitter for a ring-oscillator configured in a phase-locked-loop, and can also be used to predict the oscillator's phase noise spectrum.

Cycle-to-cycle jitter

Suppose the goal is to design a ring-oscillator with a fixed period, T_0, and minimal jitter. For an N-stage configuration the period of the oscillator is given by $2N \times t_d$, and the total jitter variance for once cycle of oscillation is given by $2N \times \Delta\tau_1^2$, provided noise sources in successive stages are independent. Using the results of the last section, the jitter per cycle of oscillation, or cycle-to-cycle jitter, can be shown to be

$$\overline{\Delta\tau_N^2} = \overline{\Delta\tau_1}^2 \times \frac{T_0}{t_d} = \frac{kT}{I_{SS}} \frac{a_v \xi^2}{(V_{GS} - V_T)} \times T_0 \qquad (6)$$

where the substitution $2N = T_0 / t_d$ is used so that the jitter can be expresses as function of T_0, rather than N.

To design for low jitter, $(V_{GS}\text{-}V_{TN})$ should chosen as large as possible. The inverter gain term, a_v, is the result of inter-stage amplification consideration. For designs where this is a factor (more true of CMOS than bipolar), this implies that a for a fixed delay and fixed current, the jitter improves with lower gain per stage. Inverter gain must be kept greater than one, however, for oscillation to occur. The noise contribution factor, ξ, is a weak function of most design parameters except gain. For many CMOS designs, a_v is kept in the range of 1.5-3, and ξ ranges from 1.3 to 1.9.

The main result of equation (7) is that with everything else fixed, the timing jitter variance improves linearly with an increase in supply current. Since power consumption depends on the quiescent current level, this implies, at least for the class of circuits considered here, a direct trade-off between power consumption and timing jitter.

Interestingly, the implications of equation (7) to *first order* do not change with changes in supply voltage, technology scaling, and configuration. If $(V_{GS}-V_{TN})$ is proportional to the supply voltage, then for a constant jitter, decreasing the supply voltage requires increasing the supply current by the same amount. This means that the power consumption stays the same. Scaling of the gate length gives access to higher speeds, but equation (7) shows that for a fixed T_0, the jitter is proportional to the current itself, and does not depend directly on the gate length. Velocity saturation effects have not been neglected, to first order, either, since no form for the current equation has been assumed. Another interesting result, is that the jitter variance does not depend on the exact configuration of the oscillator itself. Each of the configurations in figure 7, for instance, have the same period if inverters with the same $(V_{GS} - V_T)$ and I_{SS} are used; but by equation (7), they also have the same jitter variance. Power is minimized, in this case, by using the configuration with as few delay stages as necessary.

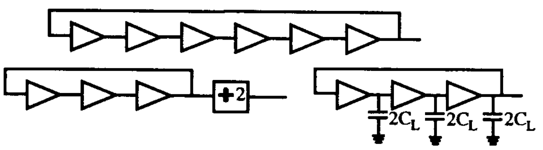


Figure 7. Multiple oscillator configurations with same period

Equation (7) shows that cycle-to-cycle jitter variance is proportional to the period, T_0, itself. A better figure of merit, however, is the jitter normalized to the period of oscillation. The r.m.s. jitter as a percentage of the output period $(\Delta\tau_{N_{rms}} / T_0)$ actually varies as $1 / \sqrt{T_0}$. This implies that higher frequency oscillators will have poorer jitter for the same power consumption.

Overall ring-oscillator PLL Jitter

In a ring-oscillator the variance of the timing error relative to a fixed reference transition, grows with each successive period of oscillation unless the oscillator is configured in a PLL. Analysis in [5] [6] shows that the total r.m.s. jitter when locked in a PLL will be α times the cycle-to-cycle jitter, where α is a multiplying factor which is inversely proportional to the bandwidth of the PLL. A wider bandwidth PLL corrects timing errors more quickly, resulting in a smaller overall jitter and an earlier roll-off point in figure 8. The minimum practical value of α is limited by clock feed-through, and other PLL design issues. α is typically in the range of 10-100. For a delay-locked-loop [4], jitter is not accumulated between periods, and α is effectively equal to one.

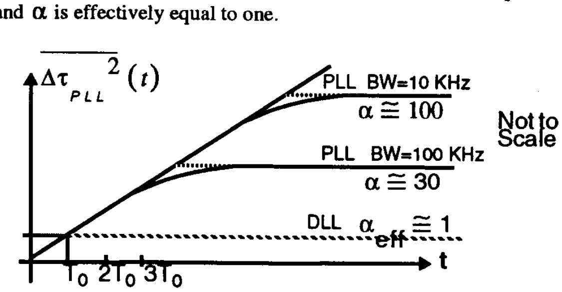


Figure 8. Jitter variance vs. time for reference transition at t=0

Ring-oscillator phase noise

Phase noise is an important figure of merit for oscillators used in RF applications. An ideal oscillator spectrum is an impulse in the frequency domain at the carrier frequency f_0. A real oscillator has its energy spread over a narrow bandwidth around f_0, and phase noise is a measure of the noise power in a 1-Hz bandwidth at a frequency f_m , offset from the carrier, relative to the total power of the oscillator. Phase noise can be determined from ring-oscillator timing jitter in a few ways. One way is to note that the accumulated phase error is a Wiener process, in which case its power spectrum can be shown to be a lorentzian. The other is to relate the spectral density of the normalized frequency fluctuations to the instantaneous error in the period of oscillation, $(\Delta\tau / T_0)$, and then use the relationships in [4] to arrive at the spectral density of phase fluctuations. With some re-arrangement of terms, the phase noise spectrum can be shown to have the following form :

$$S_{\Phi}(f_m) \cong \frac{f_0}{f_m^2}\left(\frac{\Delta\tau_{rms}}{T_0}\right)^2 = \left(\frac{f_0}{f_m}\right)^2 \bullet \frac{kTa_v\xi^2}{I_{SS}(V_{GS}-V_T)} \quad (7)$$

The phase noise is related to the ratio of the offset frequency to the oscillator frequency, and falls off at a rate of *20 dB / decade* for higher offsets. For a given frequency offset from carrier, the phase noise improves with higher inverter cell supply currents. Therefore phase noise is expected to improve with power consumption at a rate of 10 *dB* / decade.

VI . Conclusions

This paper has analyzed the relationship between design parameters of ECL type inverter cells and the resulting thermal-noise-induced jitter. The jitter per stage was shown to depend on the ratio of the *kT/C* noise level to the $(V_{GS}-V_T)$ bias point. The cycle-to-cycle jitter of a ring oscillator was shown to improve with larger bias currents and the normalized jitter was proportional to $1/\sqrt{T_0}$, indicating inherently higher jitter for higher speeds. Finally, the overall jitter in a PLL and the phase-noise of a ring oscillator were determined from the cycle to cycle jitter, and phase noise was predicted to improve at a rate of 10 dB / decade increase in power consumption.

VII . References

[1] B. Kim, D.N. Helman, P.R. Gray, "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2 mm CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 6, pp. 1385-1394, December 1990.

[2] M. Johnson, E.L. Hudson, "A Variable Delay Line PLL for CPU-coprocessor Synchronization," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1218-1223, October 1988.

[3] A. A. Abidi, R. G. Meyer, "Noise in Relaxation Oscillators," *IEEE Journal of Solid-State Circuits*, Vol. 18, No. 6, pp. 794-802, December 1983.

[4] P. R. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, NY, 1984

[5] B. Kim, T. C. Weigandt, P. R. Gray, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design," *ISCAS '94 Proceedings*, June 1994.

[6] J.A. McNeill, "A 200 mW, 155 MHz, Phase-Locked-Loop with Low Jitter VCO", *ISCAS '94 Proceedings*, June 1994.