Lec. 6

Analog to Digital Converters

Analog input is quantized. Output is a digital code.

Performance metrics are similar to Track-Hold and DACs.

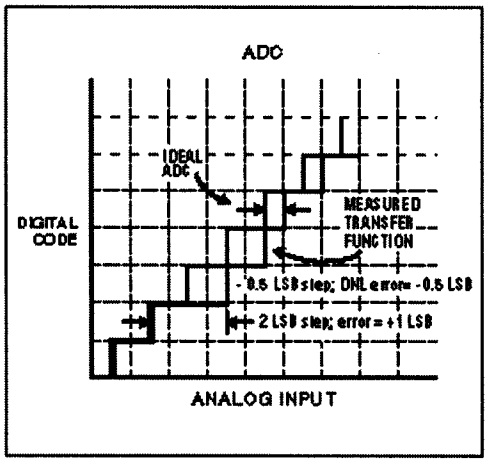
Static:

- DNL
- INL
- gain error
- offset error
- full-scale error

Dynamic:

- SNR
- SNDR
- SFDR
- aperture jitter
- settling time
- acquisition time

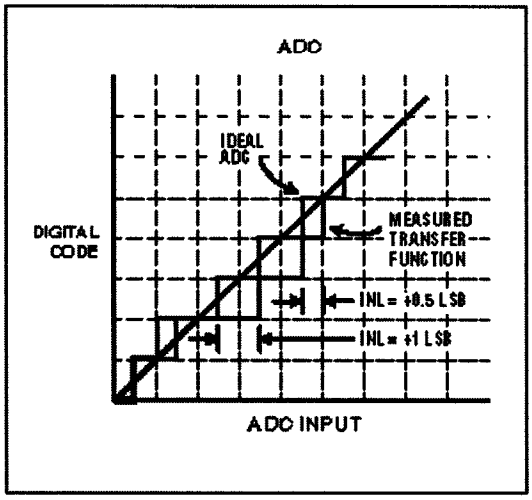
ADC DNL



Maxim AN-641

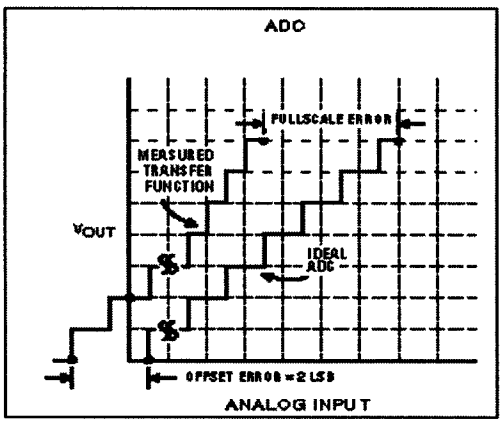
differential nonlinearity (DNL) error
For an ADC, DNL error is defined as the difference between the ideal and the measured code transitions for successive codes. An ideal ADC would have finite digital codes exactly 1LSB apart (DNL = 0). For a DAC, DNL error is the difference between the ideal and the measured output value between successive DAC codes. An ideal DAC would have analog output values exactly one code apart (DNL = 0). A DNL specification of greater than or equal to 1LSB guarantees monotonicity (see monotonic).

ADC INL



Maxim AN-641

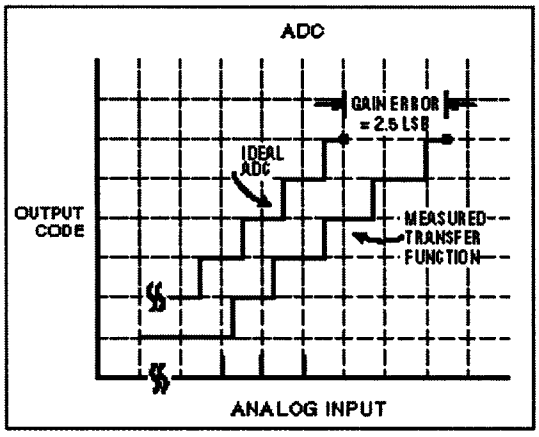
Full Scale Error



Maxim AN-641

full-scale (FS) error
For an ideal ADC, the code edge triggers the transition to full-scale at 1.5LSB below the full-scale analog voltage. The full-scale error is the difference between this ideal code transition and the actual measured code transition. Full-scale error = offset error + gain error. See Figure 4.

Gain Error



Maxim AN-641

Gain error is a figure of merit that indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or a percent of full-scale range (%FSR). It can be calibrated out with hardware or in software.

For frequency domain applications, the accuracy of the ADC is limited by SFDR, just as was true for the DAC.

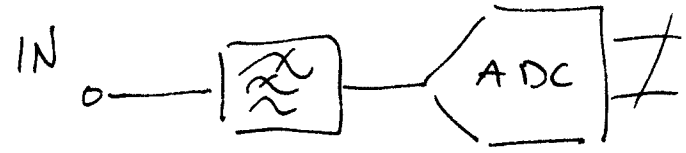
Define an effective # of bits (ENOB)

$$ENOB = \frac{SNDR(or\,SFDR) - 1.76}{6.02}$$

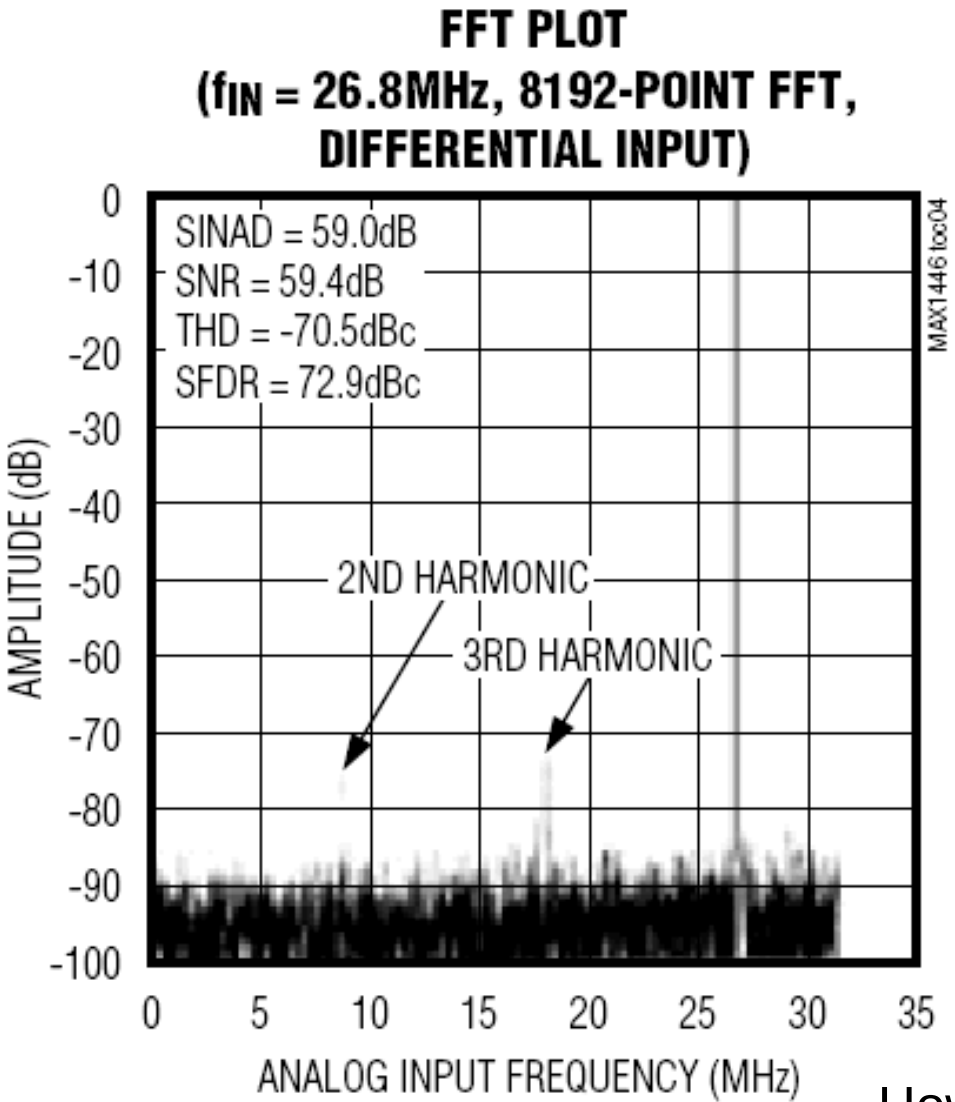
So, taking the dynamic range that is given by harmonics, aliases, intermods and using that to judge the converter.

External noise.

Input wideband noise will be aliased into the Nyquist band. So, a low-pass filter must be used to attenuate external noise. Otherwise, SNR or SFDR will be compromised.



SNR = 6 x 10bits + 1.76 = 62 dB = *total* noise power over Nyquist BW



Maxim AD1446 data sheet

$$ENOB = \frac{SINAD - 1.76}{6.02} = 9.5 bits$$

Fsample = 62.35 MHz

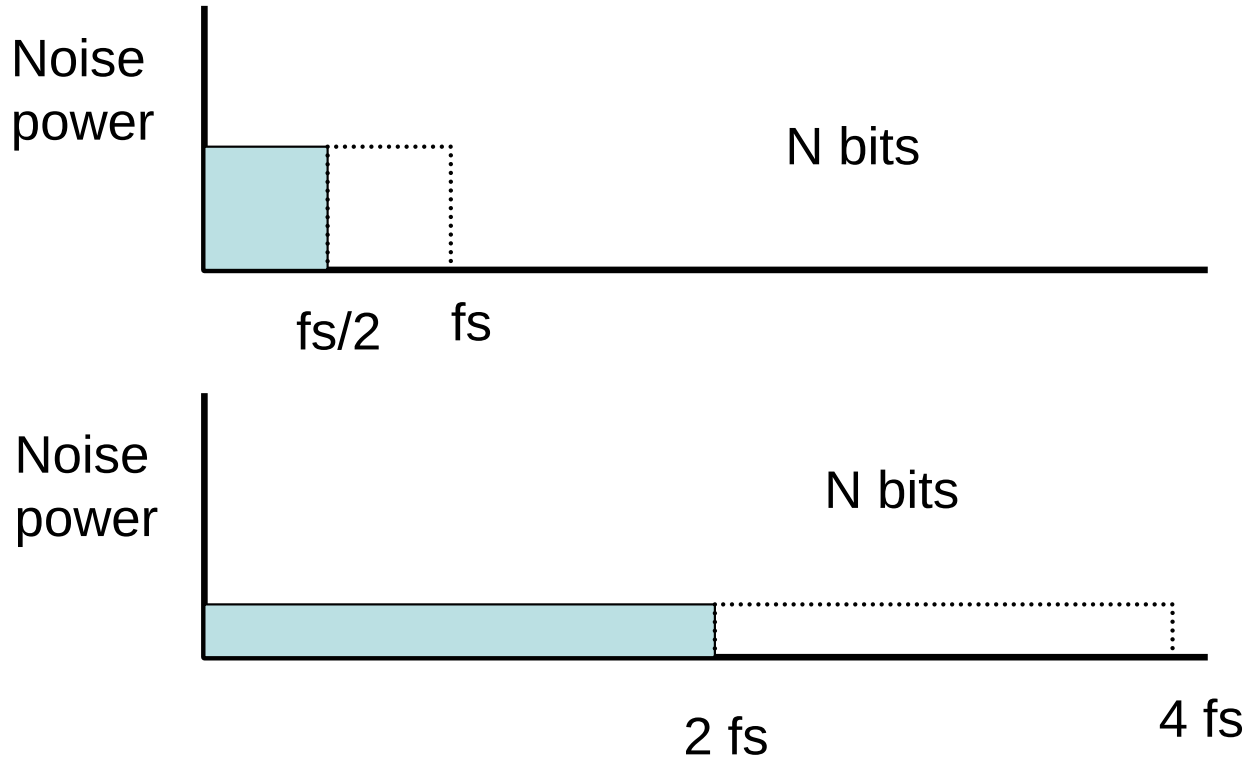
How can noise floor be – 95 dBc?

RBW = Fsample/2/8192

Noise floor reduced by 10 log 8192 = 39 dB

Oversampling

- Sampling frequency can be increased to spread quantization noise over wider Nyquist bandwidth.
- Then, noise power in a given signal bandwidth will be reduced.



Effective Resolution Bandwidth

- Increase input frequency at fixed fs
- ERBW = The frequency at which the SNR drops by 3 dB (1/2 LSB) compared with SNR at low input frequency.

Noise Figure

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} \qquad NF = 10 \log F$$

Nyquist ADCs are used in receivers, generally at IF, although for lower RF frequencies and lower SDFR, in front ends. NF needed for system analysis.

We can calculate an effective noise figure for an ADC:

1. assume white noise across Nyquist band. $f_s/2$
2. SNR is determined for continuous sinusoidal input signal 0.5 to 1 dB below full scale level.

   ideally $SNR = 6.02N + 1.76$ dB

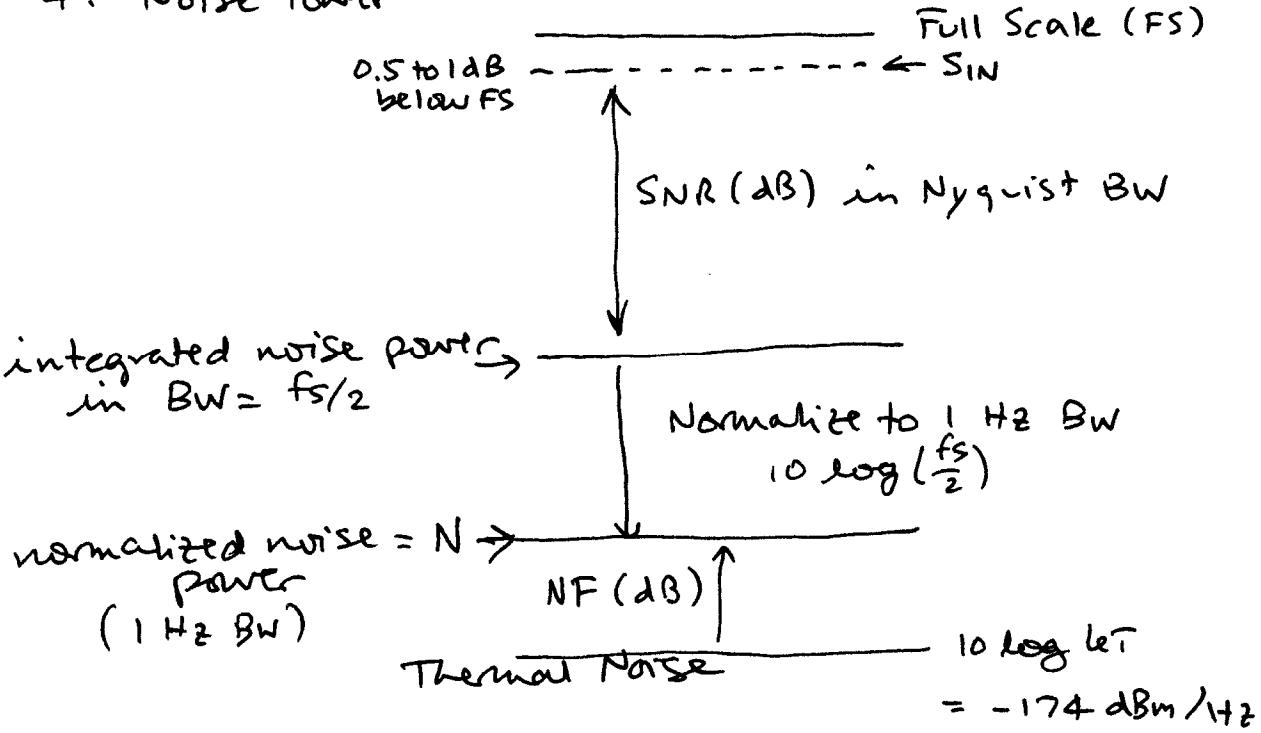
   but there are many factors that can degrade this —
3. Full Scale Power

   Peak voltage V_p

   $$\text{Signal Power} = S_{in} = \frac{V_p^2}{2R_{IN}} \quad \text{(Watts)}$$

   $$dBm = 10 \log(S_{in}) + 30\,dB$$

4. Noise Power



$$S_{in}(dBm) - SNR - 10\log\left(\frac{fs}{2}\right) = \text{effective noise power normalized to 1 Hz BW.} = N$$

So $NF = N - (-174)$ dB

example.

1. Suppose FS = 2V. $R_{IN} = 50\Omega$

$V_p = 1V$ $\quad S_{in} = \frac{1}{100} = .01\,W = 10\,mW$

$= 10\,dBm$

Drop back 1dB → 9dBm

2. Suppose measured SNR for 12bit converter at 100Ms/s = 65dB

(spurs are not included in NF calculation)

Nyquist BW noise power = $9 - 65 = -56\,dBm$

$10\log\left(\frac{fs}{2}\right) = 10\log(5\times10^7) = 77\,dB$

3. Normalized Noise Power = $-56dBm - 77dB$

$= -133\,dBm$

4. $NF = -133 + 174 = 41\,dB$

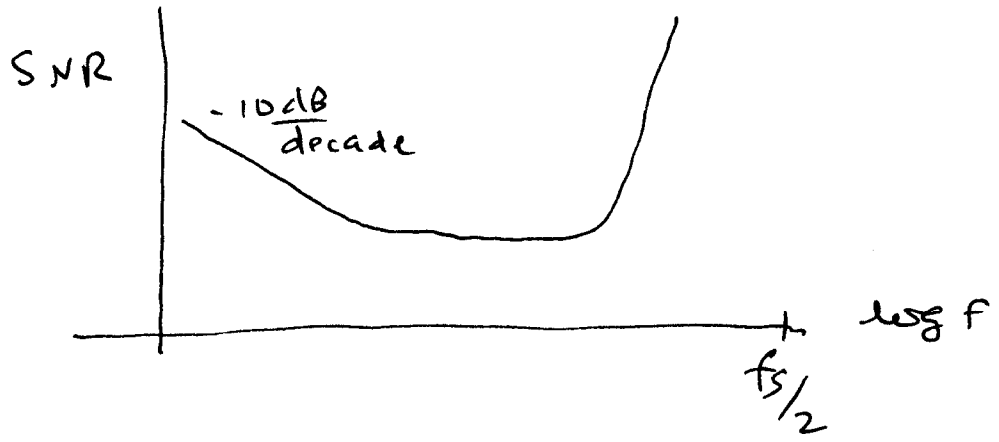
(better not put this one at the front end!)

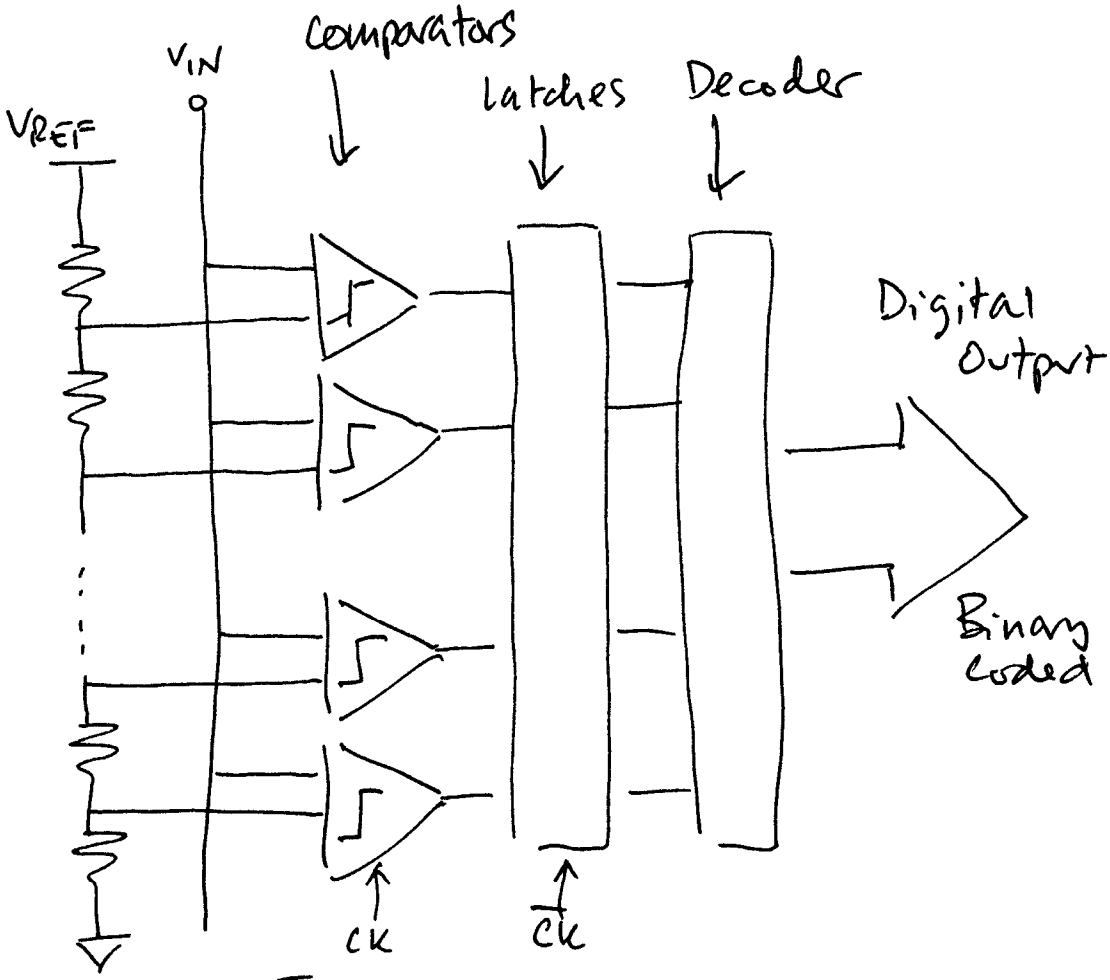
What happens if you reduce the sampling frequency?

Same noise is spread over a narrower bandwidth.

10 dB/decade increase in NF.

So you would expect to see SNR improve with fs up to the point where jitter or TH glitches start to dominate





Flash ADC. m-bits

Full parallel architecture for speed.

2^m comparators + latches

2^m resistors

comparator outputs are thermometer coded.

act as parallel sample-hold

output = 1 if $V_{in} > V_{REF}$

= 0 $V_{in} < V_{REF}$

metastable if $V_{in} \approx V_{REF}$

may not require THA at front end.

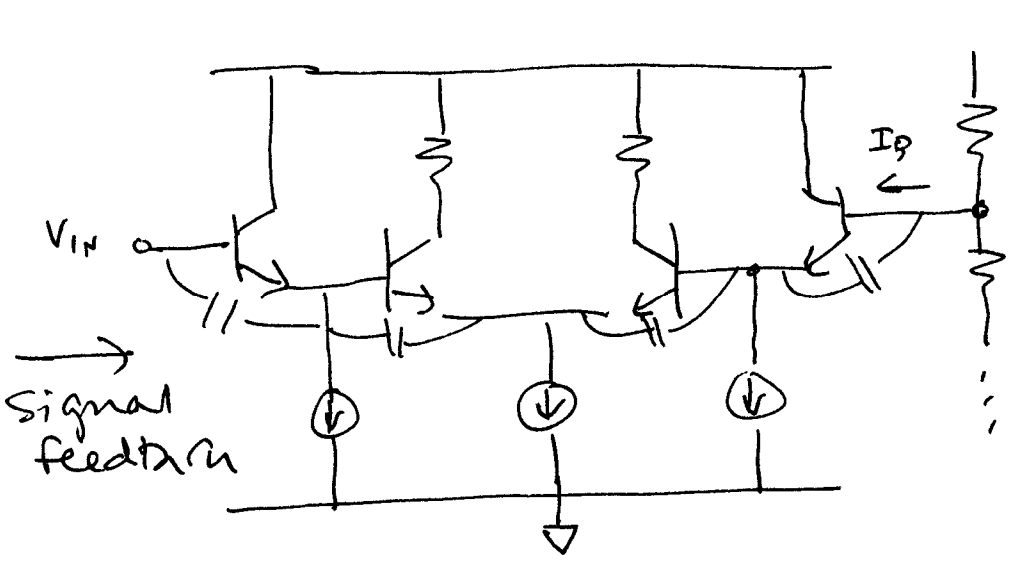
large number of components generally limits flash converters to 8 bits or less.

Errors:

1. Reference static and dynamic errors.

   A. resistor mismatch.
      same considerations as in resistor chain DAC.

   B. bias currents.
      bipolar comparator



base currents create INL - bowing
each tap voltage is decreased.

C. signal feedthru is worse at higher freq.
disturbs reference voltages dynamically.

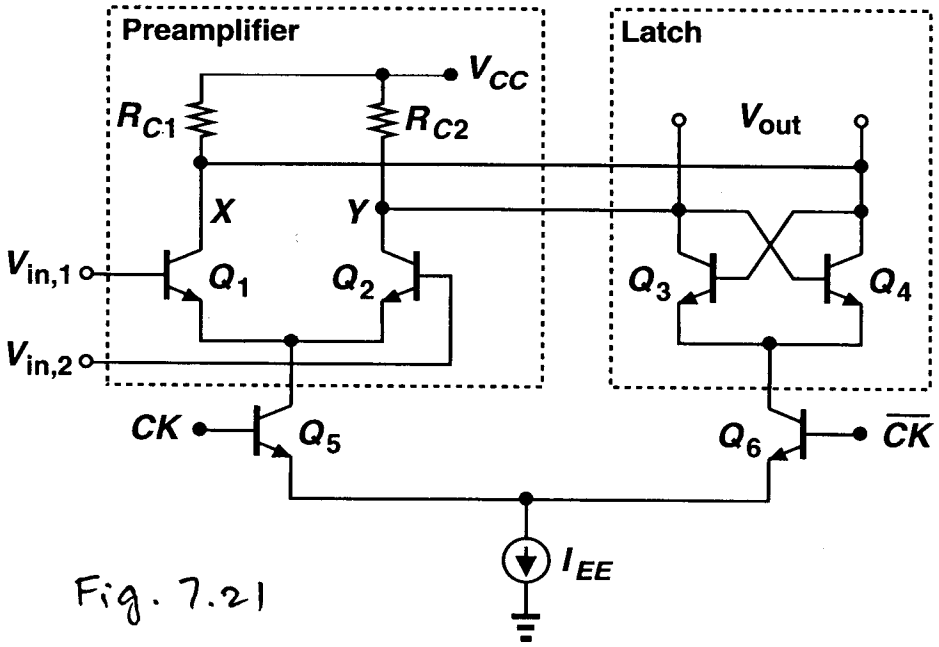
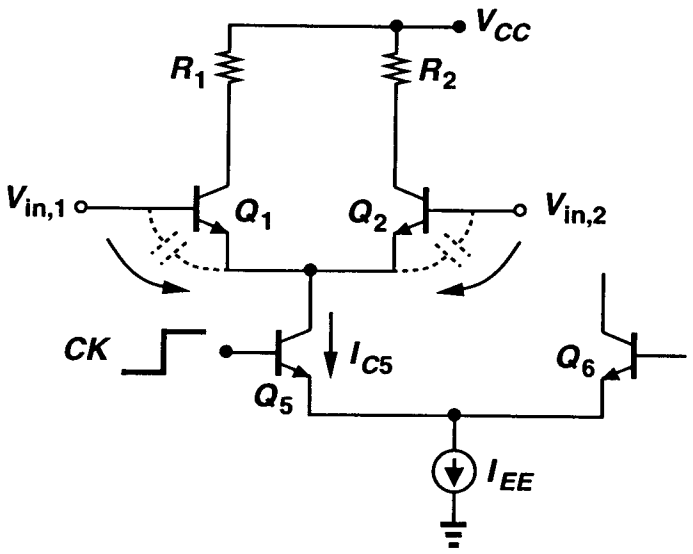
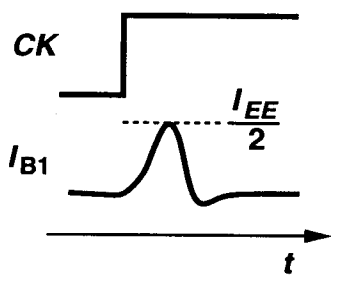


Fig. 7.21



(a)



(b)

Fig. 7.23 Generation of kickback noise in a bipolar comparator.

B. Razavi, Data Conversion System Design, IEEE Press, 1995.

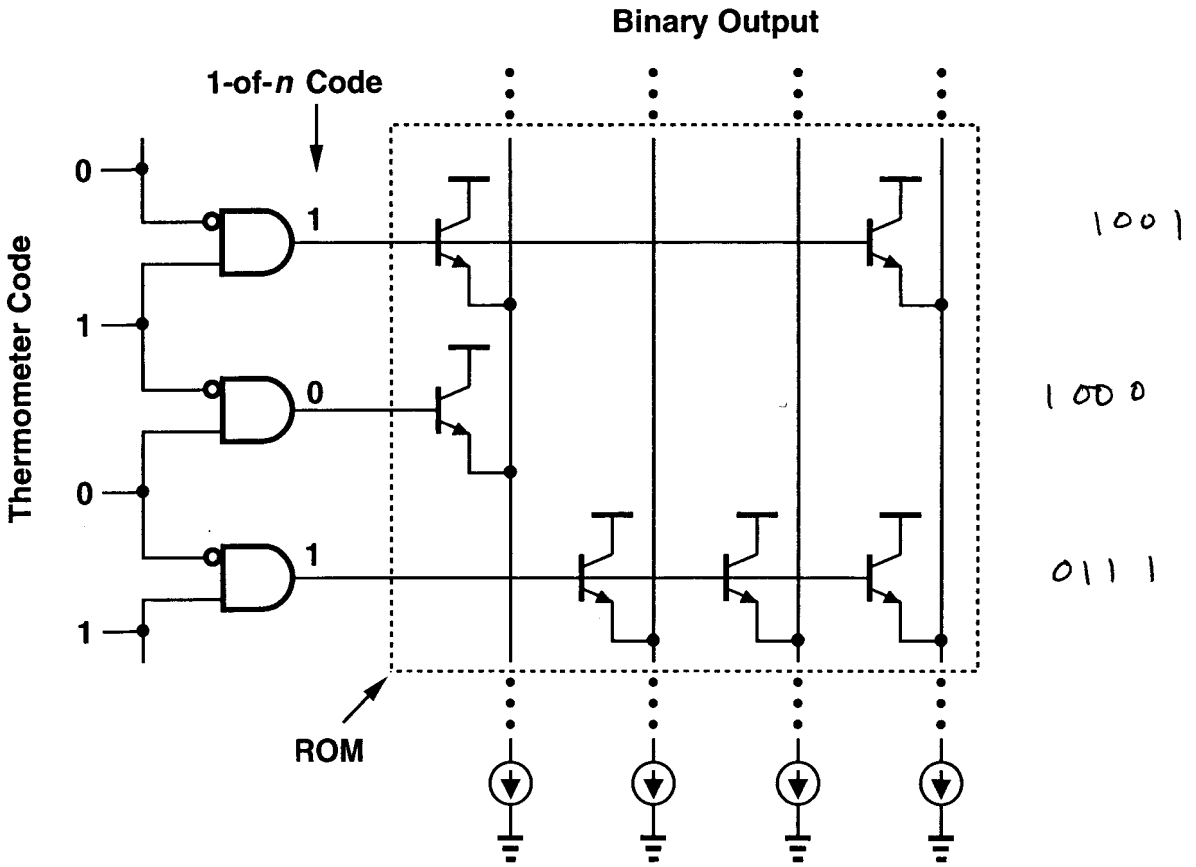


Fig. 6.13 Thermometer-binary decoder with a sparkle error.

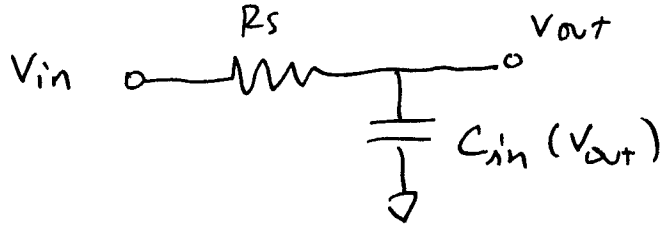
should be 1000 → instead we get 1111
half of full scale error

D. Nonlinear input capacitance.

Lots of comparators; input capacitance can be large and nonlinear.

voltage dependent phase shift.

causes harmonic distortion.

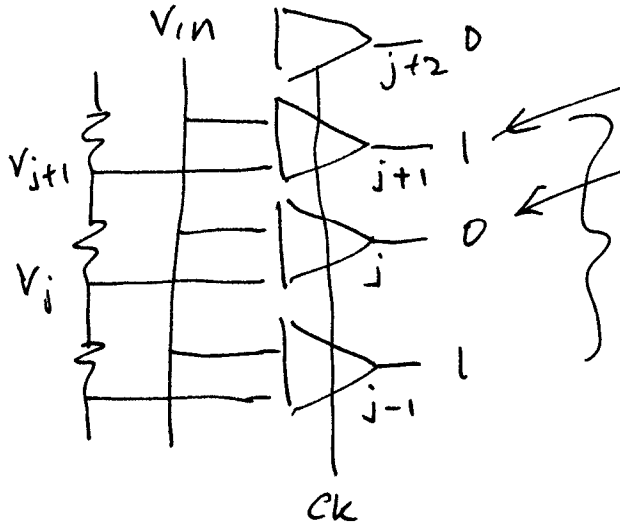


E. Kickback. When comparators are strobed, noise is generated at their inputs.

(Fig. 7.21, 7.23)

F. Comparator aperture uncertainty.

- comparators may not be identical or
- clock delay causes a lower comparator to latch earlier than the one above.



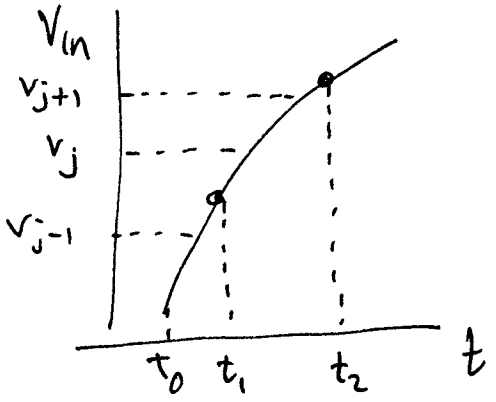
too late

too early

Should be thermometer code, but error due to mis-sampling

"sparkle"

when V_{in} has high slew rate,



can also be caused by DC offset in comparator.

Figs. 6.12, 6.13 Razavi.

can cause huge errors in therm. → binary conversion. Degrades SNR, creates distortion

Lec. 7

Last time:

ADC static performance

dynamic performance

$$ENOB = \frac{SFDR - 1.76}{6.02}$$

Noise figure

Flash ADC architecture

errors:

mismatch

loading

delay on RC input network

bubbles or sparkles in therm. code

Today:

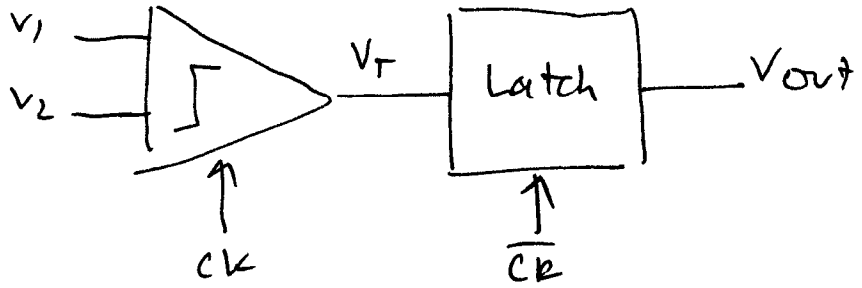
Comparator metastability

2-step converters

interpolation

Since linearity isn't needed, use positive feedback in the latch to effectively increase the gain.

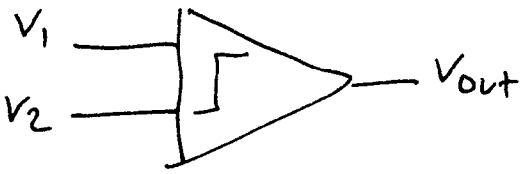
This also is used to define the sampling instant (like the track-hold)



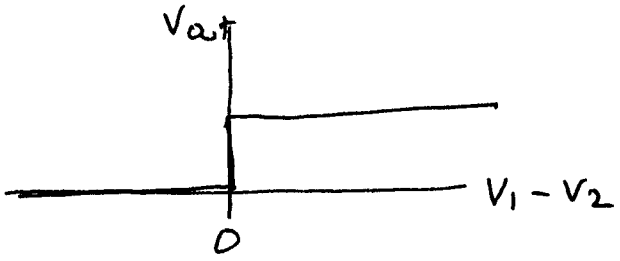
Track: $Ck = 1$ — V_T tracks input; latch is disabled

Latch: $CK = 0$ — amp. is disabled; latch holds present valve of V_T. senses polarity.

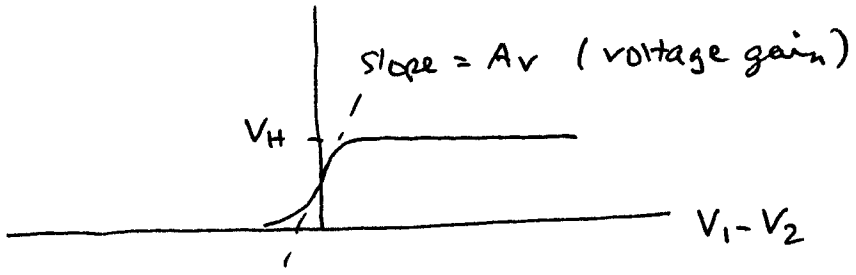
This works well when $V_1 - V_2$ is not small. When small we can have metastable case where latch can take a long time (or never) to respond. dynamic error.



ideal comparator:



can be approximated by a high gain amplifier.



output is valid when $|V_1 - V_2| > \frac{V_H}{A_V}$

so, resolution depends on gain.

Likewise,

$$N_x + T_0 \frac{dN_x}{dt} = -A_0 N_y$$

subtract

$$T_0 \frac{d(N_x - N_y)}{dt} = -(1 - A_0)(N_x - N_y)$$

initial condition $V_{xy0} = (N_x - N_y)\big|_{t=0}$

$$N_x - N_y = V_{xy0} \exp\left[(A_0 - 1)\frac{t}{T_0}\right]$$

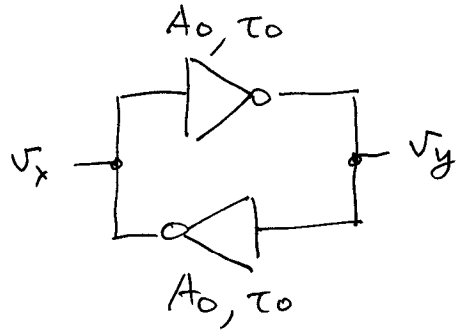
growing with time since $A_0 >> 1$

BUT!

with time constant $T_0/(A_0 - 1)$

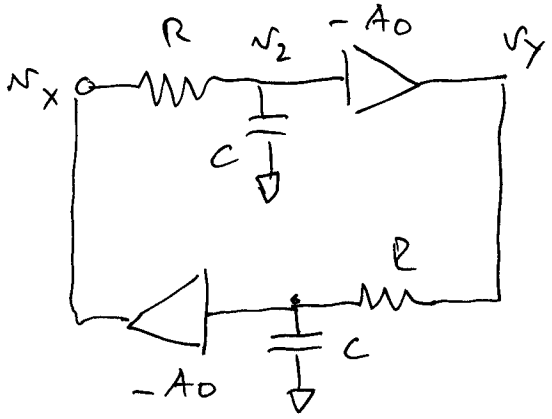
and if V_{xy0} is very small, it could take a long time to reach valid logic levels.

Simple latch model.



$\tau_0 = RC$

represent as single dominant pole for determining transient response.



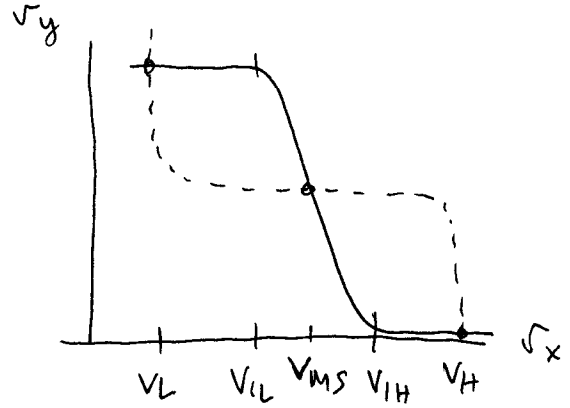
$$\frac{V_x - V_2}{R} - C\frac{dV_2}{dt} = 0$$

$$-V_2 - \tau_0 \frac{dV_2}{dt} = -V_x$$

$$V_2 = \frac{-V_y}{A_0}$$

$$\frac{V_y}{A_0} + \frac{\tau_0}{A_0}\frac{dV_y}{dt} = -V_x$$

$$V_y + \tau_0 \frac{dV_y}{dt} = -A_0 V_x$$



starting at metastable point V_{MS}, we must reach V_{IH} or V_{IL} before logic is fully stable.

How long will this take?

$$T_1 = \frac{T_0}{A_0 - 1} \ln\left(\frac{V_{IH}}{V_{xyo}}\right)$$

if V_{xyo} is very small, this can take a long time. Then, a sparkle can be produced because a valid logic state has not been obtained yet.

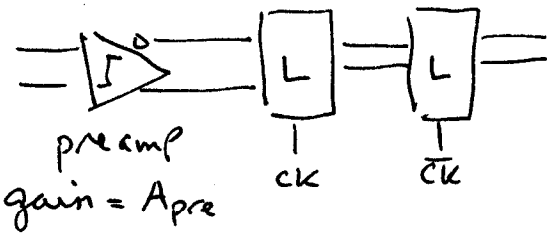
What is the probability?

$$\text{if } T_c = \text{regeneration time} = \frac{1}{2}T$$

$$P(T_1 > T_c) = \exp \frac{-(A_0 - 1)T_c}{T_0}$$

increase A_0. decrease T_0.

The effective gain in the latch stage can be increased by cascading.



For single latch stage,

$$V_o \cong A_{pre} V_{in} \exp\left(\frac{t}{\tau}\right)$$

where V_o, V_{in} are usually differential

and $\tau = \tau_0/(A_0 - 1)$

$t \cong \frac{T}{2}$ ($\frac{1}{2}$ period of clock)

By adding a second latch in cascade, we increase the regeneration time by another half clock cycle.

now,

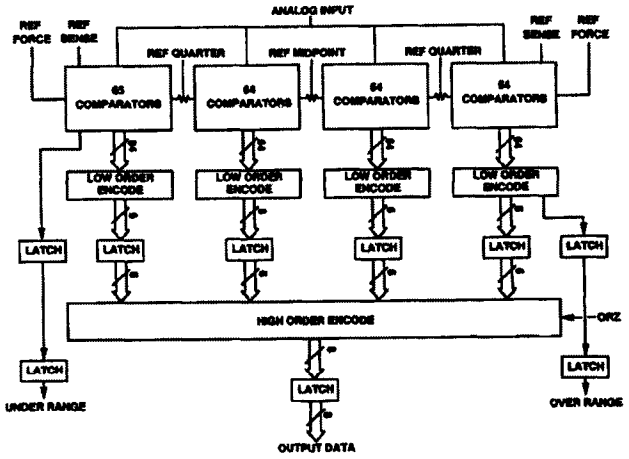
$$V_o \cong A_{pre} V_{in} \exp\left(\frac{t_1}{\tau}\right) \exp\left(\frac{t_2}{\tau}\right)$$

$$= A_{pre} V_{in} \exp\left(\frac{t_1 + t_2}{\tau}\right)$$

a third latch stage can also be used to further increase gain at the cost of latency.

Ref: C. Mangelsdorf, JSSC, Vol 25, #1, pp. 184-191, Feb. 1990.

8-bit Flash ADC



C. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

Pipeline detail

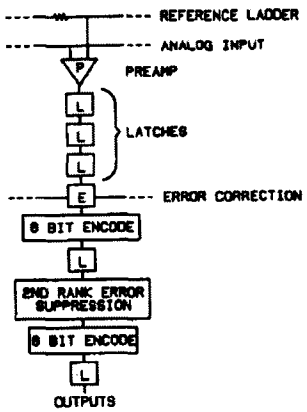
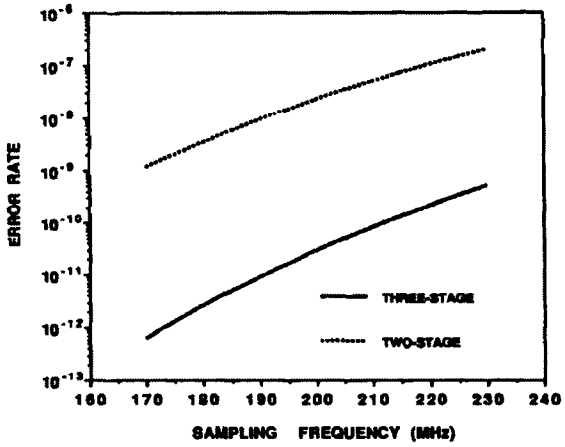


Fig. 2. Pipeline detail.

C. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

Reduced error rate due to cascaded latches



C. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

ENOB vs. input amplitude

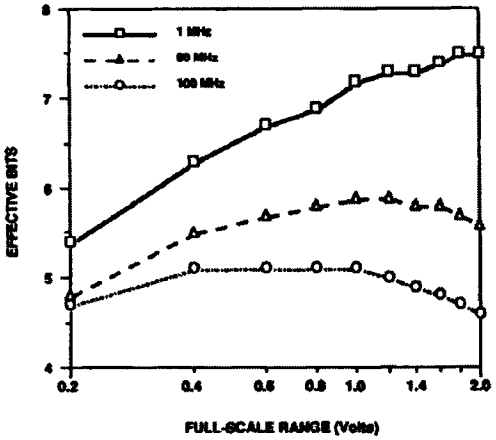


Fig. 10. Effective number of bits versus full-scale range for 1-, 50-, and 100-MHz analog input frequencies, all at 200 Ms/s. Input amplitude was adjusted for each range.

C. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," IEEE JSSC Vol.25,#1, pp184-191, Feb 1990.

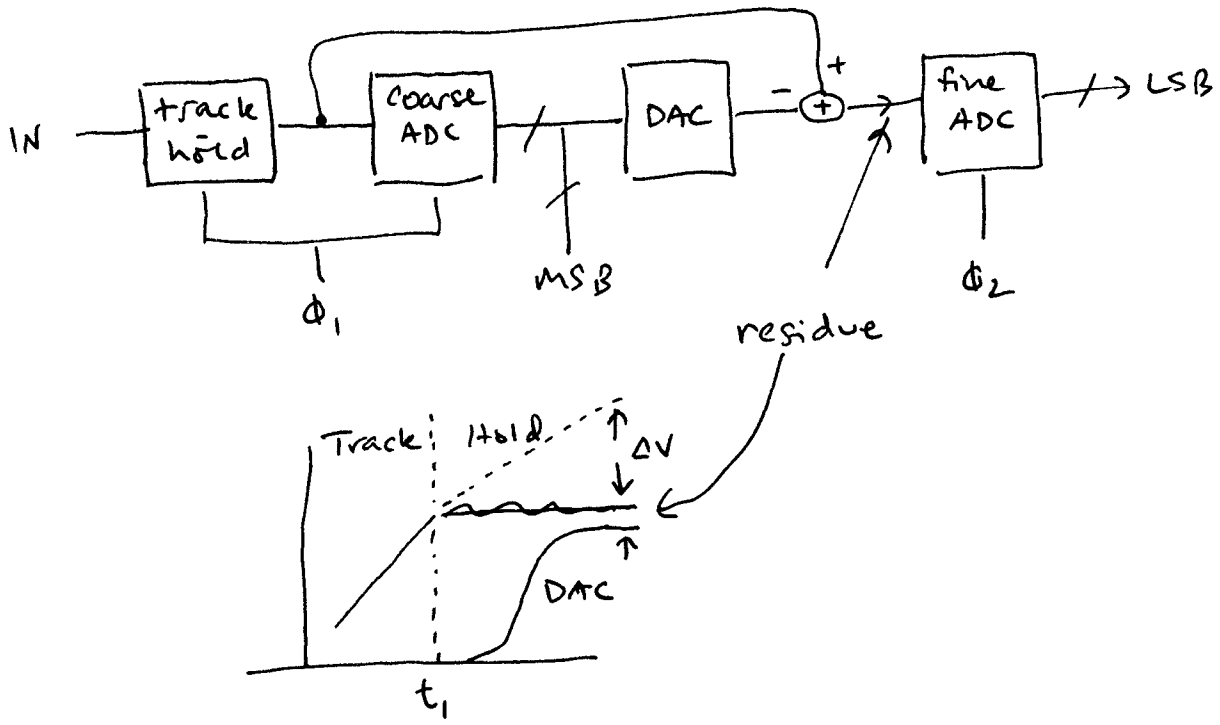
Flash ADCs have a practical limit of 8 bits or so. How can we get higher resolution?

Tradeoff speed or latency for complexity reduction and accuracy.

Two-step ADCs

t_1: coarse analog estimate + MSB quantization
take ↓ difference

t_2: fine LSB A/D using flash



TH is needed because of time delay between t_1 and DAC settling. Otherwise we have an error ΔV. This would greatly limit maximum input frequency to well below Nyquist.

Requirements.

1. Coarse DAC must have high precision
   $\pm \frac{1}{2}$ LSB

   otherwise fine ADC receives incorrect residue.

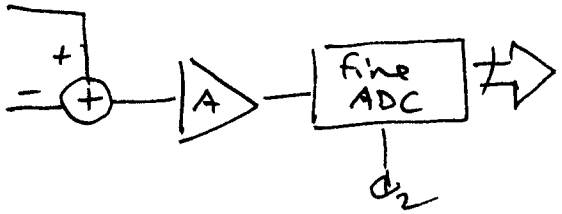
2. Much slower than flash ADC

   SH / TH stage much slower than comparator.
   comparator just requires 0 or 1 output whereas the TH must be precise and fully settled.

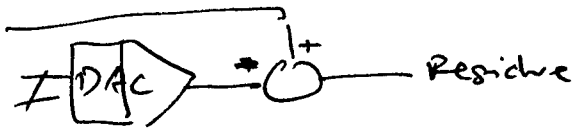
   Must wait also for DAC, subtractor, and fine AD to completely settle.

3. fine ADC has small full scale value.

   less dynamic range
   you can amplify output of subtractor, but that adds more requirements for accuracy and distortion of the amplifier.



Nonidealities.

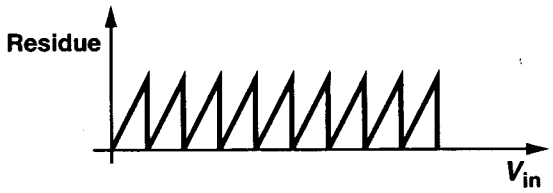


Coarse stage static error carries through since the coarse estimate and the signal are subtracted (analog). So, DNL, INL, offset and gain errors are all deadly.

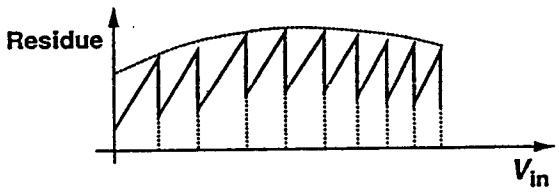
This difference is called a residue. a plot of this residue over a swept input can reveal the error type:

(Razavi)

In order to obtain a better view of these effects, the concept of the quantization error plot (Section 6.1) can be generalized to a residue plot wherein the difference between the actual and ideal characteristics is depicted as a function of the input (Figure 6.27). In a residue plot, gain error appears as peaks that follow a nonhorizontal straight line, DNL as shifted transition points, INL as peaks that do not follow a straight line, and offset as a vertical shift [Figure 6.27(b)].



(a)

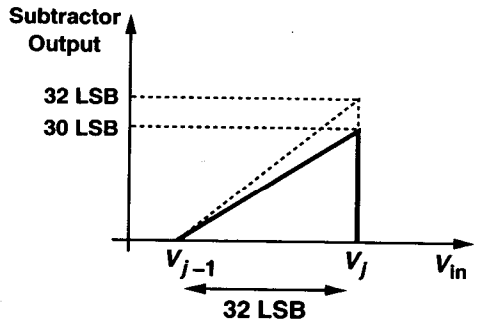


(b)

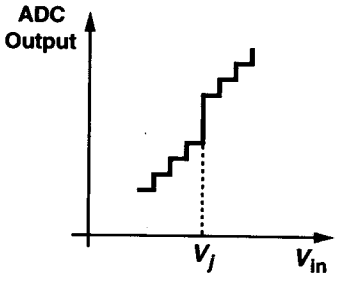
Fig. 6.27 Residue plot derived from characteristic of Figure 6.26. (a) Ideal; (b) including errors.

If these errors exceed 1 LSB, you can actually have missing codes because the subtractor output might not reach the full m-bits of the course ADC before it switches to the next course code.

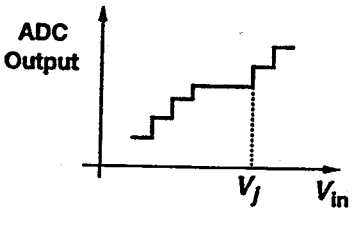
See book for example (p 123)



(a)



(b)



(c)

Fig. 6.28 (a) Subtractor output in a two-step ADC; (b) missing code; (c) ~~nonmonotonicity.~~

2 stage 10 bit ADC

94 comparators instead of 1024

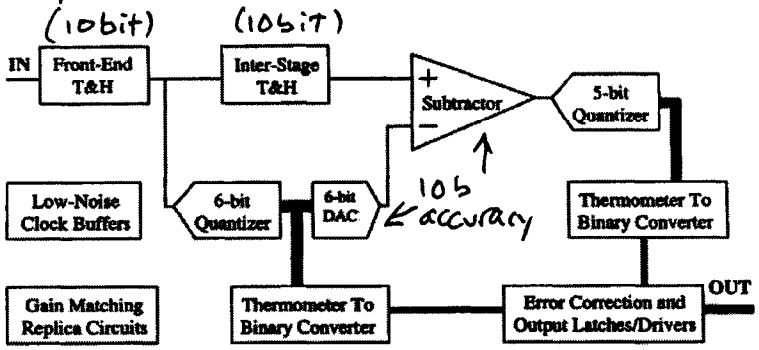


Figure 1: Block diagram of a 10-b, 1GS/s ADC.

N. Sheng, et al,"A 10-bit, 500 MS/s ADC," IEEE IMS, pp. 197-200, 1999.

2 stage ADC dynamic performance

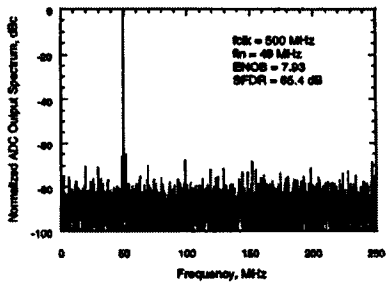


Figure 5: Measured ADC performance at 500 MS/s with 49 MHz input.

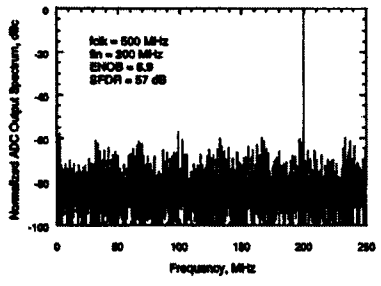


Figure 6: Measured ADC performance at 500 MS/s with 200 MHz input.

N. Sheng, et al,"A 10-bit, 500 MS/s ADC," IEEE IMS, pp. 197-200, 1999.

Subranging ADCs.

+ No subtractor.

Coarse stage subdivides reference

Fine stage compares against subdivided reference.

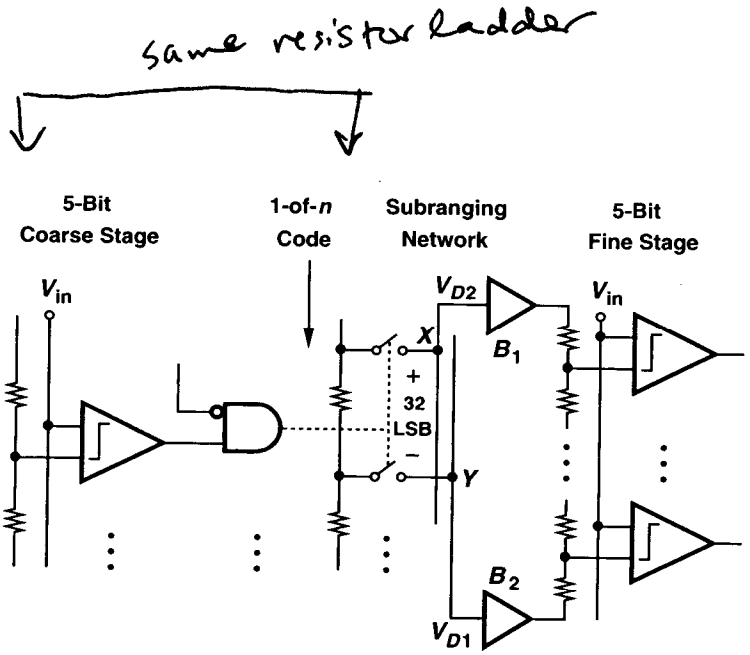


Fig. 6.31 Section of a 10-bit subranging ADC architecture.

Problems:

1. R ladders are slow to settle
2. comparators must operate over the full input common mode range.

Interpolation.

Make use of linearity of comparator preamp to obtain extra resolution while retaining one-stage ADC ~~topology~~. topology.

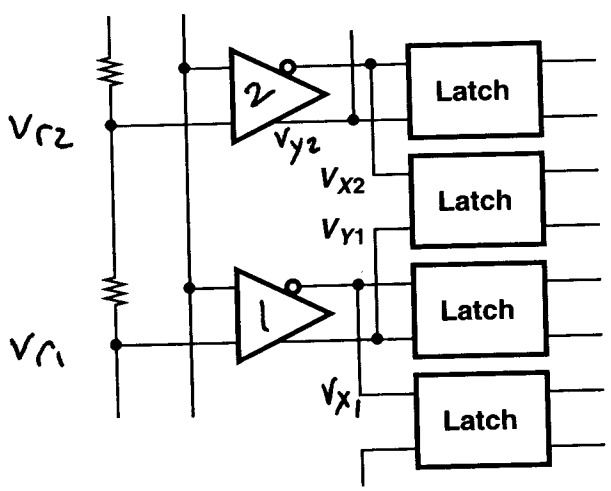
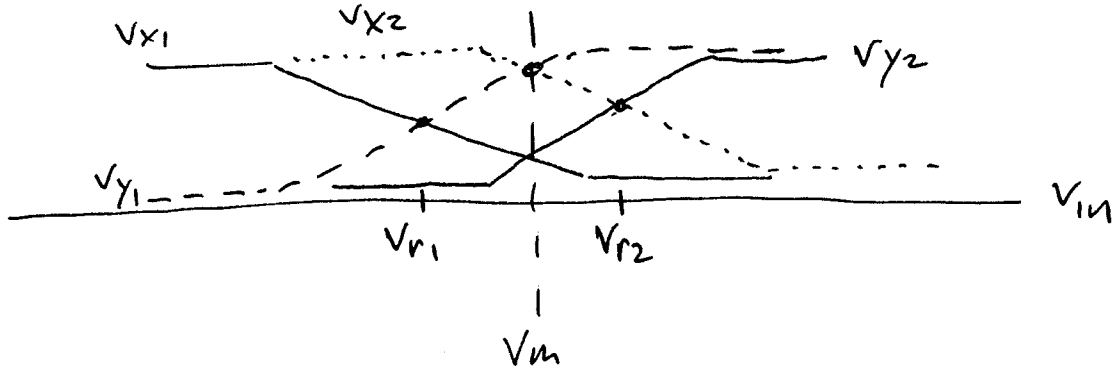


Fig. 6.33 Interpolation in a flash ADC.

How it works: plot amplifier outputs



Note that the relative values of V_{x2} and V_{y1} exactly represent the difference between V_{in} and $V_m = \frac{V_{r1} + V_{r2}}{2}$. So, we interpolate between two ref. levels. Latch senses polarity and gives extra bit

You can increase the degree of interpolation by using a resistor chain to further increase # of bits between two taps of a flash converter.

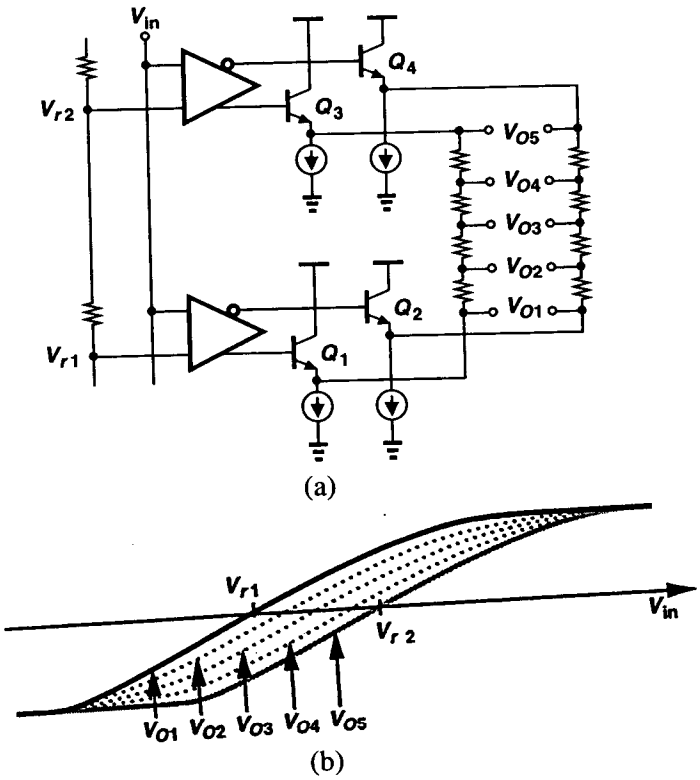
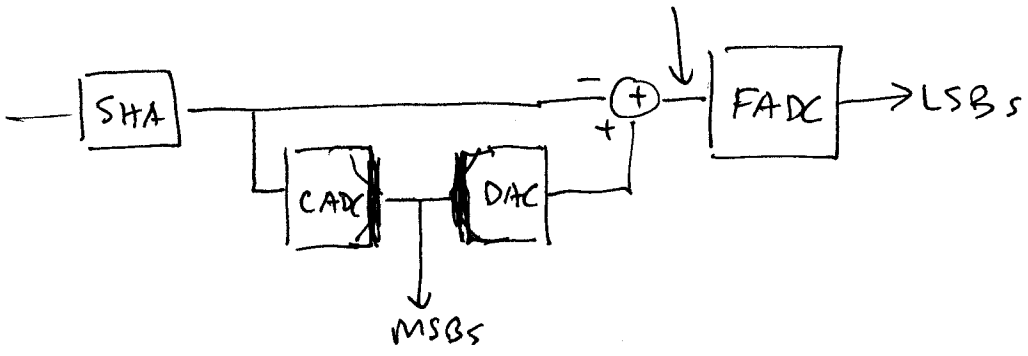


Fig. 6.36 Higher order interpolation. (a) Implementation; (b) input/output characteristics.

Folding ADC Architecture

2 step ADCs split the data conversion into two or more time phases.

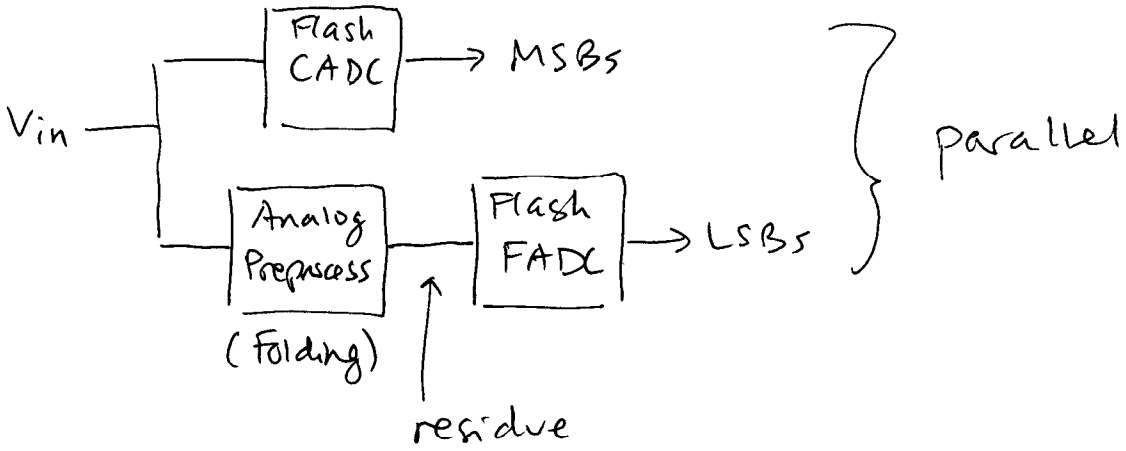
Delays of S/H A, coarse ADC, DAC and subtractor must all settle before residue is valid.



Subranging eliminates the DAC and subtractor but still is a two-step process.

CADC activates switches to select subrange for FADC.

Folding is an approach which generates the residue in a one step process.



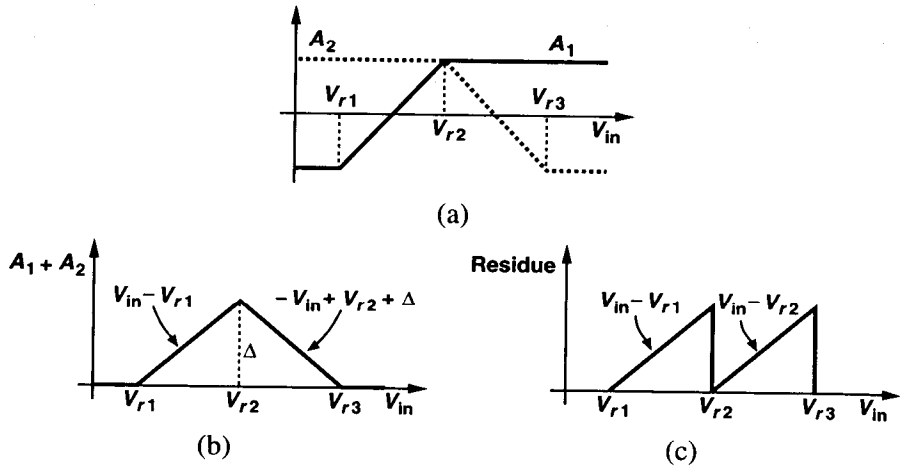


Fig. 6.40 (a) Input/output characteristics of two amplifiers; (b) sum of characteristics in (a); (c) residue in a two-step ADC.

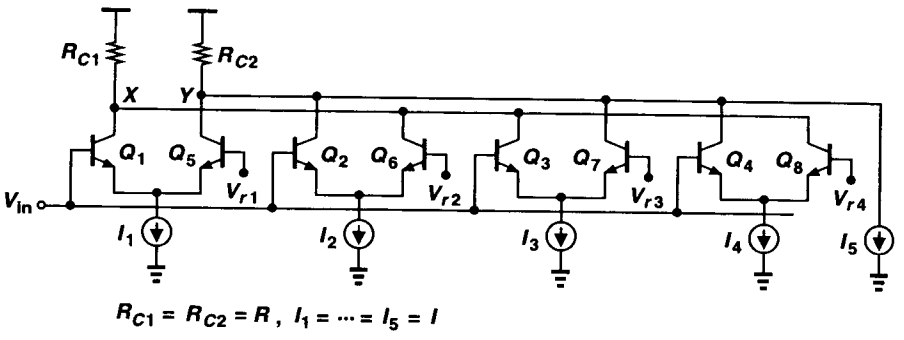


Fig. 6.41 Folding circuit.