Another way to implement a folding ADC

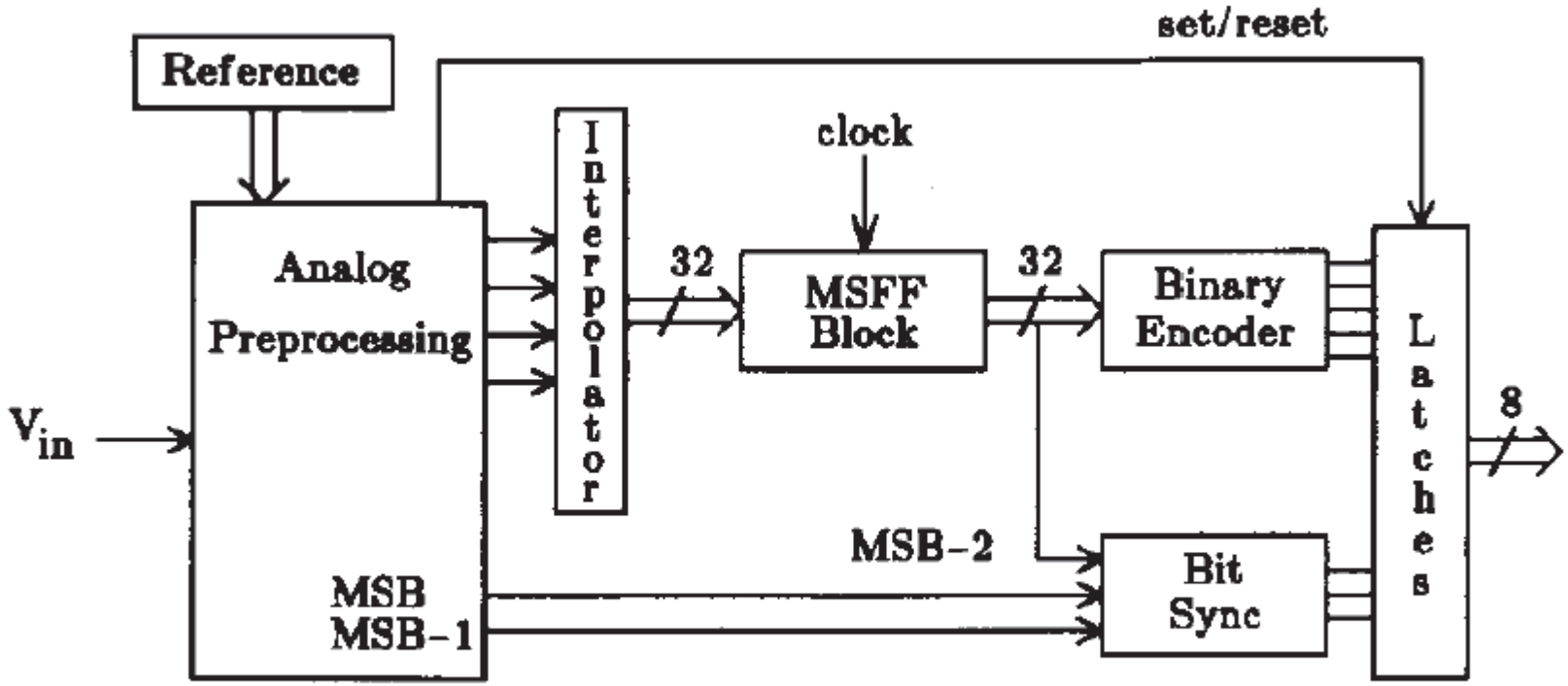


Fig. 12. System overview.

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

Coupled Differential Pair

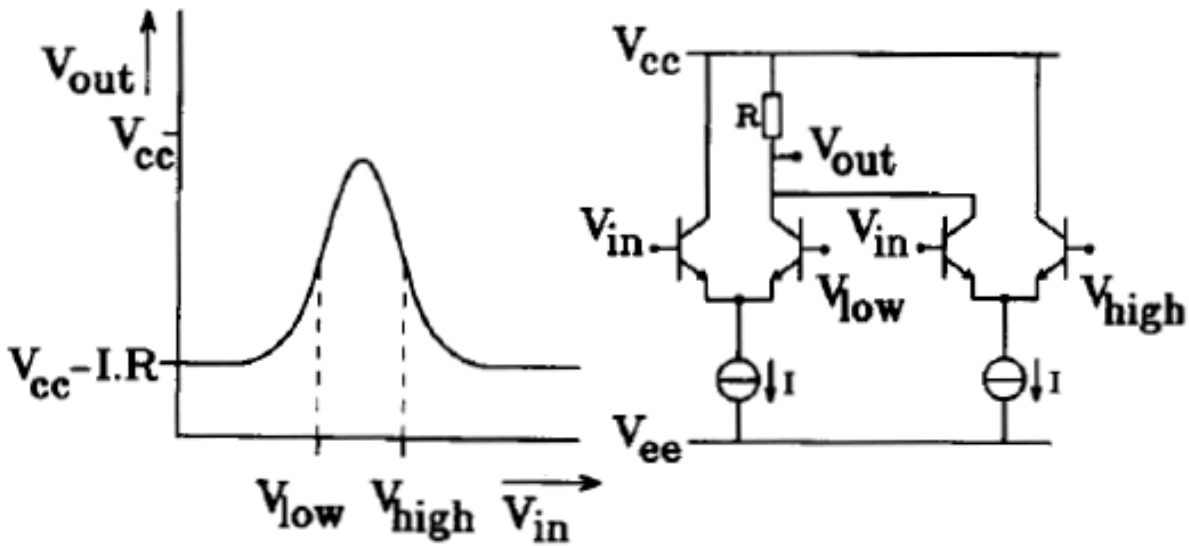


Fig. 2. Coupled differential pair.

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

1 bit ADC with 2 CDPs

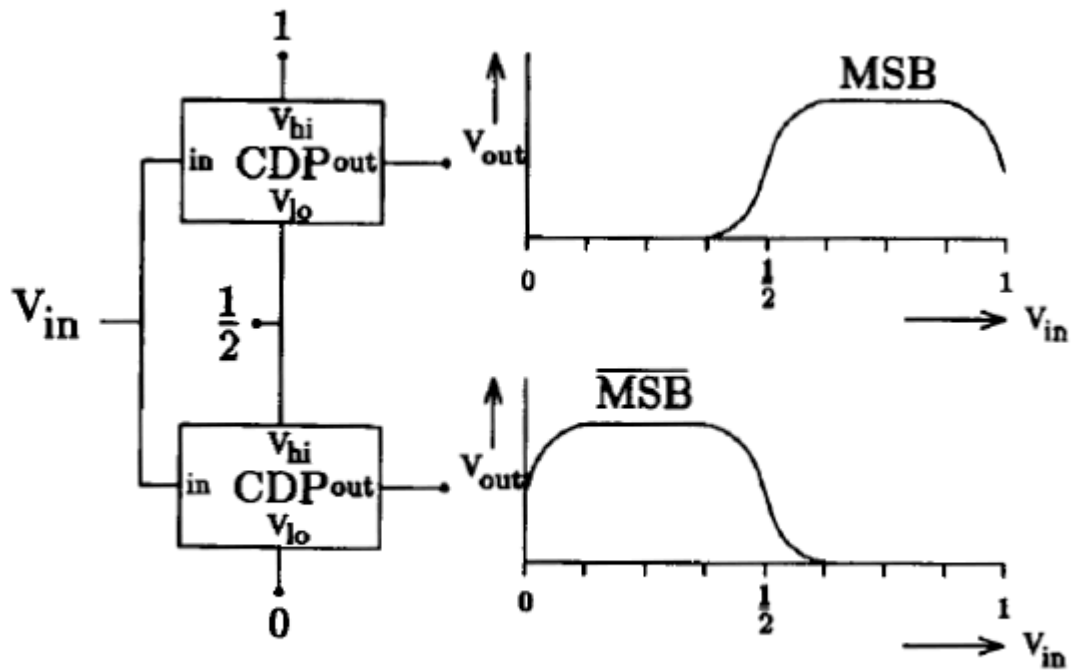


Fig. 3. 1-b ADC.

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

2-b ADC with 4 CDPs

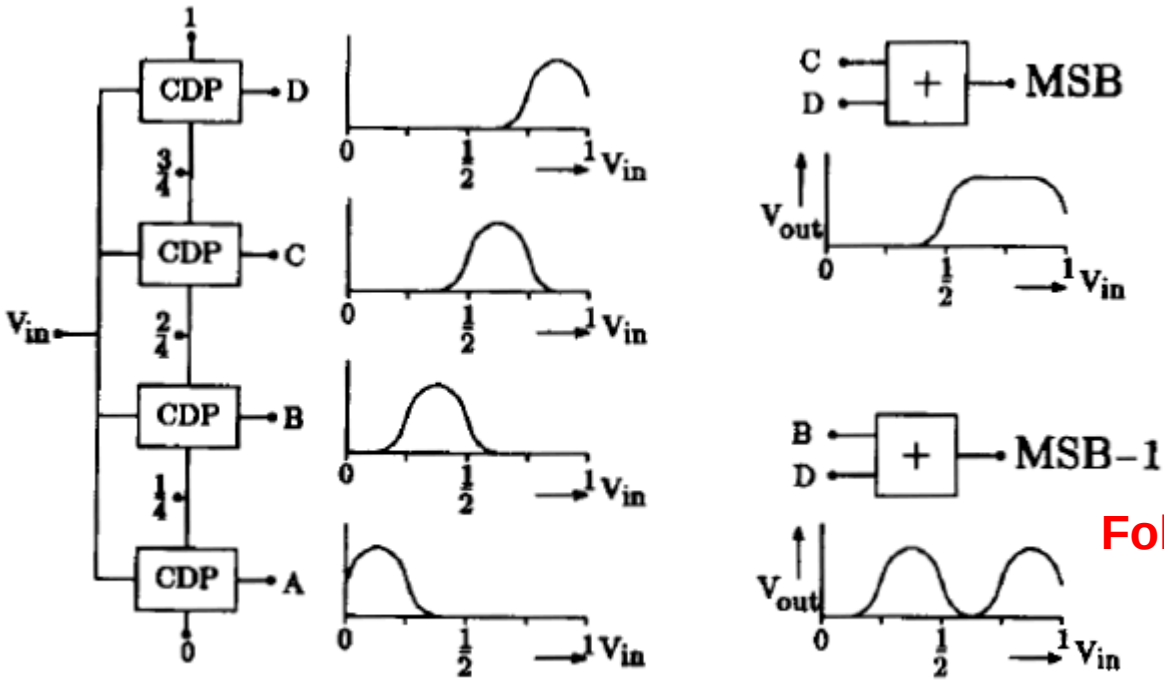


Fig. 4. 2-b ADC.

Folding rate = 4
4x f_{IN}

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

3-b ADC with 8 CDPs

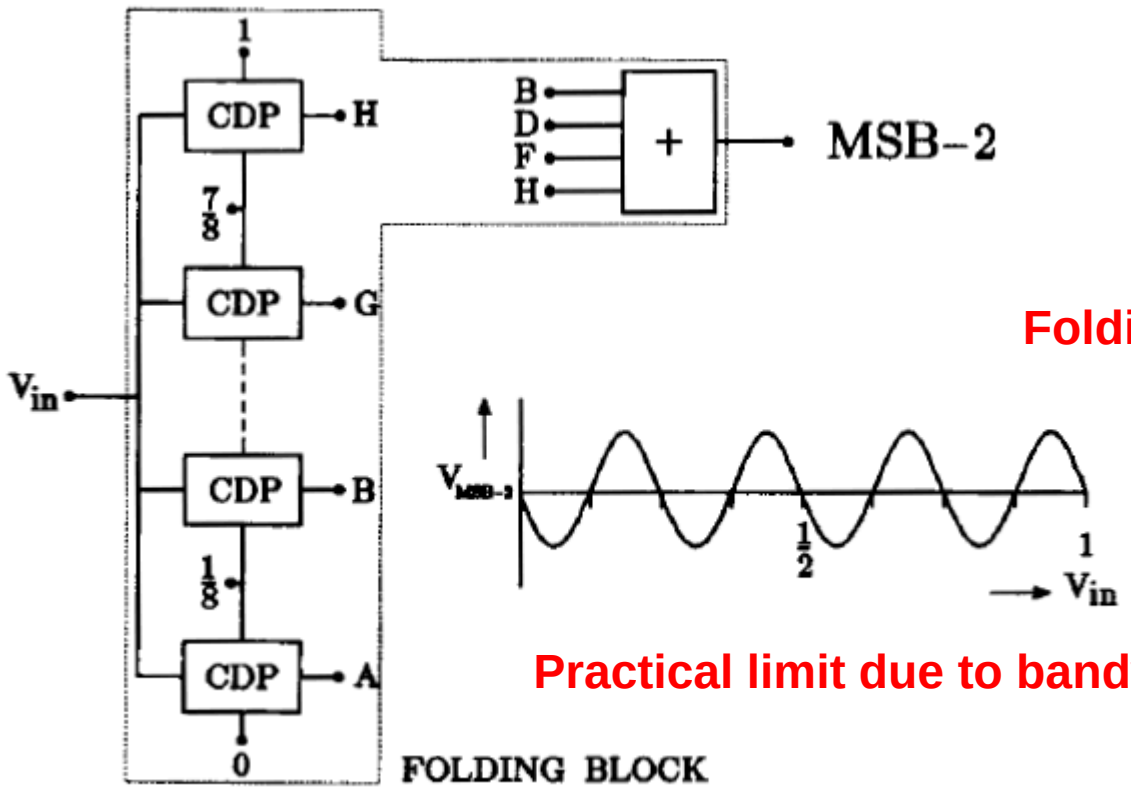


Fig. 5. 3-b ADC.

Folding rate = 8
8x f_{IN}

Practical limit due to bandwidth needed

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

I-Q folding; offset by ½ LSB

Resolution can be increased by 1 bit using parallelism without increasing folding rate. 4 folding blocks needed to get to 5 bits by folding alone.

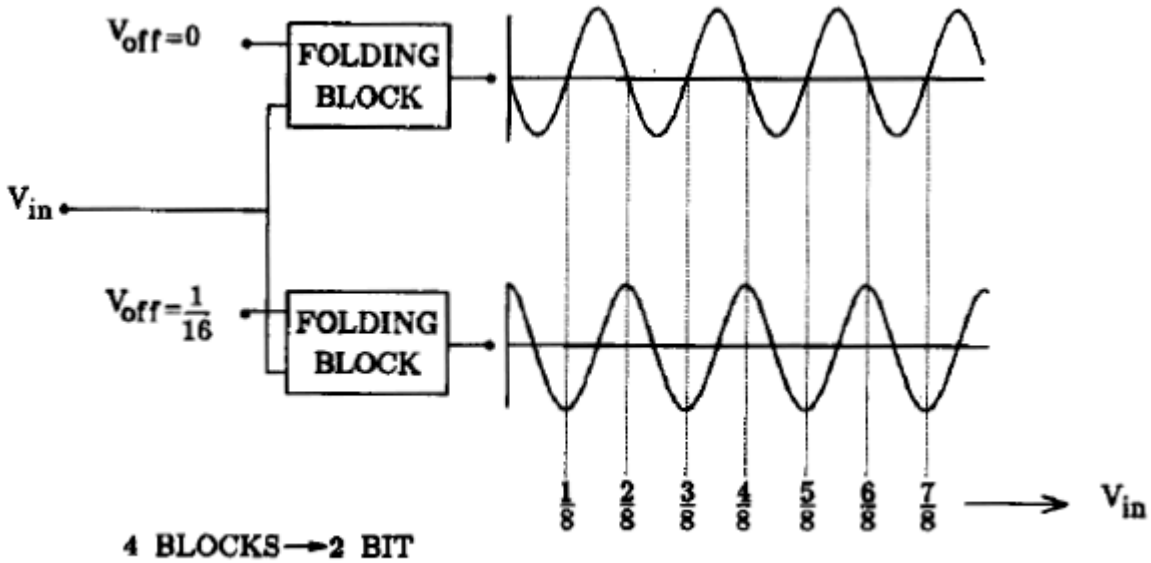


Fig. 6. Parallel use of folding blocks.

You could build all 8 bits this way, but the complexity would be as great As a flash converter. So, use interpolation to get the last 3 bits.

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

Fine bit generation through interpolation

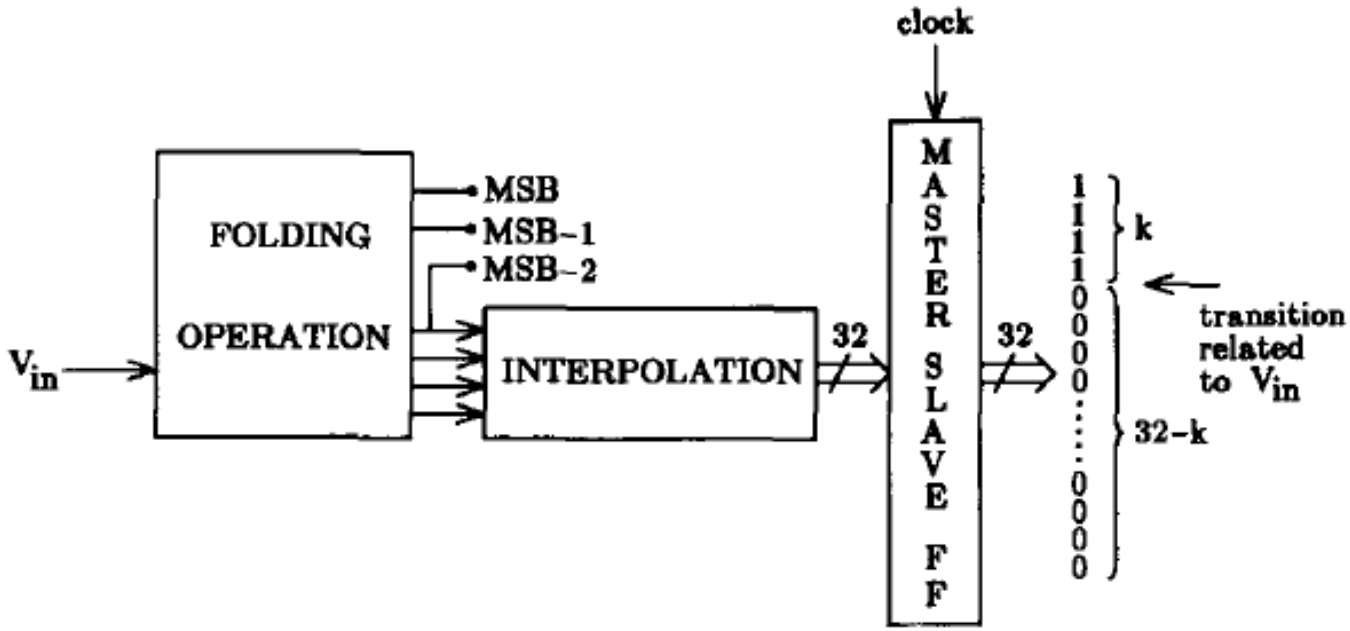


Fig. 9. Fine bit generation.

Interpolation rate = 8. provides last 3 bits

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

Resistive interpolator

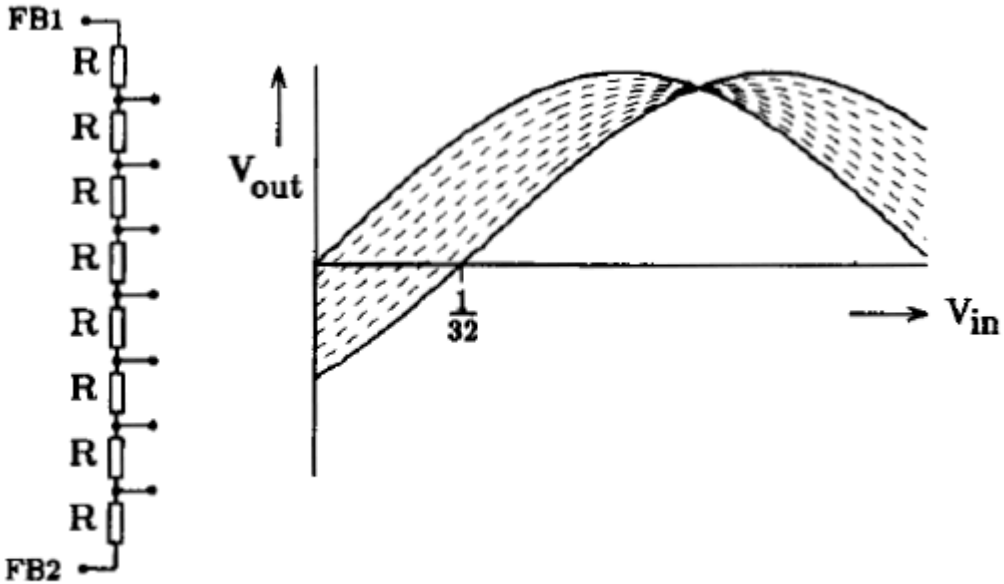


Fig. 7. Resistive interpolation.

Interpolation rate = 8. provides last 3 bits

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

Now, the MSFF comparators are all referenced to zero diff input. They are sensing zero crossings

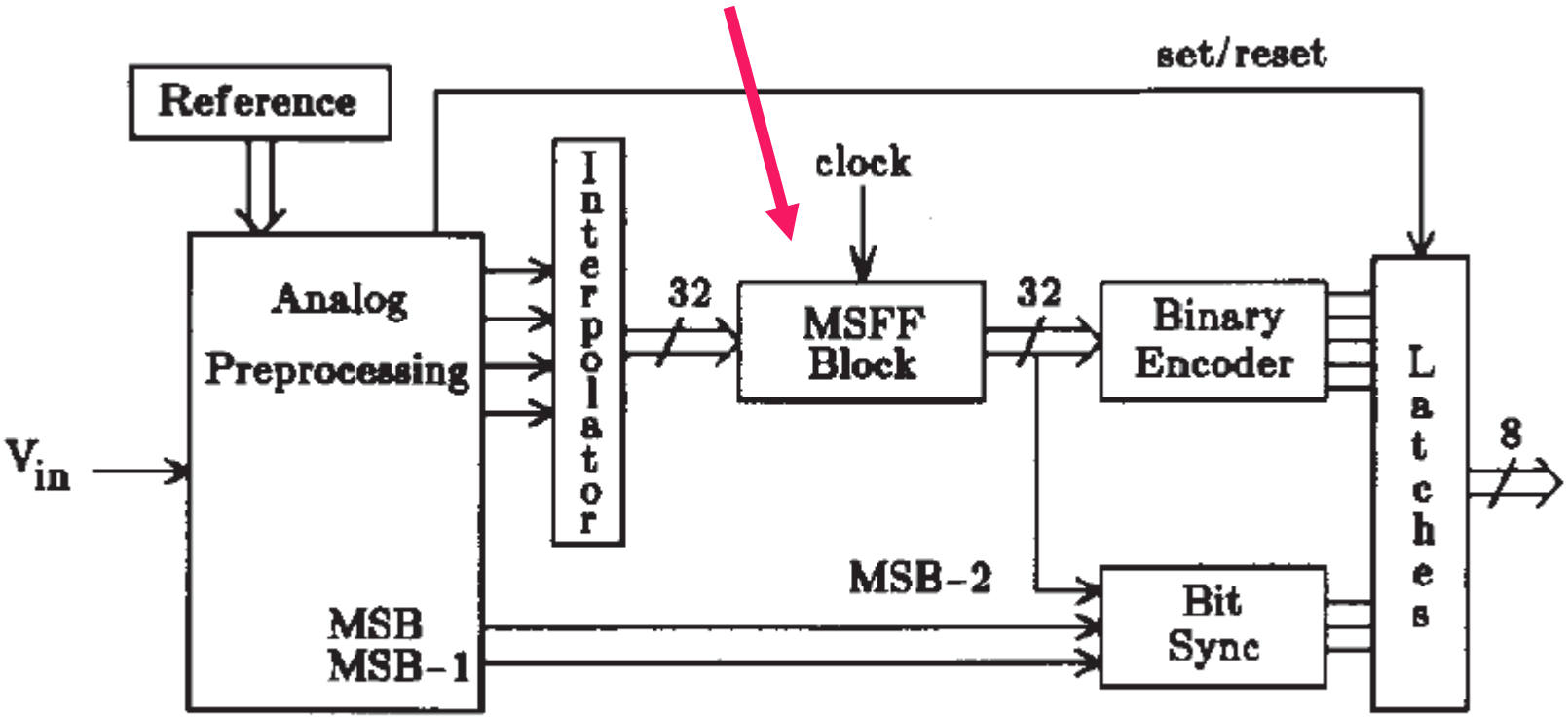


Fig. 12. System overview.

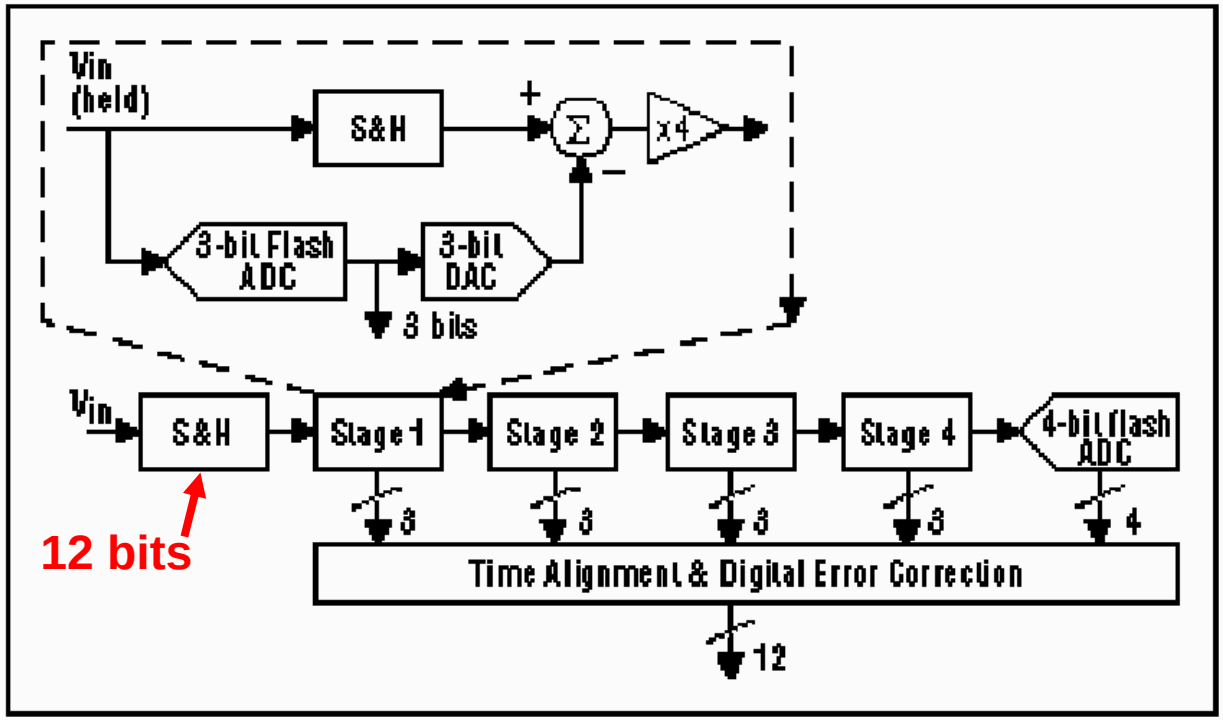
Total number of comparators is reduced (from flash) by folding rate: 256/8=32

J. Van Valburg and R. van de Plassche, An 8-b 650 MHz Folding ADC, IEEE JSSC, vol 27, #12, pp. 1662-6, Dec 1992

Pipeline architecture

Typically used up to about 100 MS/s

(Imaging, digital receiver, base station, HDTV, xDSL, cable modems, ethernet)



'. Pipelined ADC with four 3-bit stages (each stage resolves 2 bits)

Maxim AN383

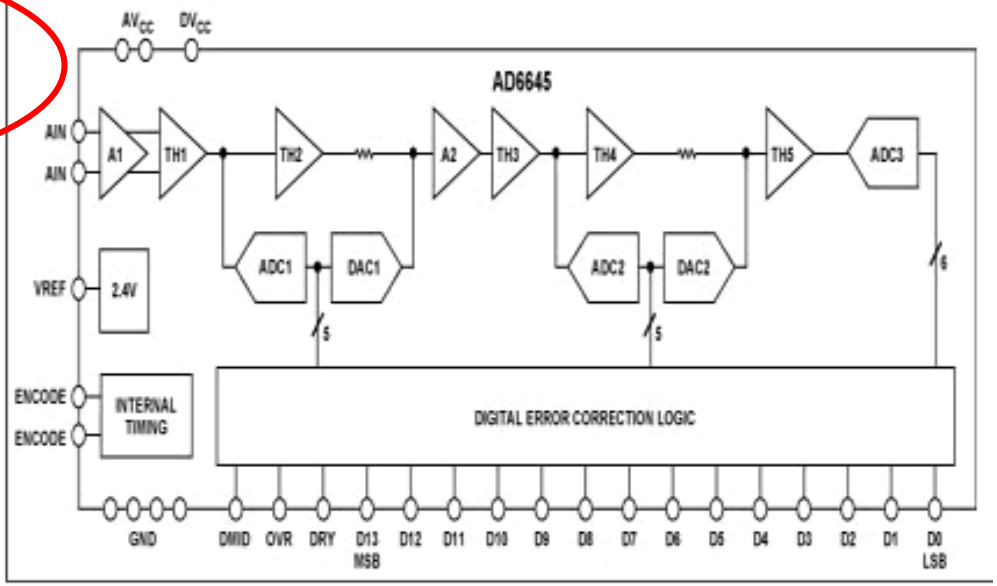
Pipeline example

- Increased sampling rate in exchange for latency
- First 4 stages: S/H; 3 bit flash; DAC; residue multiplied by 4x; 4 bit accuracy.
- 2 bits output per stage. Digital error correction uses 3rd bit to allow extra range in next stage. This can correct for offset errors.
- Final stage must have >4 bit accuracy.
- Shift registers needed for digital time alignment

14 bits; 105 MS/s

Specifications	
Res (Bits)	14bit
Thruput Rate	105MSPS
# of ADC Inputs	1
Supply V	Multi(+3.3, +5)
Pwr Diss (max)	1.75W
Interface	Par
Ain Range	2.2 V p-p
SNR (dB)	75dB
Pkg Type	QFP
Find Similar Products	

Functional Block Diagram



Features

- 75 dB SNR, Fin = 15 MHz up to 105 MSPS
- 72 dB SNR, Fin = 200 MHz up to 105 MSPS
- 89 dBc SFDR, Fin = 70 MHz up to 105 MSPS
- 100 dB Multitone SFDR
- IF Sampling to 200 MHz
- Sampling Jitter 0.1 ps
- 1.5 W Power Dissipation
- Differential Analog Inputs
- Pin-Compatible to AD6644
- Twos Complement Digital Output Format
- 3.3 V CMOS Compatible
- DataReady for Output Latching

Analog Devices AD6645 6/2003

20 Gs/s 8-b Pipelined – Interleaved ADC

High bandwidth oscilloscope application - Agilent

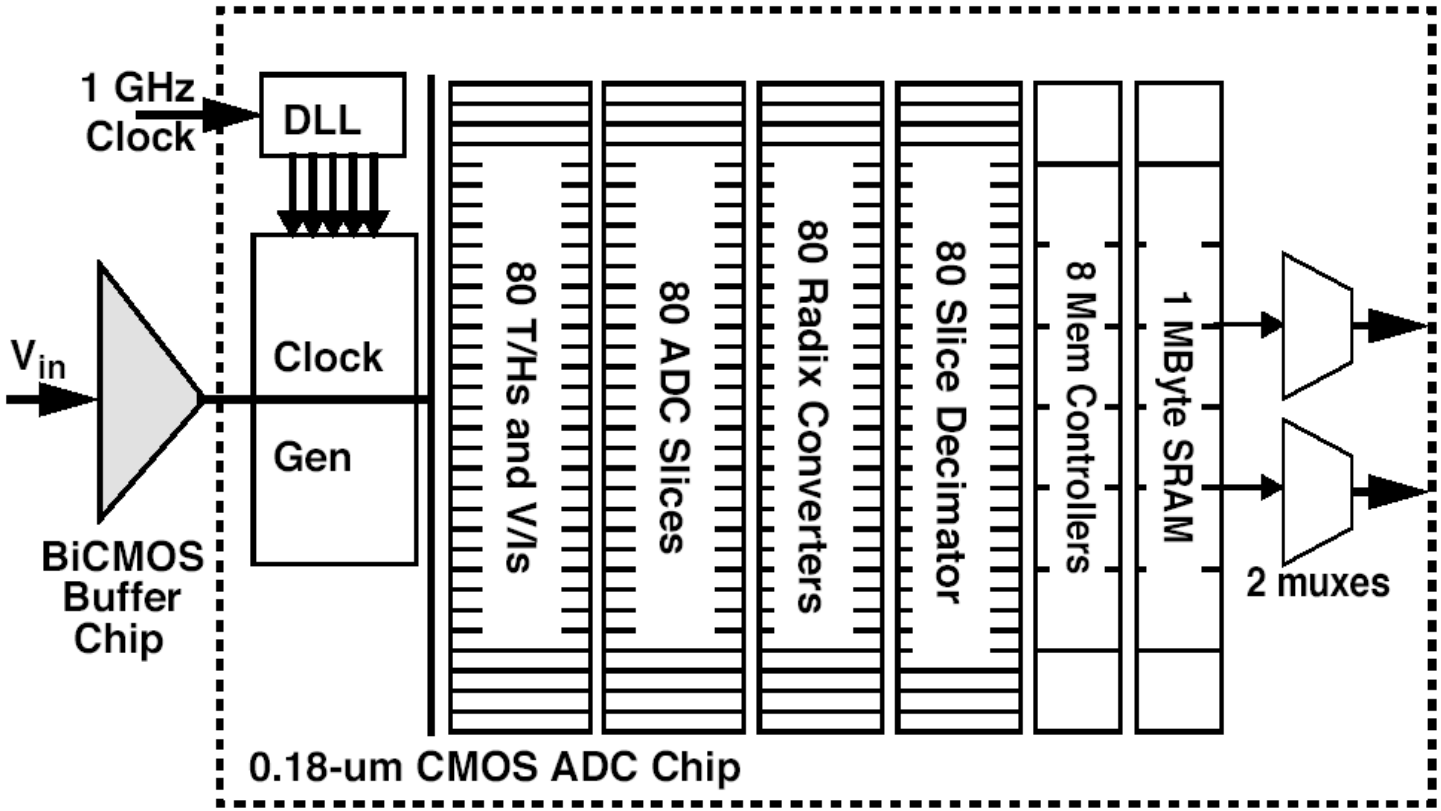


Figure 18.1.1: ADC architecture.

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

Design details

- BiCMOS buffer chip used to drive the 4pF input capacitance of the ADC
- ADC is organized in 80 slices – parallelism used to increase throughput
  - Each block works at 250 MS/s
  - T/H, V-I converter, current-mode pipelined 1-bit ADC
  - Residue is amplified by 1.6X
  - Radix 1.6 to binary conversion
  - Data capture in 1MB on-chip SRAM

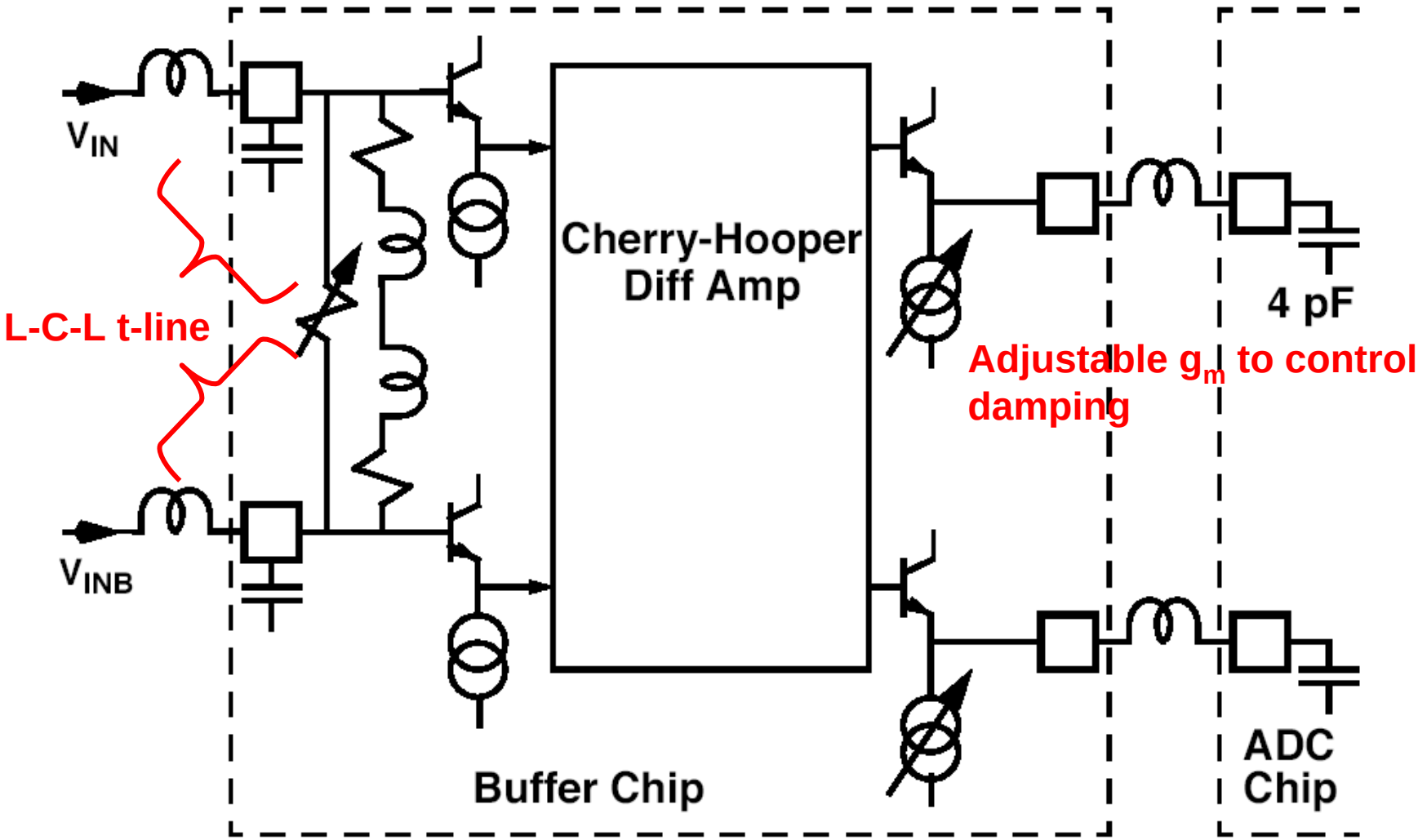


Figure 18.1.2: Input buffer chip - simplified schematic.

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

Clock Generation

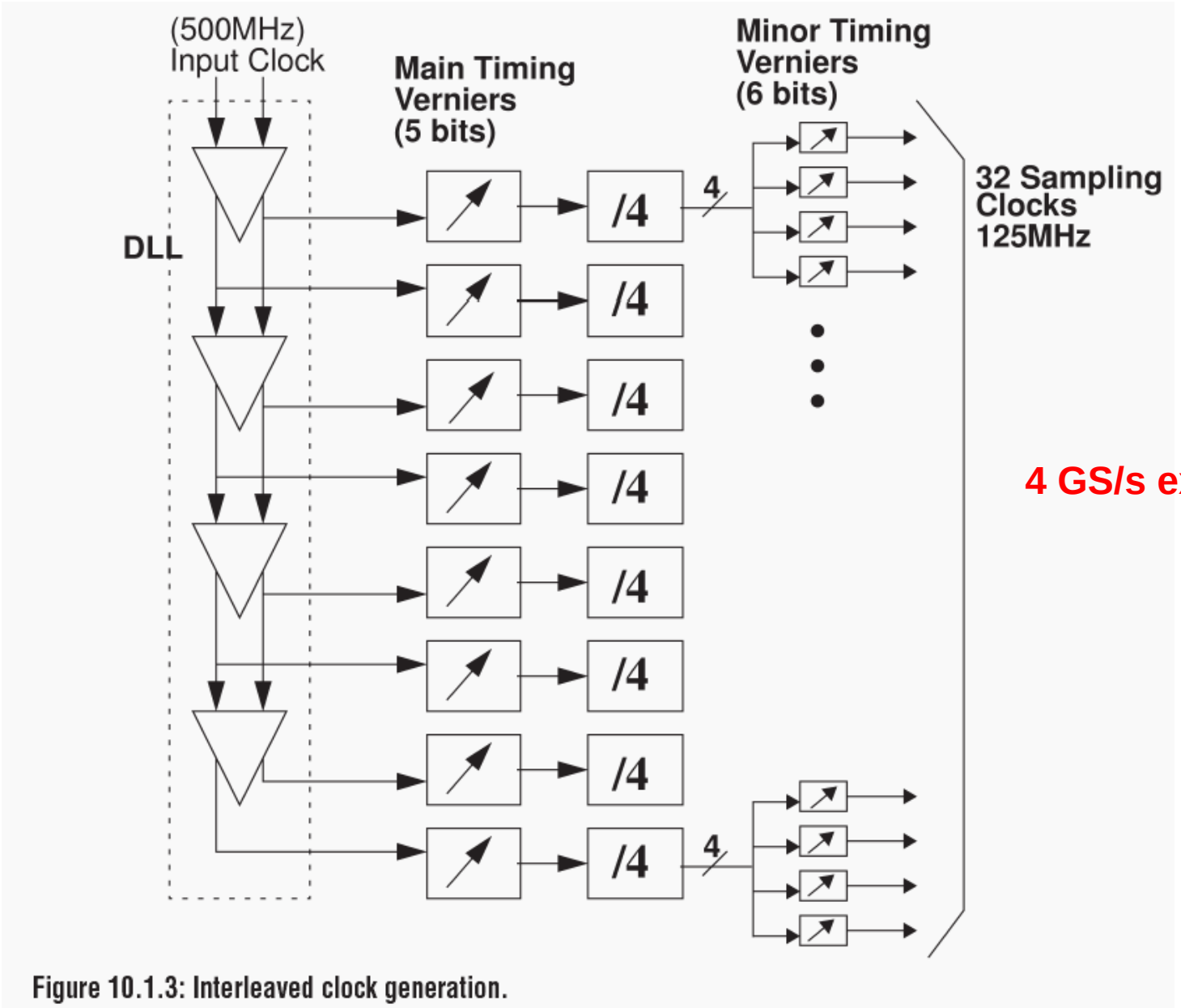


Figure 10.1.3: Interleaved clock generation.

4 GS/s example

K. Poulton, et al."A 4Gs/s 8b ADC in 0.35 um CMOS," ISSCC 2002, paper 10.1.

Clock generation

- The 20 GS/s ADC requires 80 250 MHz clocks, each offset by 50 ps with error < 1ps
- 1 GHz clock; 5 DLL stages => 5 diff clocks
- Interpolate to get 20 clocks
- Divide by 4 to get 80 clocks
- Each has digital time adjustment

Track-Hold slice

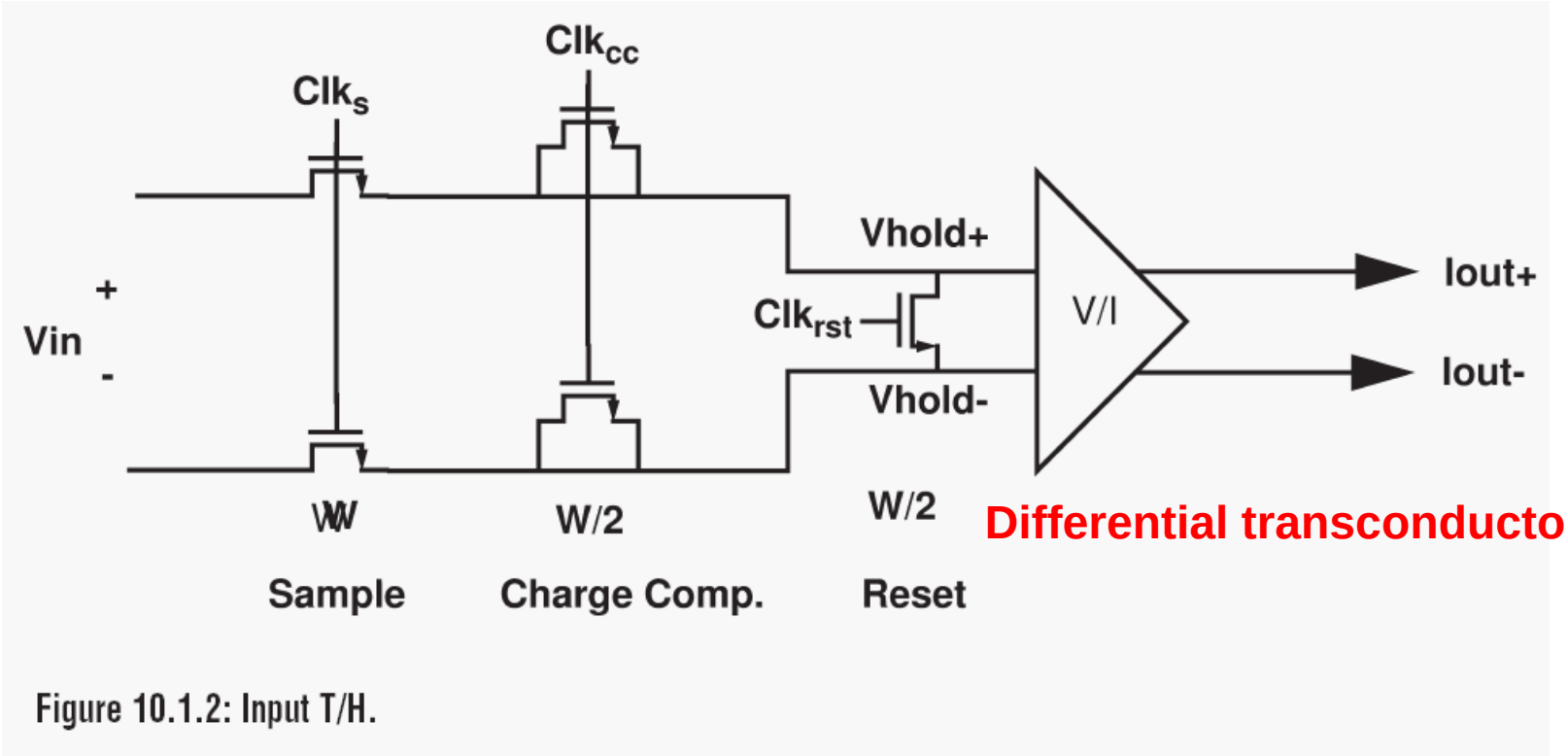


Figure 10.1.2: Input T/H.

K. Poulton, et al."A 4Gs/s 8b ADC in 0.35 um CMOS," ISSCC 2002, paper 10.1.

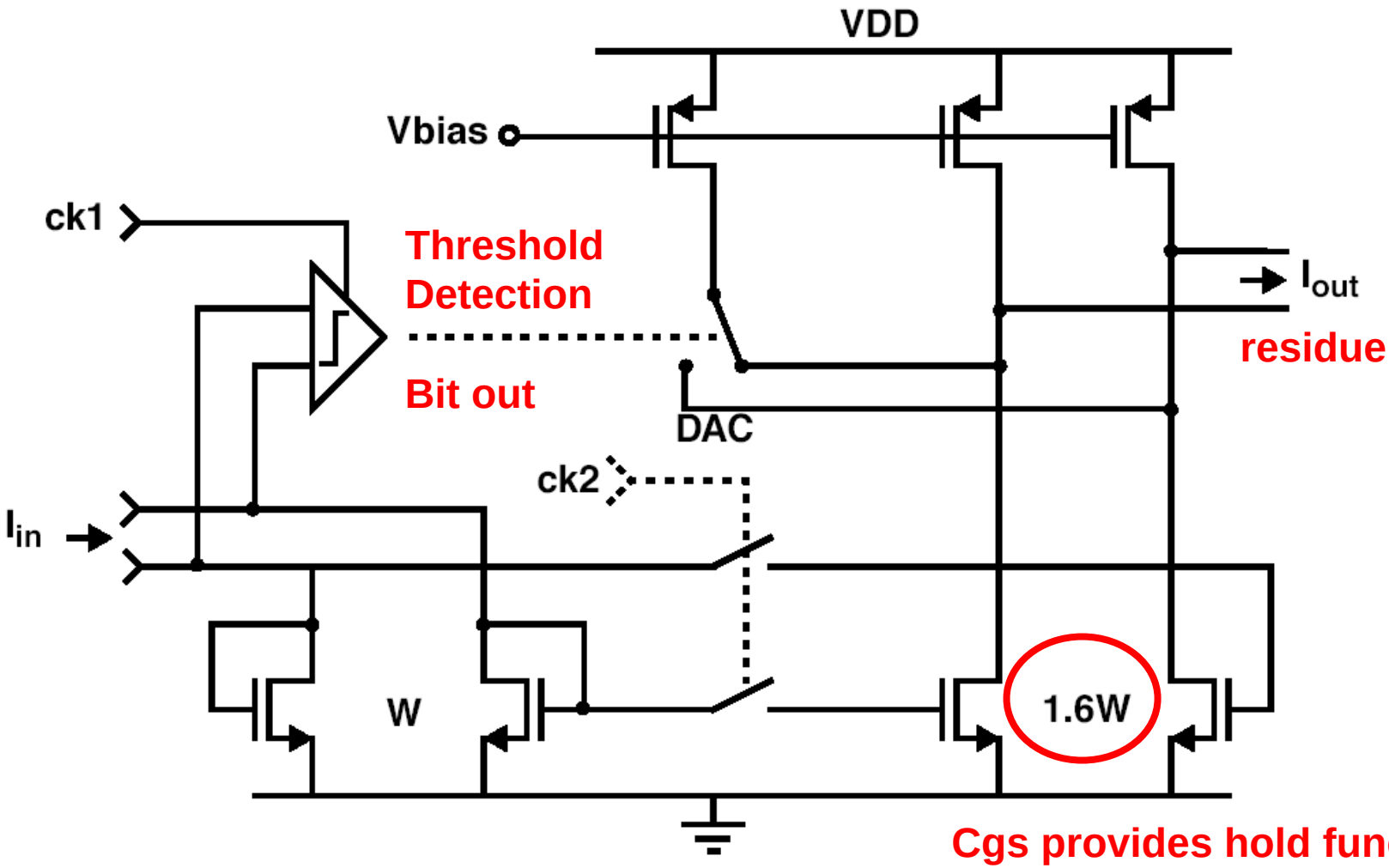


Figure 18.1.3: Simplified pipeline stage schematic.

12 stages of radix 1.6 produces 12 bits; convert to 8 bits binary

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

Extensive calibration

- Sawtooth input
  - Per slice gain and offset correction – 160 DACs on-chip
  - Gain coefficients loaded into radix converter
- Pulse input
  - Fourier analysis used to set timing adjustments

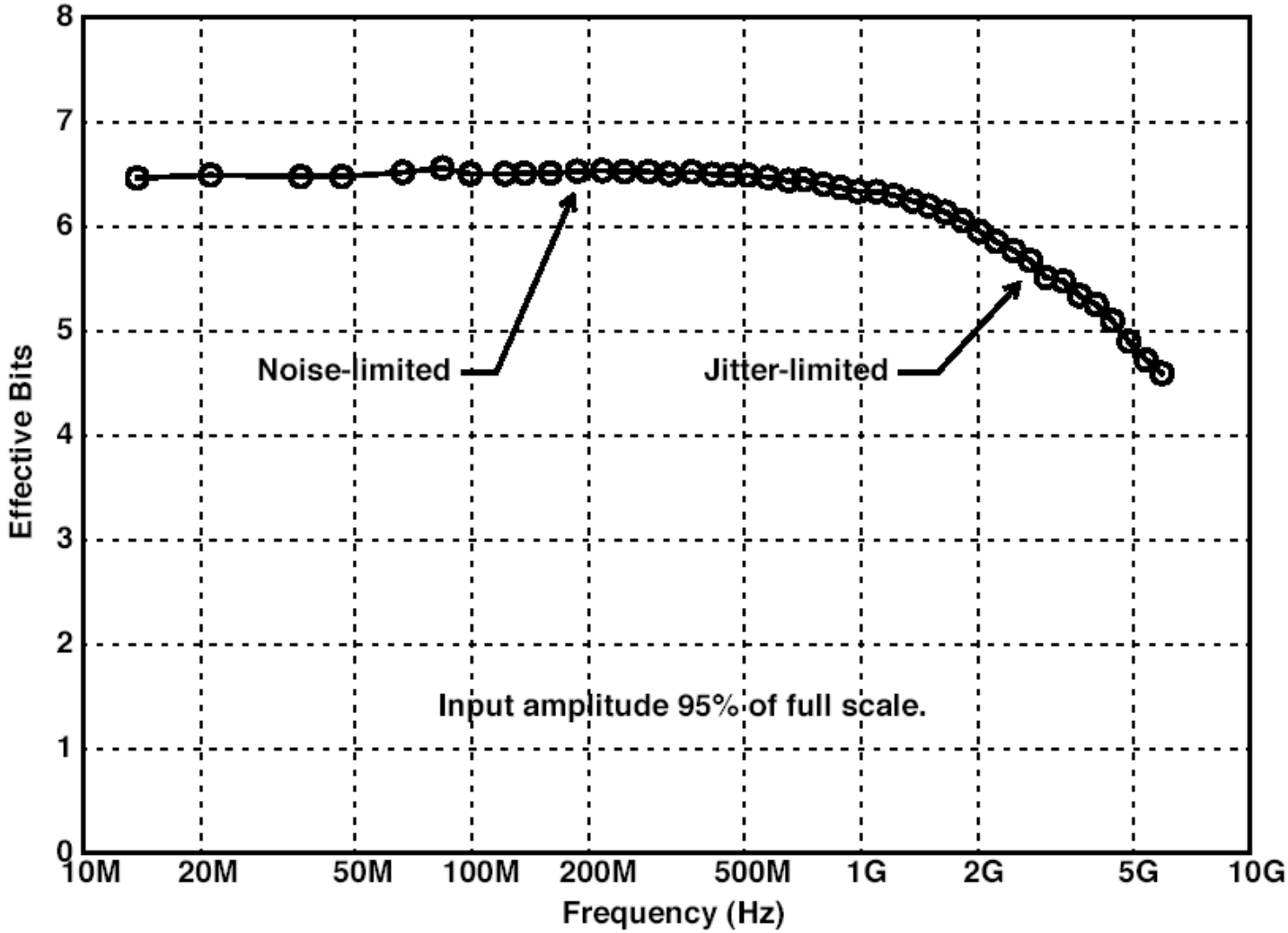


Figure 18.1.6: Effective bits vs. input frequency.

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

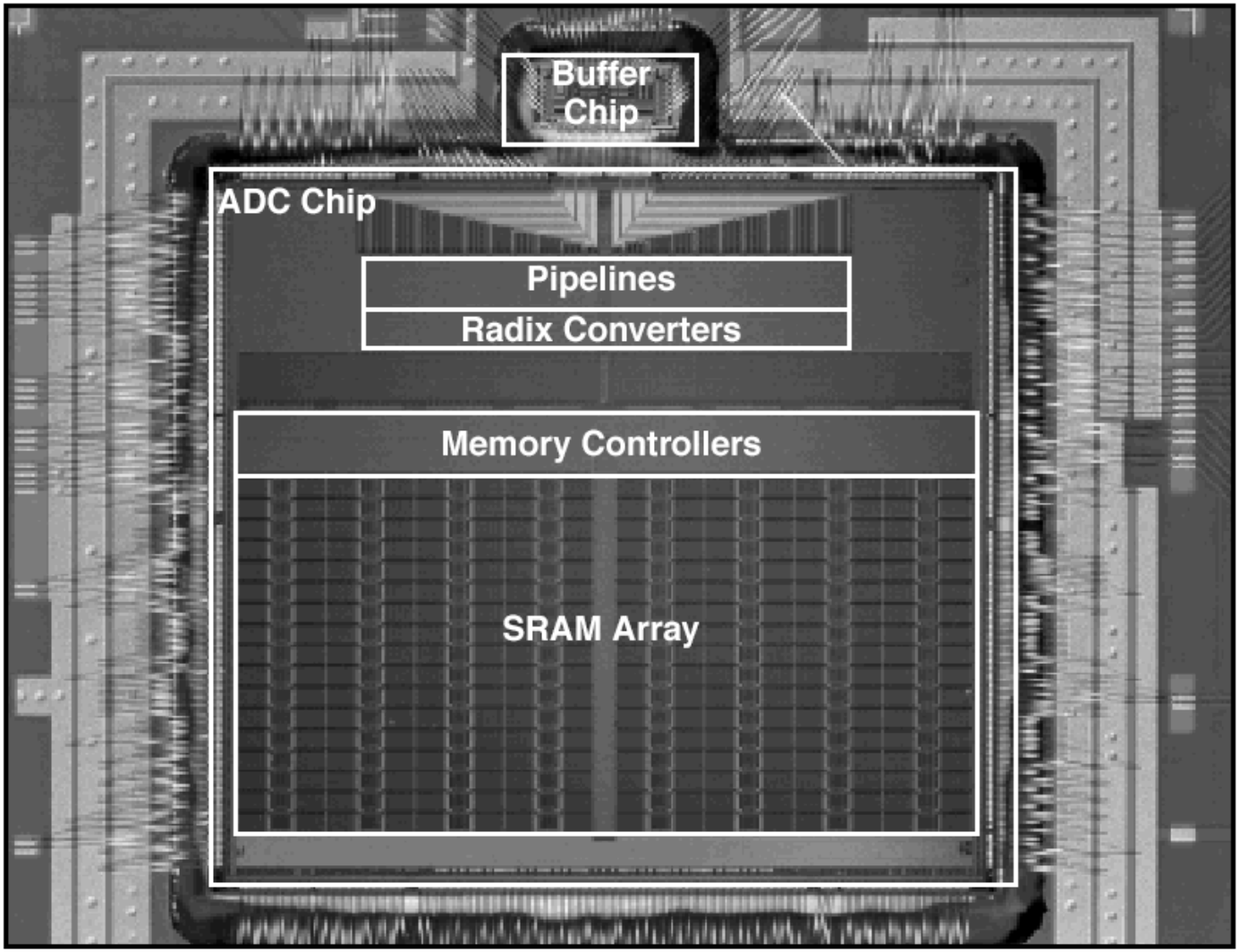


Figure 18.1.5: 1.2 x 2.6mm BiCMOS chip, 14 x 14mm CMOS chip.

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

Sample Rate	20 GSa/s	
Resolution	8 bits	
INL Intrinsic With linearity correction	 ±1.7 LSBs ±0.4 LSBs	
DNL	±0.3 LSBs	
Bandwidth	6.6 GHz	
Accuracy @ 500 MHz input @ 6 GHz input	 6.5 effective bits 4.6 effective bits	
Jitter	0.7 ps rms	
Input Range	0.25 Vpk differential	
	Buffer Chip	**ADC Chip**
Input Capacitance	0.2 pF	4 pF
Power	1 W	9 W
Chip Size	1.2 x 2.6 mm	14 x 14 mm
Technology	40-GHz SiGe BiCMOS	0.18-mm CMOS
Transistors	1000	50M
Package	438-ball BGA	

5x any other CMOS ADC

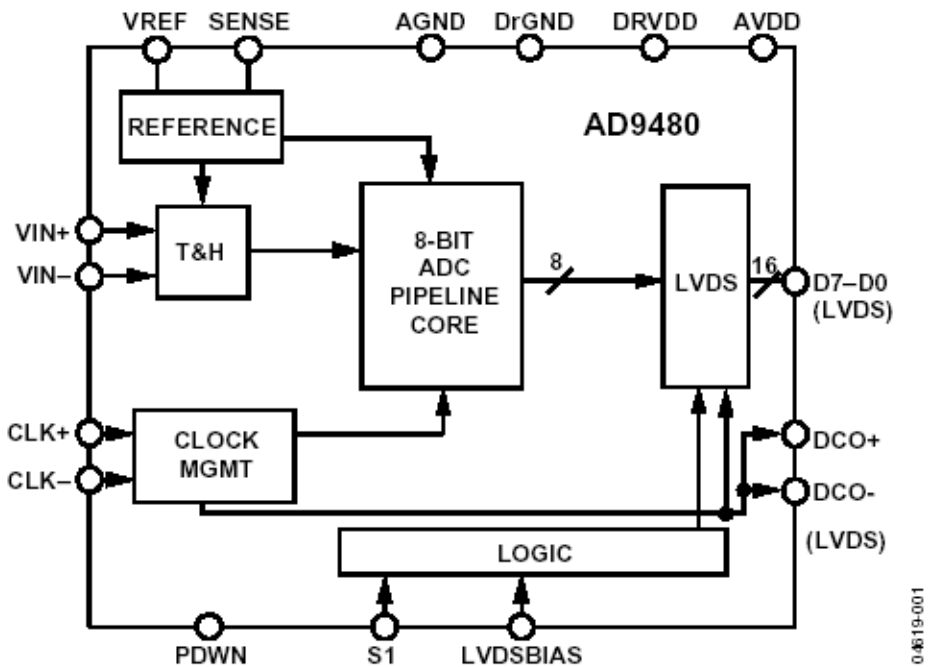
Figure 18.1.7: ADC results.

K. Poulton, et al."A 20Gs/s 8b ADC with a 1MB Memory in 0.18 um CMOS," ISSCC 2003, paper 18.1.

8-Bit, 250 MSPS 3.3 V A/D Converter

AD9480

FUNCTIONAL BLOCK DIAGRAM



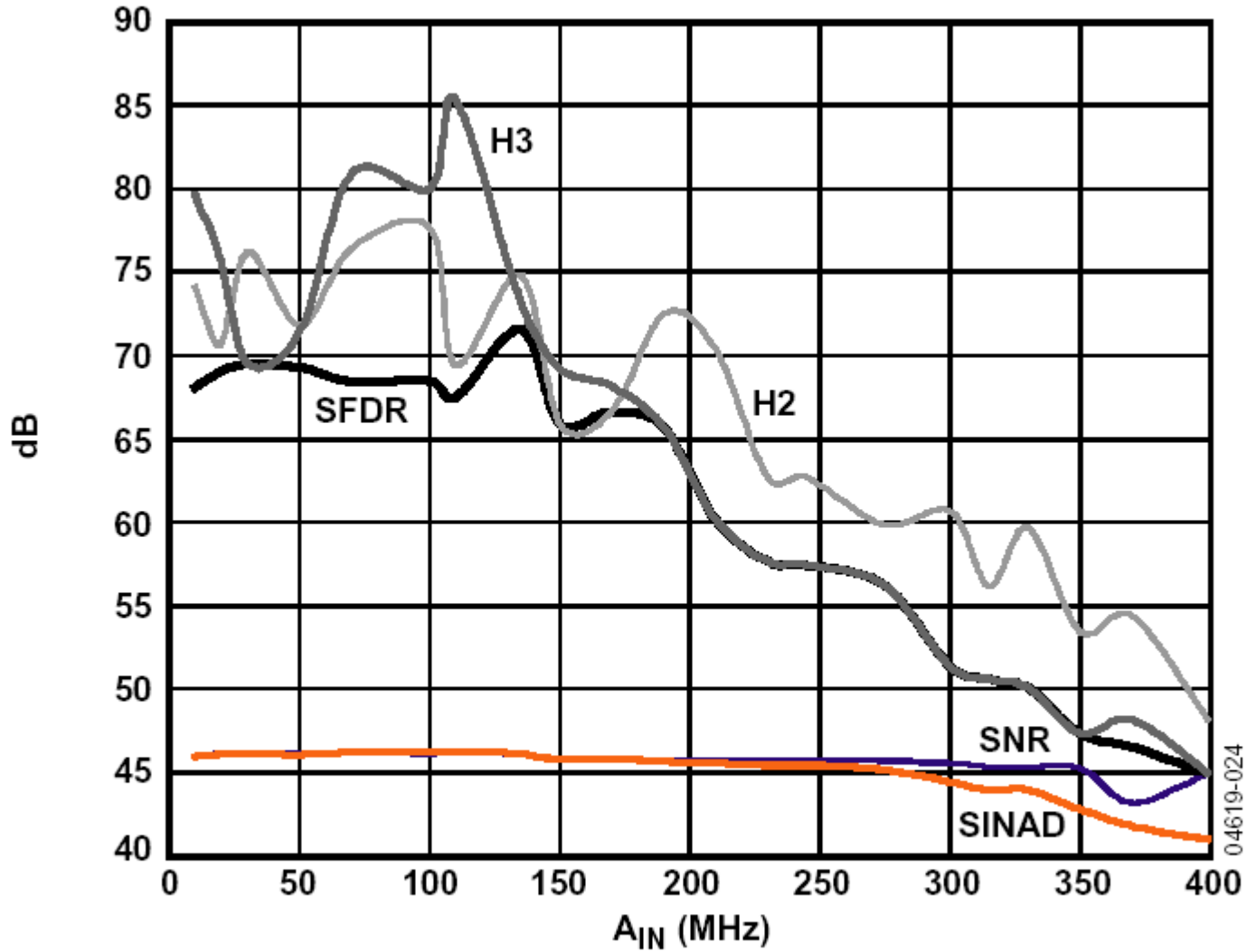
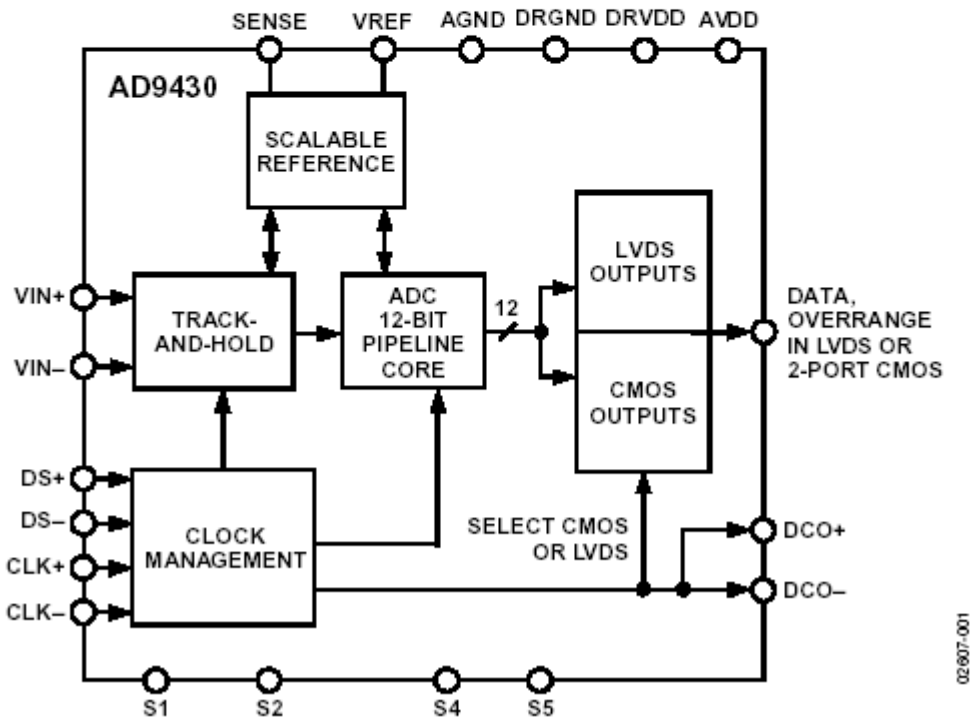


Figure 8. Analog Input Frequency Sweep, A_{IN} = −1 dBFS, FS = 1 V, f_S = 250 MSPS

12-Bit, 170/210 MSPS 3.3 V A/D Converter

AD9430

FUNCTIONAL BLOCK DIAGRAM



Analog Devices 11/2004

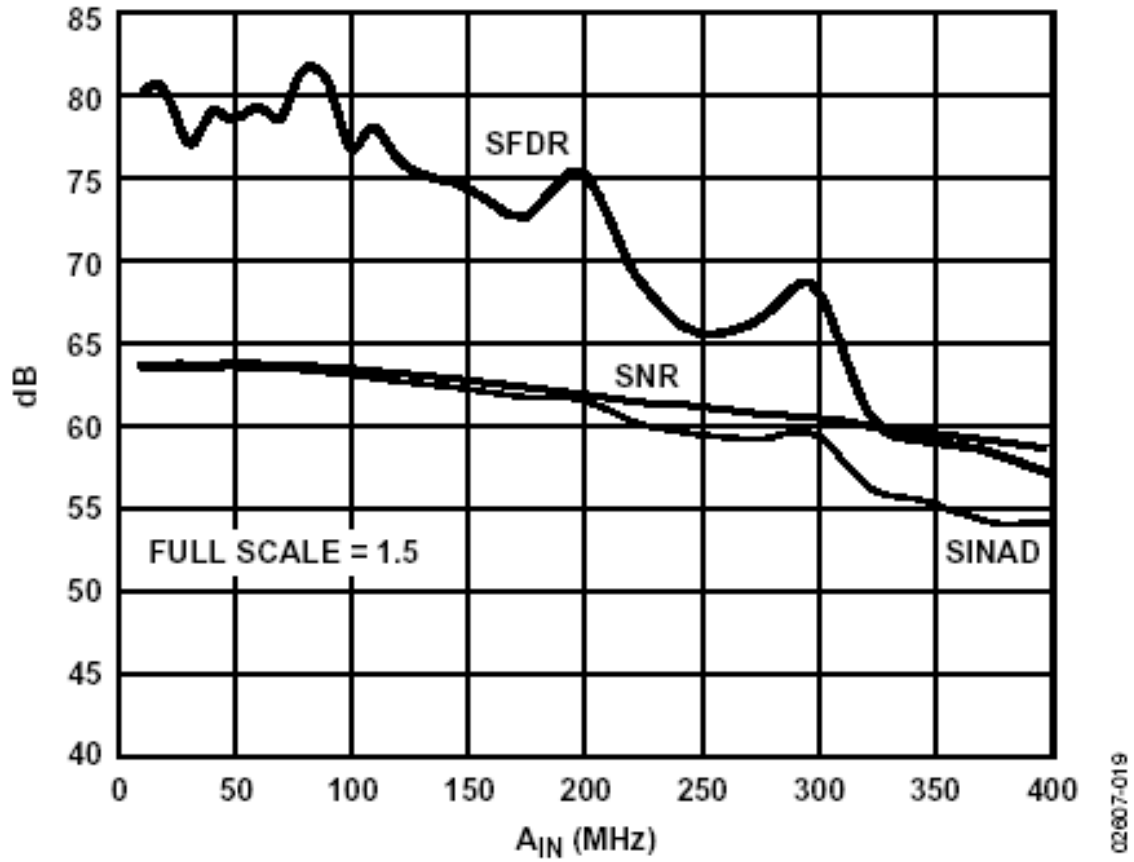
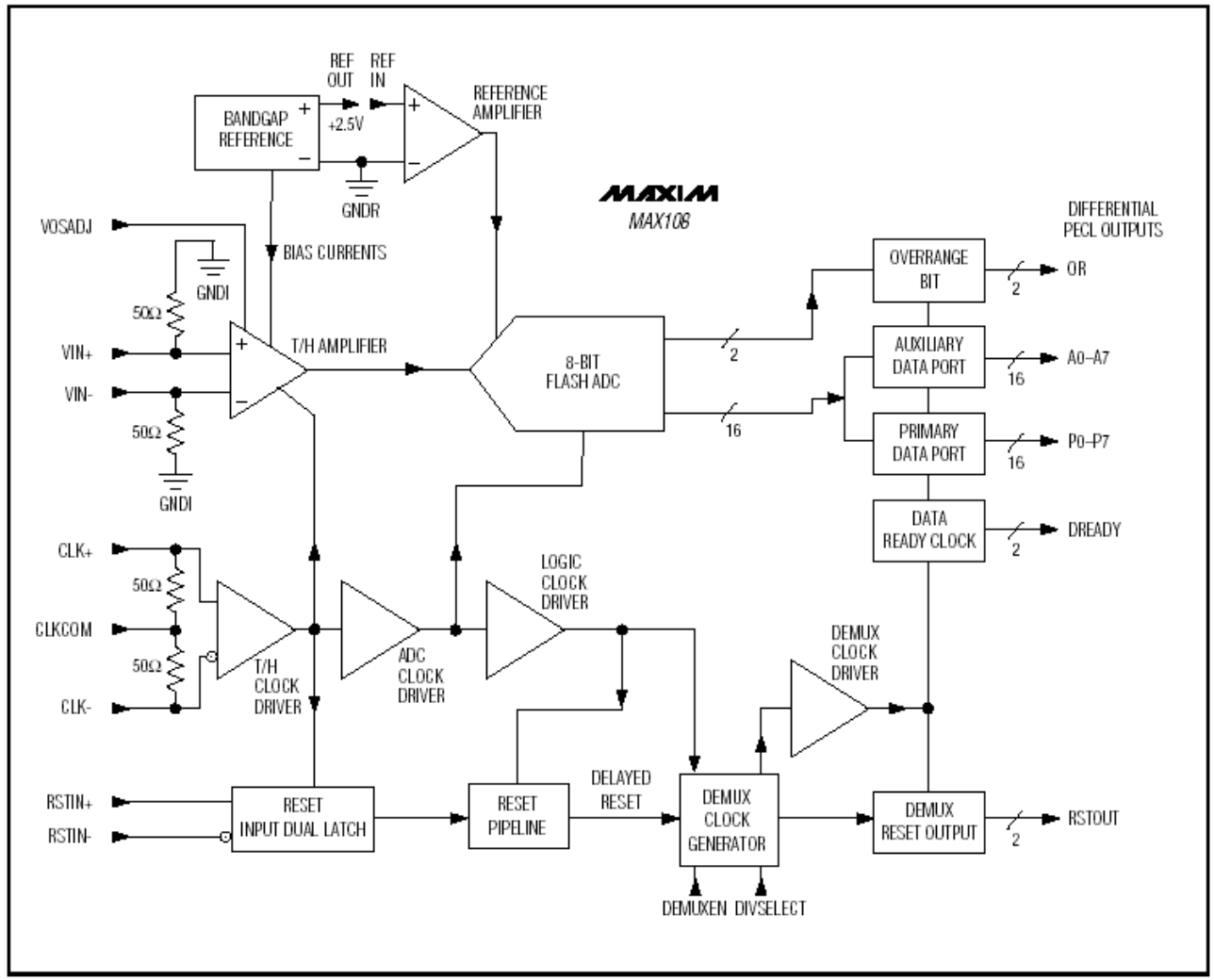
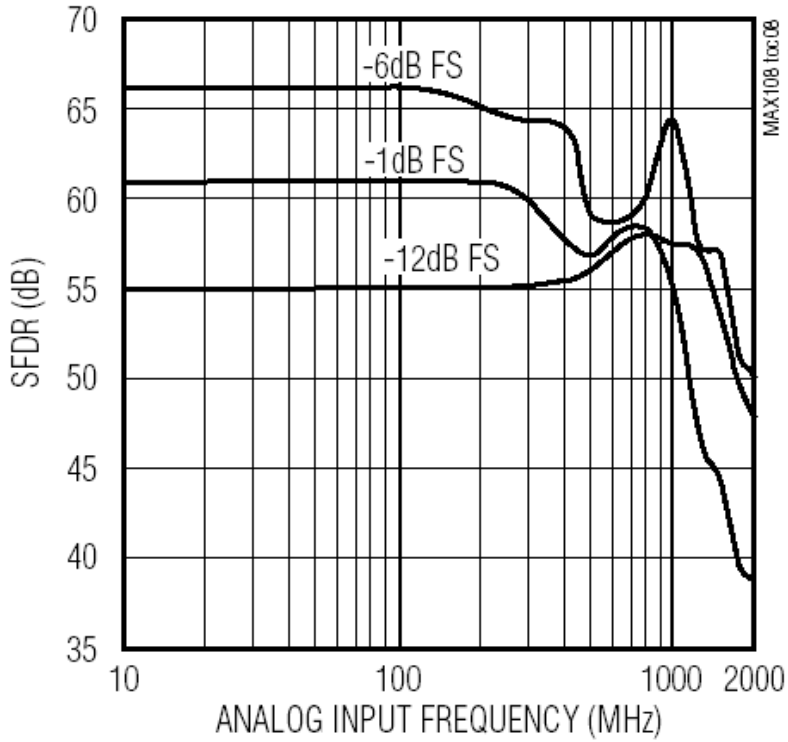


Figure 19. SNR, SINAD, and SFDR vs. A_{IN} Frequency, f_S = 210 MSPS, A_{IN} @ –0.5 dBFS, LVDS Mode

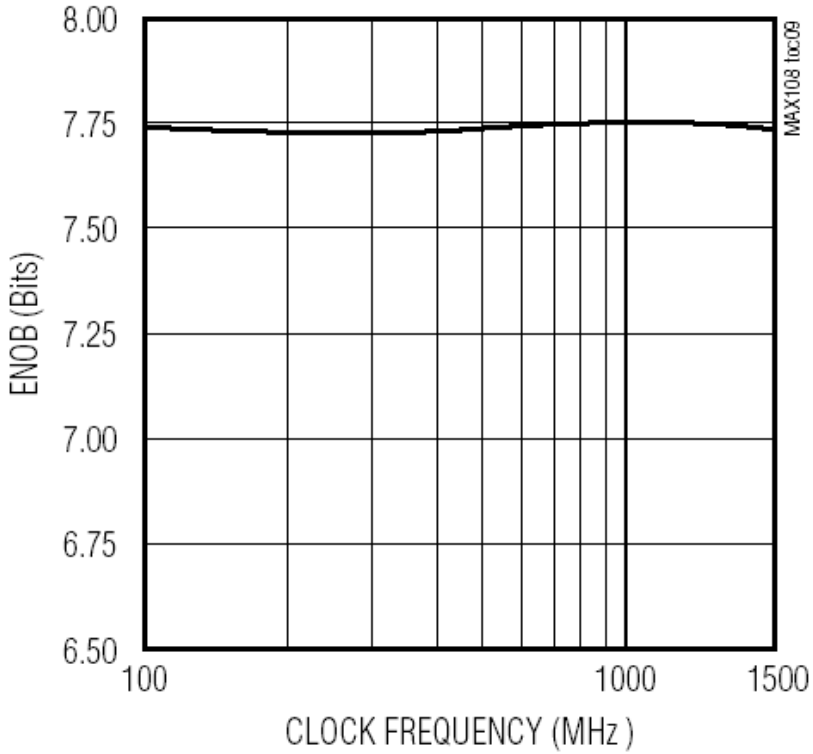
±5V, 1.5Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier



SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY (DIFFERENTIAL ANALOG INPUT DRIVE)



EFFECTIVE NUMBER OF BITS vs. CLOCK FREQUENCY (f_{IN} = 250MHz, 1dB FS)



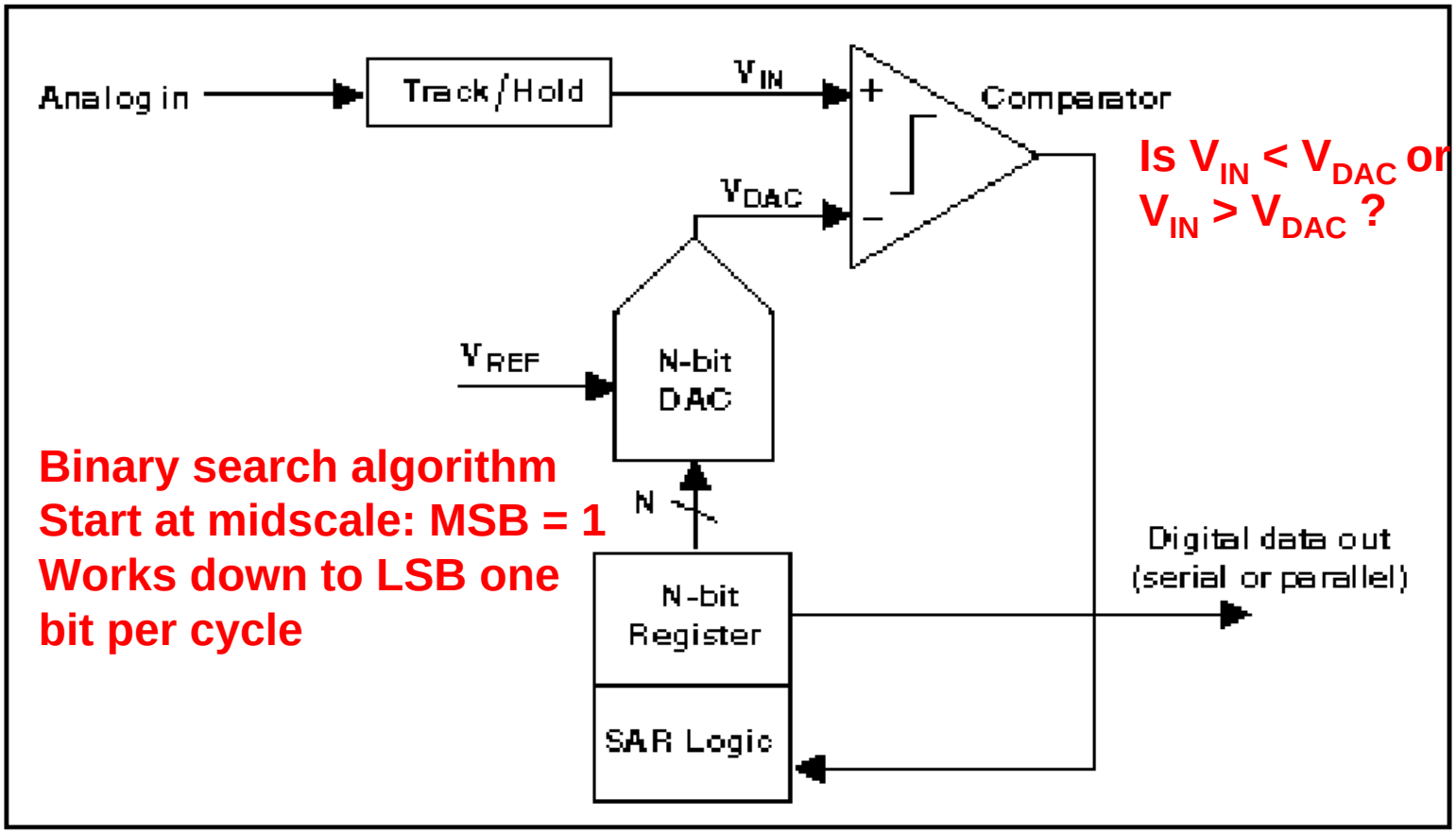
Maxim Integrated Products MAX108

Applications

Digital RF/IF Signal Processing
Direct RF Downconversion
High-Speed Data Acquisition
Digital Oscilloscopes
High-Energy Physics
Radar/ECM Systems
ATE Systems

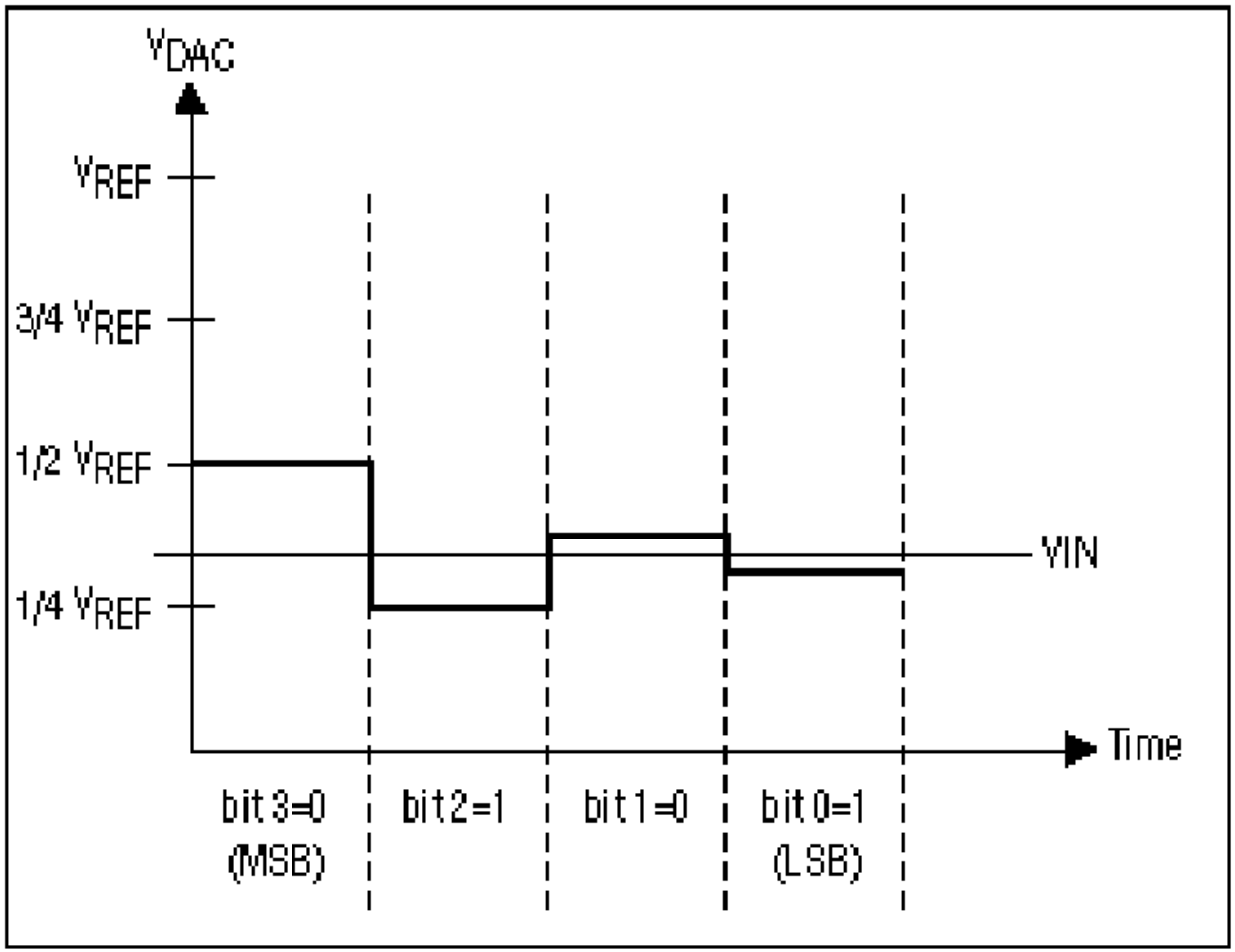
Successive Approximation ADC (SAR ADC)

Up to 5 MS/s
8 to 18 bits
Low power



Simplified N-bit SAR ADC architecture

Maxim AN387



. *SAR operation (4-bit ADC example)*

Maxim AN387