Homework #3 ECE594A Spring 2005

Due Wed, May 4. Turn in at class or by 5pm.

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1. a. Write a description of how direct digital frequency synthesis works. Explain how specific DAC nonidealities can degrade DDS spectral (dynamic) performance. [1]
b. Explain why the RZ DAC output format can provide improved linearity and SFDR.

2. a. An ADC has a full scale input voltage of 1.5V. A noise power of – 74 dBm was measured by performing a 2048 sample FFT on the digital output data. Determine the ENOB of this ADC.
b. The largest harmonic spur within the Nyquist bandwidth has a power of -60 dBm. What is the SFDR of this ADC?

3. Design and simulate the CMOS comparator shown in Fig. 7.27 of Razavi, "Data Conversion System Design." Evaluate the regeneration time as you sweep the differential input voltage through the comparator threshold.

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[1] You may find some helpful information on the Analog Devices website. In particular, application note AN237. Also, A. Bugeja et al.,"A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance," IEEE JSSC Vol 34, #12, pp. 1719-1731, Dec. 1999.