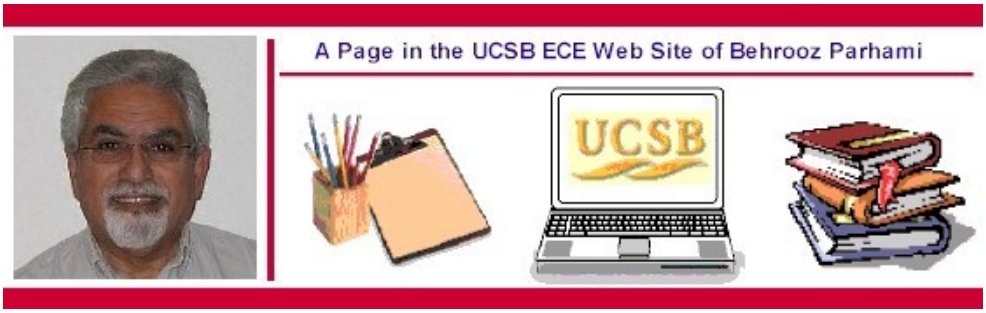

ECE 154: Information on Previous Offerings

Behrooz Parhami: 2009/01/06 || E-mail: parhami at ece.ucsb.edu || Other contact info at: Bottom of this page
Go up to: B. Parhami's course syllabi or his home page

Special note: Web links in the following descriptions may be out of date. Please refer to the most recent offering of ECE 154 for up-to-date information.

Link to the most recent offering of ECE 154: Intro. to Computer Architecture

Previous offerings of ECE 154

- ECE 154: Winter quarter 2008
- ECE 154: Winter quarter 2007
- ECE 154: Winter quarter 2006
- ECE 154: Summer session 2005
- ECE 154: Summer session 2004
- ECE 154: Summer session 2003
- ECE 154: Summer session 2002
- ECE 154: Summer session 2001
- ECE 154: Summer session 2000

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Winter quarter 2008 offering of ECE 154

This area is reserved for important course announcements: 2008/03/24: Course grades have just been submitted to the registrar. Grade stats for HW6 and the final exam have been posted below on this page. The course is now officially over. Have a pleasant spring break!

2008/03/11: The final exam will be held in HSSB 1174 on Saturday, 3/22/2008, 12:00-2:30 PM. The exam will be closed book, but the use of a calculator is allowed.

2008/03/03: Homework 6 (the last one for the course) has been posted below, along with grade stats for HW5 and MT2. Instructor and TA office hours will be held as usual during the final exams week. In addition, class times (MW 3:30-5:00) will be converted to instructor office hours in HFH 5155 and discussion times (F 10:00-1:00) will become TA office hours in Phelps 1435.

2008/02/22: As mentioned in class, HW5 and HW6 were merged into a single homework assignment so that the problems can be studied and solved before midterm 2. There will thus be one fewer homework than the 7 planned. The last homework, HW6, will be posted no later than W 3/5 (probably a few days earlier) and will be due on F 3/14.

2008/02/12 -- Homework 5 has been posted below, along with grade stats for HW4 and MT1. Please note that grade stats have been moved to a separate section below the homework assignments. Presentations for part 4 of the book are now up to date.

2008/02/05: Due to several time conflicts with existing office hours, an extra instructor office hour has been added on Tuesdays 5:30-6:30.

2008/01/29 -- Homework 4 has been posted below. Presentations for part 3 of the textbook (ch. 9-12) are now up to date. Our first midterm exam will be held in class on Monday 2/4. The exam will be closed book and notes; use of a calculator is permitted.

2008/01/21 -- Homework 3 has been posted below. Homework 1 stats have also been posted.

2008/01/15 -- Homework 2 has been posted below. Presentations for parts 1 and 2 of the textbook (ch. 1-8) are now up to date.

2008/01/09 -- Homework 1 has been posted below. Please remember to attach a sheet with your name and perm number to the pretest. This sheet

will be removed before grading. Its sole purpose is to verify that all enrolled students have turned in the pretest.

2008/01/06 -- The completed introductory course survey and the take-home pretest paper are due by 9:00 AM on Friday 1/11.

Course: ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Winter Quarter 2008. For enrollment codes, see "Meetings" below.

Catalog entry: **154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

Instructor: Behrooz Parhami, Room 5155 Harold Frank Hall (Engineering I), Phone 805-893-3211, E-mail parhami at ece.ucsb.edu

TAs: Peter Lisherness; Crystal Wei

Meetings: Lectures – MW 3:30-4:45, HSSB 1174
Discussion, option 1 – F 10:00-10:50, Phelps 3519 (Crystal, enrollment code 10587)
Discussion, option 2 – F 11:00-11:50, Bldg 387 Rm 104 (Crystal, enrollment code 10595)
Discussion, option 3 – F 12:00-12:50, Phelps 3519 (Peter, enrollment code 10603)

Consultation: Instructor's office hours, held in Room 5155 HFH – M 11:30-1:00, T 5:30-6:30, W 12:30-2:00
TA office hours, held in Phelps 1435 – T 1:00-2:30 (Crystal); R 10:00-1:00 (Peter)

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in 1-2 refresher-type lecture(s).

References: Required textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Click on the textbook title to see the textbook's Web page which has downloadable PowerPoint and PDF presentations, a list of errors, and other material. Publisher's list price $86.95, UCSB Bookstore price $81.95/new, $61.45/used.
Useful book (not required) – D.A. Patterson & J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 3rd ed., 2005.
Electronic Resources at UCSB
http://www.library.ucsb.edu/eresources/databases/ (electronic journals, collections, etc.)
http://www.library.ucsb.edu/subjects/engineering/ece.html (research guide in ECE)

Evaluation: Students will be evaluated based on these 3 components with the given weights:

20% -- ~~Seven~~ Six homework assignments posted on the course website by specified dates and due in a homework box in about one week. Homework descriptions appear below, after the course calendar.

40% -- Two closed-book midterm exams (see the course calendar for date, time, and coverage).

40% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. About half of the lectures have been marked as important or very important. These lectures cover key concepts that constitute the core of ECE 154.

Day/Date	Chapters	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 1/7	1-3	Course intro, review of logic circuits	Pretest	Introductory survey
W 1/9	4	Computer performance	HW1 (1-3)	Very important lecture
F 1/11	1-3	(Discussion: Logic circuits + technology)	Pretest due	Introductory survey due
M 1/14	5-6	MiniMIPS instructions and addressing		
W 1/16	6-7	MiniMIPS (cont.), assembly programs	HW2 (4)	
F 1/18	4	(Discussion: Computer performance + HW1)	HW1 due	
M 1/21		**No lecture:** Martin Luther King Jr. Holiday		
W 1/23	8	ISA variations, CISC, RISC, URISC	HW3 (5-7)	
F 1/25	5-8	(Discussion: Instruction sets + HW2)	HW2 due	
M 1/28	9	Number representation and basic adders		
W 1/30	10	Fast addition and multifunction ALUs	HW4 (8-10)	Important lecture

F 2/1	9-10	(Discussion: Number rep + addition + HW3)	HW3 due	
M 2/4	4-10	**1st midterm exam**, in our regular classroom		
W 2/6	13	Stages of instruction execution		Important lecture
F 2/8	4-10	(Discussion: 1st midterm exam + HW4)	HW4 due	
M 2/11	14	Control unit synthesis		Important lecture
W 2/13	15	Pipelined data paths	HW5 (13-16)	Important lecture
F 2/15	13-14	(Discussion: Data path and control)		
M 2/18		**No Lecture:** President's Day Holiday		
W 2/20	16	Pipeline performance limits	~~HW6 (15-16)~~	Important lecture
F 2/22	15-16	(Discussion: Pipelining + HW5)	HW5 due	
M 2/25	13-16	**2nd midterm exam**, in our regular classroom		
W 2/27	17, 19	Main and mass memory concepts		
F 2/29	17, 19	(Discussion: Memory system + HW6)	~~HW6 due~~	
M 3/3	18	Cache memory	HW6 (17-20)	Very important lecture
W 3/5	20	Virtual memory and paging	~~HW7 (17-20)~~	
F 3/7	18, 20	(Cache and virtual memory)		
M 3/10	21-22	Input/output devices and programming		
W 3/12	23-24	Buses, interfacing, and interrupts		Sample final handed out
F 3/14	21-24	(Discussion: I/O, buses, interrupts + HW7)	HW6 due	
Sat 3/22	4-24	**Final exam**, 12:00-3:00 PM, HSSB 1174		

Homework: General Requirements

Deposit solutions in ECE 154 homework box (Room 3120 HFH) before 9:00 AM on due date.
Because solutions will be handed out on the due date, no deadline extension can be granted.
Use a cover page that includes your name, course and assignment number for your solutions.
Staple the sheets and write your name on top of every sheet in case sheets are separated.
Although some cooperation is permitted, direct copying will have severe consequences.

Take-home pretest: Prerequisites and probability (due F 1/11/2008, 9:00 AM)

This pretest, handed out in class on Monday 1/7/2008, provides you and the instructor with feedback about preparations for ECE 154. You should answer each question on a separate sheet, then staple everything together, using the question sheet as a cover page. The question sheet has a box in which you should make a unique mark or drawing that would allow you to recognize and retrieve your test paper. Papers will be graded anonymously, so please answer each question to the best of your ability, without help from any source, including TAs. To ensure that you are credited with handing in the pretest, attach a separate sheet with your name and Perm number (to be removed before grading). If you missed the first class, please ask the instructor or one of the TAs for the pretest and introductory course survey. Aggregate scores will be reported below after grading.

Homework 1: Logic design and computer technology (ch. 1-3, due F 1/18/2008, 9:00 AM)

Do the following problems from the textbook: 1.4b [20 pts], 1.17a [15 pts], 2.7ab [20 pts], 2.10 [20 pts], 3.8 [25 pts]

Homework 2: Computer performance (ch. 4, due F 1/25/2008, 9:00 AM)

Do the following problems from the textbook: 4.4 [15 pts], 4.8b [20 pts], 4.14 [20 pts], 4.15 [20 pts], 4.B, given below [25 pts]

Problem 4.B: RISC vs. CISC Performance -- A computer has class-A, class-B, and class-C instructions that take 0.5 ns, 1 ns, and 2 ns to execute, respectively. With single-cycle implementation (CPI = 1), the clock cycle must be set at 2 ns, yielding a CPU performance of 500 MIPS. Suppose that the execution of a particular set of programs involves the instruction mix: x class A, y class B, and $1 - x - y$ class C. It is possible to remove all class-B (class-C) instructions from the design, but each such instruction in our programs must then be replaced with an average of 2.5 (7.5) class-A instructions. (a) Derive the MIPS rating of a multicycle implementation for the original machine as a function of x and y. Assume that instruction execution stages can be divided, with no overhead, so that the pieces fit within a clock cycle of any given width. (b) Repeat part a for the new machine which has only class-A instructions. (c) Characterize an instruction mix for which the new machine would offer greater performance than the 500-MIPS single-cycle implementation.

Homework 3: Instructions and assembly language (ch. 5-7, due F 2/1/2008, 9:00 AM)

Do the following problems from the textbook: 5.10cd [15 pts], 5.15 [25 pts], 5.16b [15 pts], 6.1ab [10 pts], 6.3 [20 pts], 7.3abc [15 pts]

Homework 4: ISA variations and computer arithmetic (ch. 8-10, due F 2/8/2008, 9:00 AM)

Do the following problems from the textbook: 8.9 [20 pts], 9.1de [10 pts], 9.16abc [15 pts], 10.2 [20 pts], 10.6 [15 pts], 10.14a [20 pts]

Homework 5: Data path design and control unit (ch. 13-~~14~~ 16, due F 2/22/2008, 9:00 AM)

Do the following problems from the textbook: 13.2c [10 pts], 13.11 [15 pts], 14.8 [20 pts], 15.1 [25 pts], 16.2 [15 pts], 16.11a [15 pts]

Homework 6: Memory system design (ch. 17-20, due F 3/14/2008, 9:00 AM)

The originally planned HW6, intended to cover chapters 15-16, was merged into HW5 to allow solutions to be provided and discussed before Midterm 2. The following (last homework assignment for the course) was HW7 in the syllabus distributed at the start of the winter term.

Do the following problems from the textbook: 17.5 [15 pts], 18.5bd [20 pts], 18.11 [20 pts], 19.4 [20 pts], 20.1b [10 pts], 20.12a [15 pts]

Suggested problems (ch. 21-24, for practice only, not to be turned in)

Do the following problems from the textbook: 21.8, 21.9 [Correction: Example 21.2 is intended], 22.1, 22.5, 22.9, 23.4, 24.2, 24.11

Grade stats

Pretest Grades -- Prob. 1: Range = [0, 100], Median = 50, Mean = 45, SD = 31; Prob. 2: Range = [0, 100], Median = 50, Mean = 52, SD = 24; Prob. 3: Range = [0, 100], Median = 50, Mean = 60, SD = 28; Prob. 4: Range = [0, 100], Median = 50, Mean = 44, SD = 29.

HW1 Grades: Range = [35, 99], Median = 85, Mean = 81, SD = 14

HW2 Grades: Range = [57, 100], Median = 77, Mean = 81, SD = 12

HW3 Grades: Range = [42, 93], Median = 85, Mean = 82, SD = 10

HW4 Grades: Range = [12, 100], Median = 75, Mean = 71, SD = 20

HW5 Grades: Range = [25, 100], Median = 83, Mean = 79, SD = 16

HW6 Grades: Range = [52, 93], Median = 75, Mean = 75, SD = 11

MT1 Grades: Range = [29, 87], Median = 60, Mean = 59, SD = 14

MT2 Grades: Range = [52, 98], Median = 78, Mean = 77, SD = 11

Final Exam Grades: Range = [27, 93], Median = 67, Mean = 66, SD = 13

Sample Midterm Exam

The following is meant to indicate the types and levels of problems in the midterm, rather than the coverage (which is outlined in the lecture schedule and below). This particular exam covered up to the end of Chapter 12 of the textbook and was 105 minutes long (our two midterms will be 75 minutes each). Table 6.2 of the text was appended to the end of the exam for reference in solving Problem 3.

Problem 1 [15 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inch per term) [3 points each]: Decoder; PC-relative addressing; Pseudoinstruction; Assembler directive; Directed rounding.

Problem 2 [25 points]. Amdahl's law -- Problem 4.16 in the text [part a, 15 points; part b, 10 points]

Problem 3 [20 points] Machine instructions -- Problem 7.3 in the text, parts d and g [10 points each]

Problem 4 [20 points] Multifunction ALU -- Consider the following multifunction ALU studied in class. Specify the control signal values that are needed for executing the following two instructions. [10 points each] [Fig. 10.19 of the text goes here] (a) `sll`. (b) `slt`.

Problem 5 [20 points] Shift-add binary hardware multiplier -- In the following diagram of a radix-2 hardware multiplier, explain: [Fig. 11.4 of the text goes here] (a) [6 points] Why the register holding the multiplier y can be merged with the one holding the doublewidth partial product $z^{(j)}$. (b) [6 points] The role of the multiplexer. (c) [8 points] How separate cycles or phases for loading the doublewidth partial product register and shifting it to the right can be avoided.

Sample Final Exam

The following is meant to indicate the types and levels of problems in the final, rather than the coverage (which is outlined in the lecture schedule and below). This particular exam covered up to the end of Chapter 24 of the textbook and was 150 minutes long. The single midterm had included up to the end of Chapter 12 in the textbook.

Problem 1 [16 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1 inch per term) [2 points each]: Bus arbitration; Conflict miss; Delayed branch; Interrupt handler; Pseudoinstruction; Set-associative cache; TLB.

Problem 2 [15 points] Computer arithmetic -- Problem 11.10a in the text.

Problem 3 [12 points] Processor data path -- Problem 13.2b in the text.

Problem 4 [16 points] Control unit design -- The following diagram shows a microprogrammed implementation of control unit functions [Fig. 14.7 of the text goes here]. (a) Does this diagram represent a single-cycle or multicycle implementation? Why? (b) What are the roles of the dispatch ROMs? (c) How are the values of the "Sequence control" signals, that control the 4-input mux, decided? (d) Name and describe two of the control signals that go from the microinstruction register to the data path section (choose any two and describe their functions briefly).

Problem 5 [15 points] Pipelining -- In the following diagram, a pipelined data path for MicroMIPS and some of its controls are shown [Fig. 15.10 of the text goes here]. Explain the roles of: (a) The control signals that are stored in the bottom part of the pipeline registers. (b) The multiplexer that appears below the SE circle, next to the register file. (c) The multiplexer located above the program counter.

Problem 6 [16 points] Memory hierarchy -- Example 20.3 in the text.

Problem 7 [10 points] Input/Output -- Example 22.5 in the text.

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exams (Chapters 4-10 for midterm 1, Chapters 13-16 for midterm 2) and final exam (Chapters 4-24). All sections not specifically excluded are required, even if they are not covered in class.

Chapters 1-3 -- No direct problem or question, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, and 8.4.

Chapters 9-10 -- Computer arithmetic: problem likely on 2's-complement numbers, number radix conversion, floating-point number formats, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs.

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

The following apply to the final exam, which will include material from the preceding chapters as well, but to a lesser degree.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, and 19.6 are excluded.

Chapters 21-24 -- Input/output and interfacing: problem possible on memory-mapped, polled, or interrupt-driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Winter quarter 2007 offering of ECE 154

This area is reserved for important course announcements: 2007/03/26: Course grades have been submitted to the Registrar. Final exam grades: Range [34, 84], Mean 60, Median 59, SD 11. Have a great spring break!

2007/03/07: A sample final exam and suggested problems from Chapter 21-24 have been added to this page. The instructor and TAs will maintain their normal office hours during the finals week (3/19-23). In addition, the following office hours have been added for Friday, 3/23 -- 11:00-12:00 (JK, ECI Lab), 2:00-3:00 (SC, ECI Lab), 5:00-6:00 (BP, 5155 HFH).

2007/03/03: Exam grades: [Min, Max], Mean, Median, SD -- MT1: [49, 89], 68, 68, 10 -- MT2: [61, 99], 85, 87, 10. The seventh homework assignment has been posted below a few days ahead of schedule to give you more time for working on it, given the rush of end-of-quarter assignments, projects, and exams.

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Winter Quarter 2007, Enrollment Code 11486 (for codes pertaining to discussion sessions, see "Meetings" below)
Catalog entry:	**154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and

assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

Instructor: Behrooz Parhami, Room 5155 Harold Frank Hall (Engineering I), Phone 805-893-3211, <Instructor's e-mail>

TAs: Justin Kane; H.-M. Sherman Chang

Meetings: Lectures – MW 3:30-4:45, North Hall 1006
Discussion, option 1 – F 1:00-1:50, Phelps 1508 (Chang, enrollment code 11494)
Discussion, option 2 – F 11:00-11:50, Girvetz 1112 (Kane, enrollment code 11502)
Discussion, option 3 – F 12:00-12:50, Phelps 3519 (Kane, enrollment code 11510)
Discussion, option 4 – F 2:00-2:50, Bldg 387 Room 103 (Chang, enrollment code 11528)

Consultation: Instructor's office hours, held in Room 5155 HFH – M 11:30-1:00, W 12:30-2:00
TA office hours, held in the ECI Lab, Room 1140 HFH – T 5-6 PM (Chang); R 12-2 PM (Kane) and 5-6 PM (Chang)

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in 1-2 refresher-type lecture(s).

References: Required textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Click on the link above to see the textbook's Web page which has downloadable PowerPoint presentations, a list of errors, and other material. Publisher's list price $82, UCSB Bookstore price $82.
Useful book – D.A. Patterson & J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 3rd ed., 2005.
Electronic Resources at UCSB
http://www.library.ucsb.edu/eresources/databases/ (electronic journals, collections, etc.)
http://www.library.ucsb.edu/subjects/engineering/ece.html (research guide in ECE)

Evaluation: Students will be evaluated based on these 3 components with the given weights:

20% -- Seven homework assignments posted on the course website by specified dates and due in a homework box in about one week. Homework descriptions appear below, after the course calendar.

40% -- Two closed-book midterm exams (see the course calendar for date, time, and coverage).

40% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. About half of the lectures have been marked as important or very important. These lectures cover key concepts that constitute the core of ECE 154.

Day/Date	Chapters	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 1/8	1-3	Course intro, review of logic circuits		
W 1/10	4	Computer performance	HW1 (1-3)	Very important lecture
F 1/12	1-3	(Discussion: Logic circuits + technology)		
M 1/15		**No lecture:** Martin Luther King, Jr., Holiday		
W 1/17	5-6	MiniMIPS instructions and addressing	HW2 (4)	
F 1/19	4	(Discussion: Computer performance + HW1)	HW1 due	
M 1/22	6-7	MiniMIPS (cont.), assembly programs		
W 1/24	8	ISA variations, CISC, RISC, URISC	HW3 (5-7)	
F 1/26	5-8	(Discussion: Instruction sets + HW2)	HW2 due	
M 1/29	9	Number representation and basic adders		
W 1/31	10	Fast addition and multifunction ALUs	HW4 (8-10)	Important lecture
F 2/2	9-10	(Discussion: Number rep + addition + HW3)	HW3 due	
M 2/5	4-10	**1st midterm exam**, in our regular classroom		
W 2/7	13	Stages of instruction execution		Important lecture
F 2/9	4-10	(Discussion: 1st midterm exam + HW4)	HW4 due	
M 2/12	14	Control unit synthesis		Important lecture
W 2/14	15	Pipelined data paths	HW5 (13-14)	Important lecture

F 2/16	13-14	(Discussion: Data path and control)		
M 2/19		**No Lecture:** President's Day Holiday		
W 2/21	16	Pipeline performance limits	HW6 (15-16)	Important lecture
F 2/23	15-16	(Discussion: Pipelining + HW5)	HW5 due	
M 2/26	13-16	**2nd midterm exam**, in our regular classroom		
W 2/28	17, 19	Main and mass memory concepts		
F 3/2	17, 19	(Discussion: Memory system + HW6)	HW6 due	
M 3/5	18	Cache memory		Very important lecture
W 3/7	20	Virtual memory and paging	HW7 (17-20)	
F 3/9	18, 20	(Cache and virtual memory)		
M 3/12	21-22	Input/output devices and programming		
W 3/14	23-24	Buses, interfacing, and interrupts		Sample final handed out
F 3/16	21-24	(Discussion: I/O, buses, interrupts + HW7)	HW7 due	
Sat 3/24	4-24	**Final exam**, 12:00-3:00 PM, NH 1006		

Homework: General Requirements

Deposit solutions in ECE 154 homework box (Room 3120 HFH) before 10 AM on due date.
Late homework will not be accepted, so plan to start work on your assignments early.
Use a cover page that includes your name, course and assignment number for your solutions.
Staple the sheets and write your name on top of every sheet in case sheets are separated.
Although some cooperation is permitted, direct copying will have severe consequences.

Homework 1: Logic design and computer technology (ch. 1-3, due F 1/19/2007, 10:00 AM)

Do the following problems from the textbook (20 points each): 1.7, 1.9d, 2.4a, 2.8a, 3.16

Grades: Range = [65, 100], Mean = 81, Median = 85, SD = 12

Homework 2: Computer performance (ch. 4, due F 1/26/2007, 10:00 AM)

Do the following problems from the textbook: 4.6 (20 pts.), 4.7 (20 pts.), 4.9 (25 pts.), 4.17 (10 pts.), 4.20 (25 pts.)

Grades: Range = [40, 100], Mean = 78, Median = 83, SD = 16

Homework 3: Instructions and assembly language (ch. 5-7, due F 2/2/2007, 10:00 AM)

Do the following problems from the textbook: 5.7 (10 pts.), 5.8 (10 pts.), 5.17 (25 pts.), 6.12 (20 pts.), 6.13 (25 pts.), 7.4c (10 pts.)

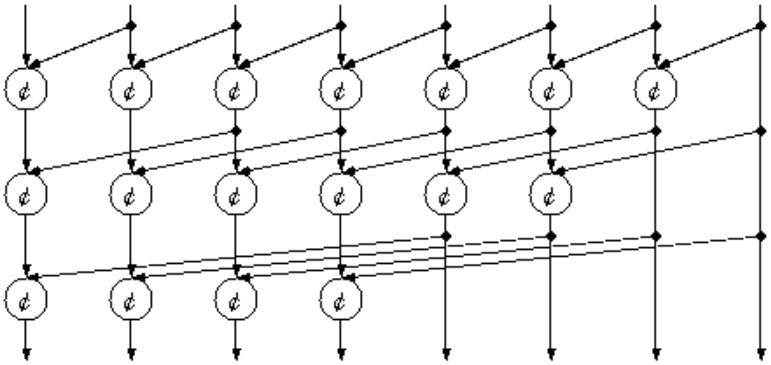
Grades: Range = [70, 100], Mean = 92, Median = 95, SD = 9

Homework 4: ISA variations and computer arithmetic (ch. 8-10, due F 2/9/2007, 10:00 AM)

Do the following problems from the textbook, plus problem 10.A (15 pts.), defined below: 8.9 (20 pts.), 8.10 (20 pts.), 9.9c (10 pts.), 9.16abc (15 pts.), 10.21 (20 pts.)

Grades: Range = [70, 100], Mean = 92, Median = 95, SD = 9

Problem 10.A -- Alternative carry networks: Consider the following Kogge-Stone carry network for an 8-bit adder. By labeling its lines in a manner similar to Fig. 10.11, verify that the network does indeed produce the required carries. Then, compare the new network with the Brent-Kung network of Fig. 10.11 with respect to cost/complexity (carry-operator count) and latency (carry-operator levels). *Challenge question (optional):* Can you write general formulas for the complexity and latency of the new network with k inputs, assuming that k is a power of 2?



Homework 5: Data path design and control unit (ch. 13-14, due F 2/23/2007, 10:00 AM)

Do the following problems from the textbook: 13.3 (25 pts.), 13.7 (25 pts.), 13.12 (20 pts.), 14.5 (10 pts.), 14.7 (20 pts.)

Grades: Range = [55, 100], Mean = 96, Median = 99, SD = 9

Homework 6: Pipelining and its limits (ch. 15-16, due F 3/2/2007, 10:00 AM)

Do the following problems from the textbook: 15.6e (20 pts.), 15.14b (10 pts.), 15.16 (15 pts.), 16.1 (15 pts.), 16.4 (20 pts.), 16.10ab (20 pts.)

Grades: Range = [60, 100], Mean = 94, Median = 97, SD = 8

Homework 7: Memory system design (ch. 17-20, due F 3/16/2007, 10:00 AM)

Do the following problems from the textbook: 17.3 (20 pts.), 18.4 (15 pts.), 18.5ac (20 pts.), 19.7d (15 pts.), 20.1a (10 pts), 20.4 (20 pts)

Grades: Range = [70, 100], Mean = 88, Median = 90, SD = 7

Suggested problems (ch. 21-24, for practice only, not to be turned in)

Do the following problems from the textbook: 21.8, 21.9 [Correction: Example 21.2 is intended], 22.1, 22.5, 22.9, 23.4, 24.2, 24.11

Sample Midterm Exam

The following is meant to indicate the types and levels of problems in the midterm, rather than the coverage (which is outlined in the lecture schedule and below). This particular exam covered up to the end of Chapter 12 of the textbook and was 105 minutes long (our two midterms will be 85 minutes each). Table 6.2 of the text was appended to the end of the exam for reference in solving Problem 3.

Problem 1 [15 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inch per term) [3 points each]: Decoder; PC-relative addressing; Pseudoinstruction; Assembler directive; Directed rounding.

Problem 2 [25 points]. Amdahl's law -- Problem 4.16 in the text [part a, 15 points; part b, 10 points]

Problem 3 [20 points] Machine instructions -- Problem 7.3 in the text, parts d and g [10 points each]

Problem 4 [20 points] Multifunction ALU -- Consider the following multifunction ALU studied in class. Specify the control signal values that are needed for executing the following two instructions. [10 points each] [Fig. 10.19 of the text goes here] (a) `sll`. (b) `slt`.

Problem 5 [20 points] Shift-add binary hardware multiplier -- In the following diagram of a radix-2 hardware multiplier, explain: [Fig. 11.4 of the text goes here] (a) [6 points] Why the register holding the multiplier y can be merged with the one holding the doublewidth partial product $z^{(j)}$. (b) [6 points] The role of the multiplexer. (c) [8 points] How separate cycles or phases for loading the doublewidth partial product register and shifting it to the right can be avoided.

Sample Final Exam

The following is meant to indicate the types and levels of problems in the final, rather than the coverage (which is outlined in the lecture schedule and below). This particular exam covered up to the end of Chapter 24 of the textbook and was 150 minutes long. The single midterm had included up to the end of Chapter 12 in the textbook.

Problem 1 [16 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1 inch per term) [2 points each]: Bus arbitration; Conflict miss; Delayed branch; Interrupt handler; Pseudoinstruction; Set-associative cache; TLB.

Problem 2 [15 points] Computer arithmetic -- Problem 11.10a in the text.

Problem 3 [12 points] Processor data path -- Problem 13.2b in the text.

Problem 4 [16 points] Control unit design -- The following diagram shows a microprogrammed implementation of control unit functions [Fig. 14.7 of the text goes here]. (a) Does this diagram represent a single-cycle or multicycle implementation? Why? (b) What are the roles of the dispatch ROMs? (c) How are the values of the "Sequence control" signals, that control the 4-input mux, decided? (d) Name and describe two of the control signals that go from the microinstruction register to the data path section (choose any two and describe their functions briefly).

Problem 5 [15 points] Pipelining -- In the following diagram, a pipelined data path for MicroMIPS and some of its controls are shown [Fig. 15.10 of the text goes here]. Explain the roles of: (a) The control signals that are stored in the bottom part of the pipeline registers. (b) The multiplexer that appears below the SE circle, next to the register file. (c) The multiplexer located above the program counter.

Problem 6 [16 points] Memory hierarchy -- Example 20.3 in the text.

Problem 7 [10 points] Input/Output -- Example 22.5 in the text.

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exams (Chapters 4-10 for midterm 1, Chapters 13-16 for midterm 2) and final exam (Chapters 4-24). All sections not specifically excluded are required, even if they are not covered in class.

Chapters 1-3 -- No direct problem or question, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, and 8.4.

Chapters 9-10 -- Computer arithmetic: problem likely on 2's-complement numbers, number radix conversion, floating-point number formats, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs.

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

The following apply to the final exam, which will include material from the preceding chapters as well, but to a lesser degree.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, and 19.6 are excluded.

Chapters 21-24 -- Input/output and interfacing: problem possible on memory-mapped, polled, or interrupt-driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Winter quarter 2006 offering of ECE 154

This area is reserved for important course announcements: 2006/3/14: During the finals weeks (3/20-24), the following extended office hours will apply -- M 11:00-12:30 (BP), T 1:00-2:30 (BP), W 12:30-2:00 (BB), R 9:00-10:30 (BP) and 2:30-4:00 (HF), F 9:00-10:30 (BP). In addition, a review session will be held by B. Benson on M 3/20, 9:00-11:00 AM in Phelps 3523.

2006/3/3: New versions of the presentations for Parts I to IV of the textbook have been posted to the book's Web page.

2006/2/28: Homework 5 has been posted below. It will be due by 10:00 AM on Friday 3/10.

2006/2/22: Homework 4 has been posted below. It will be due by 10:00 AM on Friday 3/3.

2006/2/9: Information about exclusions from the midterm exam has been updated.

2006/1/31: Homework 3 has been posted below. It will be due by 10:00 AM on Friday 2/10. Also some new corrections, including several for pages 151-153, have been posted to the textbook's Web page.

2006/1/17: Homework 2 has been posted below. It will be due by 10:00 AM on Friday 1/27.

2006/1/10: Homework 1 has been posted below. It has two parts that must be submitted separately. Both parts will be due by 10:00 AM on Friday 1/20 in the ECE 154 homework box located on the fifth floor of Engineering I.

Course: ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Winter Quarter 2006, Enrollment Code 11577 (for discussion session codes, see "Meetings" below)

Catalog entry: **154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

Instructor: Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>

TAs: Bridget Benson, Hamed Farshbaf Dadgour

Meetings: Lectures – MW 3:30-4:45, North Hall 1006
Discussion, option 1 – F 1:00-1:50, Phelps 1508 (Farhsbaf, enrollment code 11585)
Discussion, option 2 – F 11:00-11:50, North Hall 1111 (Benson, enrollment code 11593)
Discussion, option 3 – F 12:00-12:50, Phelps 3519 (Farshbaf, enrollment code 11601)
Discussion, option 4 – F 2:00-2:50, Bldg 387 Room 104 (Benson, enrollment code 11619)

Consultation: Instructor's office hours, held in Room 5155 Eng. I – M 11:00-12:30, T 1:00-2:30
TA office hours, held in Phelps 1435 – W 12:30-2:00, Benson; R 2:30-4:00, Farshbaf

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in 1-2 refresher-type lecture(s).

References: Textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Click on the link above to see the textbook's Web page which has downloadable PowerPoint presentations, a list of errors, and other material. Publisher's list price $75, UCSB Bookstore price $75.
Recommended book – D.A. Patterson & J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 3rd ed., 2005.
Electronic Resources at UCSB
http://www.library.ucsb.edu/eresources/databases/ (electronic journals, collections, etc.)
http://www.library.ucsb.edu/subjects/engineering/ece.html (research guide in ECE)

Evaluation: Students will be evaluated based on these 3 components with the given weights:

20% -- Five homework assignments posted on the course Web page by specified dates and due in a homework box in about one week. Homework descriptions appear below, after the course calendar.

30% -- Closed-book midterm exam (see the course calendar for date, time, and coverage).

50% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed.

Day/Date	Chapters	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 1/9	1-2	Introduction + review of digital circuits		
W 1/11	3-4	Computer technology and performance	HW1 (1-4)	Very important lecture
F 1/13	1-3	(Discussion: Logic circuits + technology)		
M 1/16		**No lecture:** Martin Luther King, Jr., Holiday		
W 1/18	5	Instructions and addressing	HW2 (5-8)	
F 1/20	4	(Discussion: Performance + HW1)	HW1 due	
M 1/23	6	Procedures and data		
W 1/25	7-8	Assembly programs and ISA variations		
F 1/27	5-8	(Discussion: Instruction sets + HW2)	HW2 due	
M 1/30	9	Number representation and adders		
W 2/1	10	Addition and multifunction ALUs	HW3 (9-12)	Important lecture

F 2/3	9-10	(Discussion: Number rep + addition)		
M 2/6	11	Multiplication and division		
W 2/8	12	Floating-point arithmetic		Sample midterm handed out
F 2/10	11-12	(Discussion: Computer arithmetic + HW3)	HW3 due	
M 2/13	13	Stages of instruction execution		
W 2/15	1-12	**Midterm exam**, 3:30-4:55, NH 1006		Note the extended time
F 2/17		(Discussion: Midterm exam)		
M 2/20	12	**No Lecture:** President's Day Holiday		
W 2/22	14	Control unit synthesis	HW4 (13-15)	Important lecture
F 2/24	13-14	(Discussion: Data path and control unit)		
M 2/27	15	Pipelined data paths		Important lecture
W 3/1	16	Pipeline performance limits	HW5 (17-20)	Important lecture
F 3/3	15-16	(Discussion: Pipelining + HW4)	HW4 due	
M 3/6	17-18	Main and cache memory concepts		Very important lecture
W 3/8	19-20	Mass and virtual memory concepts		
F 3/10	17-20	(Discussion: Memory system + HW5)	HW5 due	
M 3/13	21-22	Input/output devices and programming		
W 3/15	23-24	Buses, interfacing, and interrupts		Sample final handed out
F 3/17	21-24	(Discussion: Input/Output)		
F 3/24	1-24	**Final exam**, 12:00-3:00 PM, NH 1006		

Homework: General Requirements

Deposit solutions in ECE 154 homework box (5th floor of Engr I) before 10 AM on due date.
Late homework will not be accepted, so plan to start work on your assignments early.
Use a cover page that includes your name, course and assignment number for your solutions.
Staple the sheets and write your name on top of every sheet in case sheets are separated.
Although some cooperation is permitted, direct copying will have severe consequences.

Homework 1: Logic design and computer performance (due F 1/20/2006, 10:00 AM)

Please staple and submit your solutions for the two parts separately.

Part A -- Do the following problems from the textbook: 1.1ab [10 pts.], 1.11 [15 pts.], 2.5b [20 pts.], 2.9 [15 pts.]

Part B -- Do the following problems from the textbook: 4.5 [20 pts.], 4.10 [20 pts.]

Homework 2: Instructions and assembly language (due F 1/27/2006, 10:00 AM)

Do the following problems from the textbook: 5.11 [15 pts.], 5.16a [15 pts.], 6.4 [20 pts.], 7.2fghi [20 pts.], 7.3h [10 pts.], 8.13 [20 pts]

Homework 3: Computer arithmetic (due F 2/10/2006, 10:00 AM)

Do the following problems from the textbook: 9.1abc [15 pts.], 9.15 [10 pts.], 10.5a [10 pts.], 10.9 [20 pts.], 11.1a [5 pts.], 11.4d [20 pts], 12.8abd [20 pts.]

Homework 4: Data path and control (due F 3/3/2006, 10:00 AM)

Do the following problems from the textbook: 13.1a [15 pts.], 13.17 [20 pts.], 14.2c [15 pts.], 14.6 [15 pts.], 15.6a [20 pts.], 15.14a [15 pts.]

Homework 5: Memory system design (due F 3/10/2006, 10:00 AM)

Do the following problems from the textbook: 17.15 [10 pts.], 18.4bc [20 pts], 18.10 [20 pts.], 19.7b [10 pts.], 20.3 [20 pts.], 20.12b [20 pts.]

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exam (Chapters 1-12) and final exam (Chapters 1-24). All sections not specifically excluded are required, even if they were not covered in class.

Chapters 1-2 -- Logic design: no direct problem, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.

Chapter 3 -- No problem or question.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, 8.4, and 8.6.

Chapters 9-12 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs, shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic. Ignore pp. 205-206 in Section 11.3, pp. 214-215 in Section 11.6, and pp. 235-236 in Section 12.6.

The following apply to the final exam, which will include material from the preceding chapters as well, but to a much lesser degree (new material will be heavily emphasized).

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, 19.6, and 20.5 are excluded.

Chapters 21-24 -- Input/output and interfacing: problem possible on memory-mapped, polled, or interrupt-driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Summer session 2005 offering of ECE 154

This area is reserved for important course announcements: 2005/07/25: The instructor will have special office hours on the eve of the final exam for last-minute questions (i.e., on Thursday, 7/28, 5:00-7:30 PM).

2005/07/18: Homework 5 has been posted below; its due date is extended to Tuesday 7/26. There is a change in the coverage of the final exam; specifically, microprogramming (Section 14.5) is now excluded.

2005/07/13: Midterm exam (min, avg, max) grades were (56, 71, 83). The corresponding stats for HW2 and HW3 were (0, 80, 100) and (0, 63, 98), respectively. The latter become (74, 89, 100) and (50, 79, 98) if grades of 0 for homework not turned in are excluded.

2005/07/11: Homework 4 has been posted below. It will be due on Monday 7/18 during the discussion session. Note that during the rest of this week (including on Friday, 7/15), we will have lectures covering the important Chapters 13-16 of the text.

2005/7/3: Homework 3 has been posted below. It will be due on Friday 7/8; in preparation for the midterm exam on Monday, 7/11 (beginning at 7:45 AM), solutions will be distributed during the discussion session on the due date.

005/06/27: Homework 2 has been posted below. Please note critical and noncritical corrections listed for page 110 of the textbook on its Web page.

2005/06/23: Homework 1 has been withdrawn and will not be graded, because some students may have gained unauthorized access to the solutions sheet. Its weight will be redistributed among the remaining four homework assignments. You can use Homework 1 for practice, comparing your solutions against those to be handed out next Monday. Homework 2 will be posted next week and will be due on its regular due date. The previous form of Homework 2, along with its solutions, was compromised as well; so a new version of this homework is being designed.

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2005 (Session A, June 20 to July 29), Enrollment Code 02923
Catalog entry:	**154. Introduction to Computer Architecture.** **(4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.
Instructor:	Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>

TA: Shahnam Mirzaei

Meetings: Lectures and discussions – MTWR (plus some Fridays) 8:00-9:20, Phelps 1437

Consultation: Instructor's office hours, held in Room 5155 Eng. I – M 9:30-11:00, W 12:30-2:00
TA's office hours, held in Phelps 1435 – T 1:00-2:00, R 11:00-12:00, F 10:00-11:00

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in 1-2 refresher-type lecture(s).

References: Textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Click on the link above to see the textbook's Web page which has downloadable PowerPoint presentations, a list of errors, and other material. Publisher's list price $75, UCSB Bookstore price $75.
Recommended book – D.A. Patterson & J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 3rd ed., 2005.
Electronic Resources at UCSB
http://www.library.ucsb.edu/eresources/databases/ (electronic journals, collections, etc.)
http://www.library.ucsb.edu/subjects/engineering/ece.html (research guide in ECE)

Evaluation: Students will be evaluated based on these 3 components with the given weights:

20% -- Five homework assignments posted on the course Web page by specified dates and due in class in about one week. Homework descriptions appear below, after the course calendar.

30% -- Closed-book midterm exam (see the course calendar for date, time, and coverage).

50% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed.

Day/Date	Chap's	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 6/20	1	Overview + combinational circuits		
T 6/21	2-3	Sequential circuits + computer technology	HW1 (1-4)	
W 6/22	4	Computer performance		Very important lecture
R 6/23	5	Instructions and addressing		Make-up for W 6/29
F 6/24	1-4	(Discussion: Logic design + performance)		
M 6/27	6	Procedures and data	HW1 due	Will not be graded
T 6/28	7-8	Assembly programs and ISA variations	HW2 (5-8)	
W 6/29		**No lecture:** Instructor at a conference		Make-up on R 6/23
R 6/30	5-8	(Discussion: Instruction sets + HW1)		
M 7/4		**No Lecture:** Independence Day Holiday	HW3 (9-12)	Make-up on F 7/8
T 7/5	9-10	Number representation and adders	HW2 due	Important lecture
W 7/6	10-11	ALUs, multiplication, and division		Important lecture
R 7/7	12	Floating-point arithmetic		
F 7/8	9-12	(Discussion: Arithmetic + HW2)	HW3 due	Make up for M 7/4
M 7/11	1-12	**Midterm exam**, 7:45-9:15, Phelps 1437		Note the extended time
T 7/12	13	Stages of instruction execution	HW4 (13-15)	
W 7/13	14	Control unit synthesis		Important lecture
R 7/14	15	Pipelined data paths		Very important lecture
F 7/15	16	Pipeline performance limits		Make up for M 7/11
M 7/18	13-16	(Discussion: Data path & control + HW3)	HW4 due	
T 7/19	17-18	Main and cache memory concepts	HW5 (17-20)	Important lecture

W 7/20	19-20	Mass and virtual memory concepts		
R 7/21	17-20	(Discussion: Memory system + HW4)		
M 7/25	21-22	Input/output devices and programming	HW5 due	
T 7/26	23-24	Buses, interfacing, and interrupts		
W 7/27	25-28	Overview of high-performance computers		Not covered in final
R 7/28	21-24	(Discussion: I/O & interrupts + HW5)		
F 7/29	1-22	**Final exam**, 7:00-9:15 AM, Phelps 1437		Note the extended time

Homework 1: Logic design and computer performance (due Monday, June 27)

Do the following problems from the textbook: 1.9b [15 pts.], 1.16 [20 pts.], 2.5a [15 pts.], 3.15 [10 pts.], 4.2 [25 pts.], 4.15 [15 pts.]

Homework 2: Instructions and assembly language (due Tuesday, July 5)

Do the following problems from the textbook: 5.4 [15 pts.], 5.9bd [20 pts.], 6.9ab [20 pts.], 7.3def [15 pts.], 8.3 [15 pts.], 8.8 [15 pts.]

Homework 3: Computer arithmetic (due Friday, July 8)

Do the following problems from the textbook: 9.3 [20 pts.], 10.5bc [15 pts.], 10.11 [15 pts.], 11.4b [20 pts.], 11.12 [15 pts.], 12.5 [15 pts.]

Homework 4: Data path and control (originally due on Monday, July 18)

Do the following problems from the textbook: 13.6 [15 pts.], 14.2b [15 pts.], 14.7 [20 pts.], 15.8 [20 pts.], 16.3 [15 pts.], 16.10ab [15 pts.]

Homework 5: Memory system design (due Monday, July 25; extended to Tuesday, July 26)

Do the following problems from the textbook: 17.1ab [15 pts.], 18.3 [15 pts.], 18.8 [20 pts.], 19.1 [15 pts.], 20.7 [15 pts.], 20.12a [20 pts.]

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exam (Chapters 1-12) and final exam (Chapters 1-24). All sections not specifically excluded are required, even if they were not covered in class.

Chapters 1-2 -- Logic design: no direct problem, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.

Chapter 3 -- No problem or question.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, 8.4, and 8.6.

Chapters 9-12 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs, shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic. Ignore pp. 205-206 in Section 11.3, pp. 214-215 in Section 11.6, and pp. 235-236 in Section 12.6.

The following apply to the final exam, which will include material from the preceding chapters as well, but to a much lesser degree (new material will be heavily emphasized).

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, 19.6, and 20.5 are excluded.

Chapters 21-24 -- Input/output and interfacing: problem possible on memory-mapped, polled, or interrupt-driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Summer session 2004 offering of ECE 154

Course: ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2004 (June 21 to July 30), Enrollment Code 02964

Catalog entry: **154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

Instructor: Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>

TA: Mary Li

Meetings: Lectures and discussions – MTWR 8:00-9:20, Phelps 1437 (plus Fridays 6/25, 7/9, and 7/30)

Consultation: Instructor's office hours, held in Room 5155 Eng. I – M 11:00-12:30, W 12:30-2:00 (except 6/23)
TA's office hours, held in Phelps 1435 – T 9:30-10:30 R 9:30-10:30, F 11:00-12:00

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's viewpoint of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in one refresher-type lecture.

References: Textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Prepublication draft will be available for purchase at the UCSB Bookstore (cost is estimated to be around $35.00). Click on the link above to see the textbook's Web page.
Recommended book – D.A. Patterson & J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface,* Morgan Kaufmann, 2nd ed., 1998.

Evaluation: Students will be evaluated based on these 3 components with the given weights:

20% -- Five homework assignments posted on the course Web page by specified dates and due in class in about one week. Homework descriptions appear below, after the course calendar.

30% -- Closed-book midterm exam (see the course calendar for date, time, and coverage).

50% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed.

Day/Date	Chap's	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 6/21	1-2	Review of digital logic circuits		
T 6/22	1-2	(Discussion: Logic design)	HW1 (1-4)	No office hour tomorrow
W 6/23	3	**No lecture:** instructor away (read Ch. 3)		Make up on Friday 6/25
R 6/24	4	Computer performance + discussion		Very important lecture
F 6/25	5	Instructions and addressing	HW2 (5-8)	Make up session for 6/23
M 6/28	6-7	Procedures, data, and programs	HW1 due	
T 6/29	7-8	Assembly programs & ISA variations		
W 6/30	9	Number representation formats	HW3 (9-12)	
R 7/1	5-8	(Discussion: Instruction sets + HW1)	HW2 due	
M 7/5		**No Lecture:** Independence Day Holiday		Make up on Friday 7/9
T 7/6	10	Adders and multifunction ALUs		Important lecture

W 7/7	11	Multipliers and dividers		
R 7/8	12	Floating-point arithmetic		
F 7/9	9-12	(Discussion: Arithmetic + HW2)	HW3 due	Make up session for 7/5
M 7/12	1-12	Midterm exam, 8:00-9:20 AM		In our regular classroom
T 7/13	13	Stages of instruction execution	HW4 (13-15)	
W 7/14	14	Control unit synthesis		Important lecture
R 7/15	13-14	(Discussion: Control unit + HW3)		
M 7/19	15	Pipelined data paths		Very important lecture
T 7/20	16	Pipeline performance limits	HW4 due	
W 7/21	17-18	Main and cache memory concepts	HW5 (17-20)	Important lecture
R 7/22	15-16	(Discussion: Pipelining + HW4)		
M 7/26	19-20	Mass and virtual memory concepts		
T 7/27	21-22	Input/output devices and programming		
W 7/28	23-25	Interrupts and high-performance systems	HW5 due	Not covered in final
R 7/29	17-22	(Discussion: Memory & I/O + HW5)		
F 7/30	1-22	Final exam, 7:00-9:20 AM		Note the extended time

Homework 1: Logic design and computer performance (due Monday, June 28)

Do the following problems from the textbook: 1.9 (parts a and c), 2.19, 3.14b, 4.1, 4.12

Homework 2: Instructions and assembly language (due Thursday, July 1)

Do the following problems from the textbook: 5.2 (parts c and d), 5.9 (parts a and c), 6.5 (parts c and d), 6.7, 7.4 (parts a and b)

Homework 3: Computer arithmetic (due Friday, July 9)

Do the following problems from the textbook: 9.5, 9.14, 10.6, 11.1 (part a), 11.2 (part b), 12.6 (parts d and e)

Homework 4: Data path and control (due Tuesday, July 20)

Do the following problems from the textbook: 13.8, 13.13, 14.9, 15.5, 15.10

Homework 5: Memory system design (due Wednesday, July 28)

Do the following problems from the textbook: 17.2, 18.2, 18.9, 19.5, 20.6 (part b), 20.8

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exam (Chapters 1-12) and final exam (Chapters 1-22). All sections not specifically excluded are required, even if they were not covered in class.

Chapters 1-2 -- Logic design: no direct problem, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.

Chapter 3 -- No problem or question.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, 8.4, and 8.6.

Chapters 9-12 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs, shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic. Ignore pp. 264-265 in Section 11.3, pp. 274-275 in Section 11.6, and pp. 299-301 in Section 12.6.

The following apply to the final exam, which will include material from the preceding chapters as well, but to a much lesser degree (new material will be heavily emphasized).

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine; microprogramming (Section 14.5) is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, 19.6, and 20.5 are excluded.

Chapters 21-24 -- Input/output devices and Programming: problem possible on memory-mapped, polled, or interrupt-driven I/O. Sections 21.5, 21.6 and 22.6 are excluded.

Chapters 23-24 -- Buses, interfacing, interrupts: no problem or question.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Summer session 2003 offering of ECE 154

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2003 (June 23 to August 1), Enrollment Code 02766
Current catalog entry:	**154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* Computer architecture representation methods. Classical processor/memory/switch aspects of computer architecture: instructions, addressing, interpretation and control, I/O systems, and memory hierarchies. Aspects of system architecture: protection mechanisms and hardware aids to supervision, specialized processors, and multi-processor/computer systems. Evaluation methods and system analysis. (F, S, SS)
Catalog entry, new version for 2003-04:	**154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers. (F, S, SS)
Instructor:	Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>
TA:	Jonathan Lui
Meetings:	Lectures – MTW 8:00-9:20, Girvetz 1112 Discussions, led by the course TA – R 8:00-9:20, Girvetz 1112 Note minor variations in the last two weeks due to time conflicts and final exam
Consultation:	Instructor's office hours, held in Room 5155 Engineering I – M 11:00-12:30 (except 7/28), W 12:30-2:00 TA's office hours, held in Phelps 1435 – R 9:30-10:30, F 11:00-12:00
Motivation:	Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's viewpoint of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).
Prerequisite:	Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in one refresher-type lecture.
References:	Textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2004. Prepublication draft will be made available as course reader via the Alternative Copy Shop (6556 Pardall Rd., Isla Vista). Click on the link above to see the textbook's Web page. Recommended book (used as text in previous offerings) – David A. Patterson & John L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 2nd ed., 1998. The 2nd ed. is significantly different from the 1st ed. (chapter structure is the same, but the 1st ed. is 100+ pages shorter and also contains many errors).
Evaluation:	Students will be evaluated based on these 3 components with the given weights:

15% -- Five equal-weight weekly homework assignments posted on the course Web page by specified dates and due in class the following week (in six days). Homework descriptions appear below, following the course calendar.

25% -- Closed-book midterm exam (see the course calendar for date, time, and coverage).

60% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed.

Day/Date	Chap's	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 6/23	1-2	Review of digital logic circuits		
T 6/24	3-4	Computer technology and performance	HW1 (1-4)	Very important lecture
W 6/25	5	Instructions and addressing		
R 6/26	1-4	(Discussion: Logic design & performance)		
M 6/30	6-7	Procedures, data, and programs	HW1 due	
T 7/1	7-8	Assembly programs & ISA variations	HW2 (5-8)	
W 7/2	9	Number representation formats		
R 7/3	3	(Discussion: Instruction sets + HW1)		
M 7/7	10	Adders and multifunction ALUs	HW2 due	Important lecture
T 7/8	11	Multipliers and dividers	HW3 (9-12)	
W 7/9	12	Floating-point arithmetic		
R 7/10	9-12	(Discussion: Computer arithmetic + HW2)		
M 7/14	13	Stages of instruction execution	HW3 due	
T 7/15	14	Control unit synthesis	HW4 (13-16)	Important lecture
W 7/16	1-12	Midterm exam, 8:00-9:20 AM		
R 7/17	13-14	(Discussion: Control unit + HW3)		
M 7/21	15	Pipelined data paths	HW4 due	Very important lecture
T 7/22	16	Pipeline performance limits	HW5 (17-20)	
W 7/23	17-18	Main and cache memory concepts		Important lecture
R 7/24	19-20	Mass and virtual memory concepts		
M 7/28	15-16	(Discussion: Pipelined data paths + HW4)	HW5 due	No office hour today
T 7/29	21-24	Input/output and interrupts		Not covered in final
W 7/30	17-20	(Discussion: Memory system + HW5)		
R 7/31	1-20	Final exam, 7:00-9:20 AM, Girvetz 1112		++ Note extended time ++

Homework 1: Logic design and computer performance (due Monday, June 30)

Do the following problems from the textbook: 1.3, 2.6, 3.14a, 4.4, 4.11

Clarification on Problem 4.11a: Instruction mix means the fraction of instructions that are of each type. In this problem, two types of instructions are involved, so the answer would be the fraction x of instructions that are floating-point. The fraction of floating-point instructions executed is not the same as the fraction of time spent on executing them (50% in this case). The point here is to make you realize that the instruction mix and running time fractions are not the same but that they are related.

Homework 2: Instructions and assembly language (due Monday, July 7)

Do the following problems from the textbook: 5.2ab, 5.10ab, 6.5ab, 6.6, 7.3abc

Homework 3: Computer arithmetic (due Monday, July 14)

Do the following problems from the textbook: 9.6, 9.10, 10.7, 11.2ac, 12.6abc

Homework 4: Data path and control (due Monday, July 21; extended to Wednesday, July 23)

Do the following problems from the textbook: 13.12, 14.2a, 15.2, 16.9

Homework 5: Memory system design (due Monday, July 28; extended to Tuesday, July 29)

Do the following problems from the textbook: 17.3, 18.4ad, 18.7, 19.2, 20.4

Midterm and Final Exam Preparation

The following includes topics that will be emphasized, as well as list of exclusions from the midterm exam (Chapters 1-12) and final exam (Chapters 1-20). All sections not specifically excluded are required, even if they were not covered in class.

Chapters 1-2 -- Logic design: no direct problem, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, etc., used to explain the topics that follow.

Chapter 3 -- No problem or question.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 8.4 and 8.6.

Chapters 9-12 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (incl. distinction between arithmetic and logical shifts), adders and ALUs, shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic. Ignore pp. 261-262 in Section 11.3, Sections 11.5-11.6, pp. 297-298 in Section 12.6, and all but the first two paragraphs of p. 296.

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine; microprogramming is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB.

Chapters 21-24 -- Input/output, buses, interfacing, interrupts: no problem or question.

Chapters 25-28 -- Advanced architectures: no problem or question.

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Summer session 2002 offering of ECE 154

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2002 (June 24 to August 2), Enrollment Code 02253 (Discussion session 02261)
Catalog entry:	**154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* Computer architecture representation methods. Classical processor/memory/switch aspects of computer architecture: instructions, addressing, interpretation and control, I/O systems, and memory hierarchies. Aspects of system architecture: protection mechanisms and hardware aids to supervision, specialized processors, and multi-processor/computer systems. Evaluation methods and system analysis. (F, S, SS)
Catalog entry, new version proposed in August 2002:	**154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour.* The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers. (F, S, SS)
Instructor:	Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>
TA:	Hongtao Xu
Meetings:	Lectures – MTW 9:30-10:50, HSSB 1231 Discussions, led by the course TA – R 9:30-10:50, HSSB 1231
Consultation:	Instructor’s office hours, held in Room 5155 Engineering I – M 11:00-12:30, W 12:30-2:00 TA’s office hours, held in Room 101 Trailer 380 – R 11:00-12:00, F 10:00-11:00
Motivation:	Computer architecture is the study/specification of (digital) computer systems at the interface of

hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's viewpoint of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in one refresher-type lecture.

References: Textbook – B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, to appear in 2003. Prepublication draft will be made available as course reader or will be handed out in class. Click on the link above to see the textbook's Web page.
Recommended book (used as text in previous offerings) – David A. Patterson & John L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 2nd ed., 1998. The 2nd ed. is significantly different from the 1st ed. (chapter structure is the same, but the 1st ed. is 100+ pages shorter and also contains many errors).

Evaluation: Students will be evaluated based on these 3 components with the given weights:

15% -- Five equal-weight weekly homework assignments posted on the course Web page by specified dates and due in class the following week (in six days). Homework descriptions appear below, following the course calendar.

25% -- Closed-book midterm exam (see the course calendar for date, time, and coverage).

60% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed.

Day/Date	Chap's	Subject of Lecture or Discussion	HW (chap's)	Special Notes
M 6/24	1-2	Review of logic circuits		
T 6/25	3-4	Computer technology and performance	HW1 (1-4)	Very important lecture
W 6/26	5	Instructions and addressing		
R 6/27	1-4	(Discussion: Logic design & performance)		
M 7/1	6-7	Procedures, data, and programs	HW1 due	
T 7/2	7-8	Assembly programs & ISA variations	HW2 (5-8)	
W 7/3	9-10	Number representation, adders, & ALUs		
R 7/4	3	No discussion held: Independence Day		Holiday
M 7/8	11	Multipliers and dividers	HW2 due	No office hour today
T 7/9	12	Floating-point arithmetic	HW3 (9-12)	
W 7/10	5-8	(Discussion: Instruction sets + HW1)		Instructor away at conf.
R 7/11	9-12	(Discussion: Computer arithmetic + HW2)		Instructor away at conf.
M 7/15	13	Stages of instruction execution	HW3 due	
T 7/16	1-12	Midterm exam, 9:30-11:00 AM		++ Note extended time ++
W 7/17	14	Control unit synthesis	HW4 (13-16)	
R 7/18	13-14	(Discussion: Control unit + HW3)		
M 7/22	15	Pipelined data paths		
T 7/23	16	Pipeline performance limits	HW5 (17-20)	
W 7/24	17-18	Main and cache memory concepts	HW4 due	
R 7/25	15-16	(Discussion: Pipelined data paths + HW4)		
M 7/29	19-20	Mass and virtual memory concepts		
T 7/30	21-23	Input/output and interfacing	HW5 due	
W 7/31	24-25	Interrupts and some advanced topics		Not covered in final
R 8/1	17-23	(Discussion: Memory & I/O + HW5)		
F 8/2	1-23	Final exam, 1:00-3:30 PM		Place: North Hall 1109

Homework 1: Logic design and computer performance (due Monday, 2002 July 1)

Problem 1.19 Arithmetic expressions for logic gates
The arithmetic expressions characterizing logic gates (Fig. 1.1 in the notes) can be extended to gates with more than two inputs. This is trivial for AND gates. Write the equivalent arithmetic expressions for 3- and 4-input OR gates. Generalize the expression to an *h*-input OR gate.

Problem 2.15 Building larger shift registers and counters
a. Explain how you would build a 32-bit shift register, given two 16-bit shift registers.
b. Repeat part a for a 32-bit up counter, given two 16-bit up counters.

Problem 3.15 Effects of yield on die cost
A wafer containing 100 copies of a complex processor die costs $900 to manufacture. The area occupied by each processor is 2 cm^2 and the defect density is 2 per cm^2. What is the manufacturing cost per die?

Problem 4.7 Instruction mix and performance
This problem is a continuation of Example 4.6. We can redesign the machine M_1 so that its clock rate is 1.4 times the current rate (say, 1.4 GHz instead of 1 GHz). Doing this will require other design changes that increase all the CPIs by 1. How does M_2 compare to the redesigned M_1 in terms of performance?

Problem 4.15 Amdahl's law
You live in an apartment from which you have a 7-minute drive for your twice-a-week shopping trips to a nearby supermarket and a 20-minute drive to a warehouse store where you shop once every four weeks. You are planning to move to a new apartment. Compare the following two candidate locations with respect to the speedup they offer for your driving time during shopping trips.
a. An apartment that is 10 minutes away from both a supermarket and a warehouse store.
b. An apartment that is 5 minutes away from a supermarket and 30 minutes from a warehouse store.

Homework 2: Instructions and assembly language (due Monday, 2002 July 8)

Problem 5.4 Multiplying by a small power of two
Write a sequence of MiniMIPS instructions (using only the instructions in Table 5.1) to multiply the integer *x* stored in register `$s0` by 2^n, where *n* is a small nonnegative integer stored in `$s1`. The result should be placed in `$s2`. *Hint:* Use repeated doubling.

Problem 6.3 Divisibility by powers of two
A binary integer that has *h* consecutive 0s at its right end is divisible by 2^h. Write a MiniMIPS procedure that accepts a single unsigned integer in register `$a0` and returns the largest power of 2 by which it is divisible (an integer in [0, 32]) in register `$v0`.

Problem 7.3 Additional pseudoinstructions
The following are some additional pseudoinstructions that one could define for MiniMIPS. In each case, supply an equivalent MiniMIPS instruction or sequence of instructions with the desired effect.

```
partc: bgtz    reg,L           # if (reg) > 0, goto L
partg: triple  regd,regs       # regd = 3 ´(regs)
parth: mulacc  regd,reg1,reg2  # regd = (regd) + (reg1) ´(reg2)
```

Problem 8.2 Instruction formats
Categorize each of the MiniMIPS instruction given in Table 6.2 according to the number of addresses in its format (0-, 1-, 2-, or 3-address instruction, as in Fig. 8.2).

Homework 3: Computer arithmetic (due Monday, 2002 July 15)

Problem 9.11 Number radix conversion
Convert each of the following numbers from its indicated radix to radix-2 and radix-16 representations.
a. Radix-10 numbers: 12, 5 655, 76 545 336
b. Radix-12 numbers: 9a5, b0a, baabaa

Problem 9.15 Floating-point numbers
Consider the entries supplied for *min* and *max* in Table 9.1. Show how these values are derived and explain why the *max* values in the two columns are specified as being approximately equal to a power of 2.

Problem 10.x Brent-Kung carry network
Draw a diagram similar to Fig. 10.11 that corresponds to the carry network of a 16-digit adder. *Hint:* See Fig. 10.12.

Problem 11.1 Multiplication algorithm
a. By redoing the multiplication steps in Fig. 11.2, verify that if the cumulative partial product is initialized to 1011 instead of 0000, a multiply-add operation is performed.
b. Show that regardless of the radix *r* and the initial value of the *k*-digit $z^{(0)}$, the multiply-add result with *k*-digit operands is always representable in 2*k* digits.

Problem 12.x Floating-point arithmetic
Show the results of the following floating-point operations. Justify your answers.
a. $min +_{fp} max$
b. $min \acute{}_{fp} max$
c. $min /_{fp} max$

Homework 4: Data path and control (due Wednesday, 2002 July 24, one day later than originally announced, in order to allow time for covering the material in class)

Problem 13.x Control signals in the single-cycle data path
Extend Table 13.3 with lines corresponding to the following new instructions that might be added to the single-cycle MicroMIPS implementation. Justify your answers.
a. Shift left logical (`sll`)
b. Shift right arithmetic variable (`srav`)

Problem 14.x Extending the multicycle data path
Suggest some simple changes (the simpler, the better) in the multicycle data path of Fig. 14.3 so that the following instructions can be included in the machine's instruction set:
a. Load byte (`lb`).
b. Load byte unsigned (`lbu`).
c. Store byte (`sb`).

Problem 15.x Pipelined data path and control
The following sequence of instructions is to be executed on the pipelined MicroMIPS of Chapter 15; i.e., with no data forwarding or branch prediction logic. Determine how many bubbles must be inserted and where. Explain your reasoning in each step. Can you suggest any reordering of instructions that would reduce the number of bubbles?

```
       addi  $9,$zero,0
       addi  $12,$zero,5000
Loop:  addi  $12,$12,4
       lw    $8,40($12)
       add   $9,$9,$8
       addi  $11,$11,-1
       bne   $11,$zero,Loop
```

Problem 16.x Pipeline performance
A 10-stage instruction pipeline runs at a clock rate of 1 GHz. The data forwarding scheme and the instruction mix are such that for 15% of instructions one bubble, for 10% two bubbles, and for 5% four bubbles must be inserted in the pipeline. The equivalent single-cycle implementation would lead to a clock rate of 150 MHz.
a. What is the reduction in pipeline throughput over the ideal pipeline as a result of bubbles?
b. What is the speedup of the pipelined implementation over the single-cycle implementation?

Homework 5: Memory system design (due Tuesday, 2002 July 30)

Problem 18.x Cache memory design
A computer system has 4 GB of byte-addressable main memory and a 256-KB cache memory with 32-byte blocks.
a. Draw a diagram showing each of the components of a main memory address (i.e., how many bits for tag, set index, and byte offset) for a 4-way set-associative cache.
b. Draw a diagram showing the tag comparison circuits, generation of the cache miss signal, and the data output for the cache.
c. The performance of the computer system with 4-way set-associative cache architecture proves unsatisfactory. Two redesign options are being considered, implying roughly the same additional design and production costs. Option A is to increase the size of the cache to 512 KB. Option B is to increase the associativity of the 256 KB cache to 16-way. In your judgment, which option is more likely to result in greater overall performance and why?

Problem 18.y Cache memory performance
A computer system uses two levels of caches L1 and L2. L1 is accessed in one clock cycle and supplies the data in case of an L1 hit. For an L1 miss, occurring 3% of the time, L2 is consulted. An L2 hit incurs a penalty of 10 clock cycles while an L2 miss implies a 100-cycle penalty.
a. Assuming a pipelined implementation with a CPI of 1 when there are no cache misses whatsoever (i.e., ignoring data and control dependencies), calculate the effective CPI when L2's local miss rate is 25%.
b. If we were to model the 2-level cache as a single cache, what miss rate and miss penalty should we use?
c. Changing the mapping scheme of L2 from direct to 2-way set-associative can improve its local miss rate to 22% while increasing its hit penalty to 11 clock cycles due to the more complex access scheme. Ignoring cost issues, is this change a good idea?

Problem 19.x Virtual memory performance
The following computation is to be performed on a table T having 17 rows and 1024 columns. Note that i is row index and j is column index.

```
for j = [0 ... 1023] {
   temp = 0;
   for i = [0 ... 16]
      temp = temp + T[i][j];
   print(temp/17.0); }
```

The preceding program fragment computes an average value for each table column and prints it to the screen. Assume that each table element is a 32-bit floating-point number and that the memory is word-addressable. The temporary variable temp is kept in a processor register, so access to temp does not involve a memory reference. The main memory is paged and holds 16 pages of size 1024 words. The page replacement policy is "least-recently-used."

a. Assuming that T is stored on the disk in row-major format, how many page faults will be encountered and what is the main memory hit ratio?
b. What fraction of the misses in part a are compulsory? Capacity? Conflict?
c. Repeat part a, this time assuming that T is stored on the disk in column-major format.
d. What fraction of the misses in part c are compulsory? Capacity? Conflict?

Final Exam Preparation

Chapters 1-2 -- Logic design: no direct problem, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, etc., used to explain the topics that follow.

Chapter 3 -- No problem or question.

Chapter 4 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapters 5-8 -- Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Section 8.6.

Chapters 9-12 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (incl. distinction between arithmetic and logical shifts), shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic. Ignore pp. 198-199 in Section 11.3, Sections 11.5-11.6, and pp. 226-228 in Section 12.6.

Chapters 13-14 -- Data path and control: problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine; microprogramming is excluded.

Chapter 15-16 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapters 17-20 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB.

Chapters 21-22 -- Input/output: problem likely on I/O performance, polling vs. interrupts, and/or I/O addressing.

Chapters 23-24 -- Buses, interfacing, interrupts: no problem or question.

Chapters 25-28 -- Advanced architectures: no problem or question.

Solutions for the practice final exam

1. *Address translation*: The process by which physical memory address is derived from a given virtual address (also known as address mapping).
Bus arbitration: The process used to decide which of several units that need to use the bus is allowed to use it next.
Conflict miss: A cache miss that occurs because restricted mapping in the cache (direct or set-associative) has caused the required data to be overwritten by other data; does not apply to a fully associative cache.
Delayed branch: A type of conditional branch in which the instruction (or several instructions) immediately following the branch are always executed, whether or not the branch is taken.
Interrupt-driven I/O: Input/output operations that are performed at the request of devices that have something to send to the CPU or need to receive data from the CPU (as opposed to polling-based I/O in which the CPU takes the initiative).
Pseudoinstruction: An assembly-language command that is used as if it were a machine instruction but is replaced by one or more actual machine instructions during the assembly process.
Set-associative cache: A cache that allows an incoming cache line (block) to be mapped into any of a fixed number of locations (at least two).
TLB: (Translation lookaside buffer) A small cache that keeps the most recently used page table entries to avoid an extra memory access for translating a virtual address to a physical address.

2. (a) The largest k-bit unsigned integer is 2^k - 1 whose square is 2^(2k) - 2^(k+1) + 1. This is less than or equal to 2^(2k) - 1 for all k (so 2k bits are adequate) but it it greater than 2^(2k-1) - 1 for k > 1 (so 2k - 1 bits are inadequate, except in the uninteresting case of k = 1).
(b) The magnitude of k-bit 2's-complement numbers is at most 2^(k-1), so the magnitude of the product of two such numbers can be as large as 2^(2k-2). Therefore, the two MSBs of the 2k-bit product must be identical (00 for a positive product and 11 for a negative product). There is only one exception: The square of -2^(k-1), which is 2^(2k-2) begins with 01 at the most significant end.

3. (a) The ALU output is stored in rt for arithmetic and logic instructions with an immediate operand. Examples include addi, andi, xori.
(b) Data memory output is stored in a register only for lw instruction. In this case, the destination register is rt. So, data memory to rt is never used.
(c) Register $31 can be the destination of arithmetic/logic results when it is specified as rd or rt. The only instruction for which we choose register $31 implicitly is jal. In this case, the incremented PC value will be stored in $31. So, ALU to $31 is never used.

4. (a) It represents a multicycle implementation (due to the sequencing and branching logic shown). A single-cycle implementation is usually not microprogrammed; even if it were, the microprogram address logic would consist of a simple decoder that selects a single microinstruction to be executed for a given opcode.

(b) They allow the microprograms for several instructions to share a common segment and then branch out to do different things for different instructions (based on their opcodes).
(c) It is derived directly from a 2-bit field in the current microinstruction.
(d) Say, ALUSrc (which selects the lower input to the ALU) and RegWrite (which instructs the register file to perform a write operation). We can choose any two signals from the diagram of Problem 5.

5. (a) These are control signals that are carried along with the instruction until they are needed.
A represents control signals for the last pipeline stage (register writeback).
B represents control signals for the data cache access stage.
C represents control signals for the ALU operation stage.
(b) This mux allows the output of the ALU or the incremented PC value to be written in a register.
(c) This box extends a 16-bit immediate operand to 32 bits by replicating its sign bit (sign extension).

6. This problem was solved in Homework 5. It is included in this practice final as a representative example of problems on memory hierarchy.

7. (a) Rate of polling must be at least 600/min or 10/s to ensure that no data is lost. The time to execute 400 instructions is 400 / (20 000 000) s = 0.02 ms. Hence, polling time is 10 (rate/s) x 100 (terminals) x 0.02 = 20 ms in each second or 2%. This option is thus infeasible.
(b) Interrupt rate is at most 12 000 / min or 200/s. The time to execute 1000 instructions is 1000 / (20 000 000) s = 0.05 ms. Hence, interrupt servicing time is 200 (rate/s) x 0.05 = 10 ms in each second or 1%. This option is also infeasible.

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Summer session 2001offering of ECE 154

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2001 (June 25 to August 3), Enrollment Code 01875 (Discussion 01883)
Instructor:	Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>
TA:	Hongtao Xu
Meetings:	Lectures – MTW 8:00-9:20 AM, North Hall 1105 Discussions, led by the TA – R 8:00-9:20 AM, North Hall 1105
Consultation:	Instructor's office hours, held in Room 5155 Engineering I – TW 9:30-10:30 TA's office hours, held in Room 101 Trailer 380 – R 9:30-10:30, F 1:00-2:00
Motivation:	Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's viewpoint of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).
Prerequisite:	Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in one refresher-type lecture.
References:	Text – David A. Patterson & John L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 2nd ed., 1998. The 2nd ed. is significantly different from the 1st ed. (chapter structure is the same, but the 1st ed. is 100+ pages shorter and also contains many errors). The SPIM simulator for running MIPS assembly language programs can be obtained through the Internet (see p. xvii of the text for details). Although students are encouraged to experiment with SPIM, knowledge of SPIM is not a requirement for the course.
Evaluation:	Students will be evaluated based on these 3 components with the given weights: 15% -- Five equal-weight weekly homework assignments posted on the course Web page before each Tuesday (except in the last week of classes) and due in class the following Monday. Homework descriptions appear below, following the course calendar. 25% -- Closed-book midterm exam (see the course calendar for date, time, and coverage). 60% -- Closed-book final exam (see the course calendar for place, date, time, and coverage).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. It is a good idea to look over the specified course material *before* each lecture if possible. A six-week session is not long enough for covering the entire 900-page textbook. Students are encouraged to read other parts of the text, such as sections providing historical perspective, but the course exams are based only on the topics covered in class (including any handouts) and text pages listed in the "required" column below. Sections in the "recommended" column contain particularly useful background or supplementary material.

Day/Date	Chap	Subject of Lecture or Discussion	HWs	Required	Recomm	Optional

M 6/25	1	Computer systems and technology		3-28		32-43
T 6/26	B	Review of logic circuits	HW1	B3-B44		
W 6/27	2	Computer performance		54-75	76-83	83-89
R 6/28	1-2, B	(Discussion: Logic design & performance)				
M 7/2	3	Instructions and operands	#1 due	106-131		
T 7/3		Procedures, data, and programs	HW2	132-174	185-188	189-195
W 7/4		No lecture: Independence Day				
R 7/5	3	(Discussion: Assembly language + HW1)				
M 7/9	4	Basic ALU and multiplication	#2 due	210-264		
T 7/10		Division and Floating-point arithmetic	HW3	265-291	297-301	312-321
W 7/11		Recap: Instruction-set architecture				
R 7/12	4	(Discussion: Computer arithmetic + HW2)				
M 7/16	1-4	Midterm exam, 7:30-9:15 AM	#3 due	++ Note extended time ++		
T 7/17	5	Data path and control	HW4	338-372	373-377	
W 7/18		Control design and microprogramming		377-416		423-425
R 7/19	5	(Discussion: Datapath & control + HW3)				
M 7/23	6	Pipelined data path and control	#4 due	436-470	471-476	
T 7/24		Pipeline hazards and exceptions	HW5	476-509	510-514	525-528
W 7/25	7	Cache Memory		540-576	576-578	
R 7/26	6	(Discussion: Pipelining + HW4)				
M 7/30		Virtual Memory	#5 due	579-611		621-626
T 7/31	8	Input/output and interfacing		638-686		694-698
W 8/1	9	Road to higher performance		712-746	746-754	
R 8/2	7-8	(Discussion: Mem. hierarchy & I/O + HW5)				
F 8/3	1-8	Final exam, 8:00-11:00 AM, Girvetz 1112		++ Note different place/time ++		

Homework 1: Logic design and computer performance (due Monday, 2001 July 2)

All exercises in this homework are from the textbook.
A [15 points]: Do exercises 1-21 to 1-26.
B [15 points]: Do exercise B-13.
C [15 points]: Do exercise B-14.
D [10 points]: Do exercise 2.1.
E [10 points]: Do exercise 2.5.
F [20 points]: Do exercise 2.15.
G [15 points]: Do exercise 2.16.

Homework 2: Instructions and assembly programming (due Monday, 2001 July 9)

All exercises in this homework are from the textbook.
A [10 points]: Do exercise 3.1.
B [15 points]: Do exercise 3.6.
C [30 points]: Do exercise 3.11.
D [20 points]: Do exercise 3.17.
E [15 points]: Do exercise 3.18.
F [10 points]: Do exercise 3.20.

Homework 3: Computer arithmetic and ISA (due Monday, 2001 July 16)

All but one (item H) of the exercises in this homework are from the textbook.
A [10 points]: Do exercise 4.15.
B [15 points]: Do exercise 4.19.
C [10 points]: Do exercise 4.26.
D [15 points]: Do exercise 4.40.
E [10 points]: Do exercise 4.41.
F [10 points]: Do exercise 4.49.
G [10 points]: Do exercise 4.50.
H [10 points]: Modify the top diagram in Figure 4.56 so that E and F are added first, with their sum then added to the sum of A and B; in other words, A + B and E + F are formed in parallel before using the 5-bit adder in the bottom row of the diagram. Calculate the time for this new arrangement and compare the result to those obtained in Exercise 4.50.

I [10 points]: Do exercise 4.55.

Homework 4: Datapath and control (due Monday, 2001 July 23)

All exercises in this homework are from the textbook.
A [15 points]: Do exercise 5.3.
B [15 points]: Do exercise 5.7.
C [15 points]: Do exercise 5.9.
D [15 points]: Do exercise 5.10.
E [15 points]: Do exercise 5.16.
F [25 points]: Do exercise 5.23.

Homework 5: Pipelining and memory hierarchy (due Monday, 2001 July 30)

All exercises in this homework are from the textbook.
A [10 points]: Do exercise 6.4.
B [20 points]: Do exercise 6.9.
C [10 points]: Do exercise 6.15.
D [15 points]: Do exercise 6.21.
E [20 points]: Do exercise 6.31.
F [10 points]: Do exercise 7.7.
G [15 points]: Do exercise 7.13.

Final Exam Preparation

Appendix B -- Logic design: no direct problem, but you need to know concepts such as tristate buffers, multiplexers, register files, etc., used to explain the topics that follow.

Chapter 2 -- Computer performance: problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.

Chapter 3 -- Instruction-set architecture: no direct problem, only conceptual questions (see problem 1 in the practice final). However, you do need to know various instructions and their execution steps to be able to explain control, pipelining, pipeline hazards, etc.

Chapter 4 -- Computer arithmetic: problem likely on 2's-complement numbers, shift/logical operations (incl. distinction between arithmetic and logical shifts), shift-add multiplication, shift-subtract division, floating-point numbers, and/or floating-point arithmetic (no need to know floating-point instructions in MIPS).

Chapter 5 -- Data path and control: problem very likely on single-cycle design, control signal generation, multicycle design, control state machine, and/or microprogramming.

Chapter 6 -- Pipelining: problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.

Chapter 7 -- Memory hierarchy: problem very likely on the need for memory hierarchy, cache memory (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB.

Chapter 8 -- I/O and interfacing: problem likely on I/O performance, polling vs. interrupts, I/O addressing, buses, and/or bus arbitration.

Chapter 9 -- Parallel processing: no problem or question.

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Summer session 2000 offering of ECE 154

Course:	ECE 154 – Introduction to Computer Architecture, University of California, Santa Barbara, Summer Session 2000 (June 26 to August 4), Enrollment Code 09290
Instructor:	Behrooz Parhami, Room 5155 Engineering I, Phone 805-893-3211, <Instructor's e-mail>
TA:	Hongtao Xu, Room 101 Trailer 380
Meetings:	Lectures – MTW 9:30-11:00; Room 1431 Phelps Hall Discussions, conducted by the TA – R 9:30-11:00; Room 1431 Phelps Hall (in weeks 3 & 6, discussion will be held on Wed. and midterm/final exam on Thur.)
Consultation:	Instructor's office hours, held in Room 5155 Engineering I – TWR 11:00-12:00 TA's office hours, held in Room 101 Trailer 380 – MF 11:00-12:00

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's viewpoint of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participating in computer design efforts and for learning the advanced techniques used in vector supercomputers (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Prerequisite: Familiarity with logic design and digital circuits (ECE 152A or equivalent). Fundamentals of digital logic circuits will be reviewed in one refresher-type lecture.

References: Text – David A. Patterson & John L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 2nd ed., 1998. The 2nd ed. is significantly different from the 1st ed. (chapter structure is the same, but the 1st ed. is 100+ pages shorter and also contains many errors). The SPIM simulator for running MIPS R2000/R3000 assembly language programs can be obtained through the Internet (see p. xvii of the text for details). Although students are encouraged to experiment with SPIM, knowledge of SPIM is not a requirement for the course.

Evaluation: Students will be evaluated based on these 3 components with the given weights:

15% -- Five equal-weight homework assignments handed out every Monday, except in the last week of classes. Each homework is due the following Monday.

25% -- Closed-book midterm exam, covering Chapters 1-4 and Appendix B (see the course calendar for date and time).

60% -- Closed-book final exam covering Chapters 1-8 (see the course calendar for details).

Calendar:

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. It is a good idea to look over the specified course material *before* each lecture if possible. A six-week session is not long enough for covering the entire 900-page textbook. Students are encouraged to read other parts of the text, such as sections providing historical perspective, but the course exams are based only on the topics covered in class (including any handouts) and text pages listed in the "required" column below. Sections in the "recommended" column contain particularly useful background or supplementary material.

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M 6/26	1	Computer technology	HW1	3-28		32-43
T 6/27*	B	Review of logic circuits		B3-B44		
W 6/28*	2	Computer performance		54-75	76-83	83-89
R 6/29		(Discussion: Logic & performance)				
M 7/3	3	Instructions and operands	HW2	106-131		
T 7/4		No lecture: Independence Day				
W 7/5		Procedures, data, & programs		132-174	185-188	189-195
R 7/6		(Discussion: Assembly language)				
M 7/10	4	Basic ALU & multiplication	HW3	210-264		
T 7/11		Division & Floating-point		265-291	297-301	312-321
W 7/12		(Discussion: Computer arithmetic)				
R 7/13		Midterm exam, 9:30-11:30		++ Note the extended time ++		
M 7/17	5	Data path and control	HW4	338-372	373-377	
T 7/18		Control design (microprogramming)		377-416		423-425
W 7/19	6	Pipelined data path & control		436-470	471-476	
R 7/20		(Discussion: Pipelining & control)				
M 7/24		Pipeline hazards & exceptions	HW5	476-509	510-514	525-528
T 7/25	7	Cache Memory		540-576	576-578	
W 7/26		Virtual Memory		579-611		621-626
R 7/27		(Discussion: Memory hierarchy)				
M 7/31	8	Input/output & interfacing		638-686		694-698
T 8/1	9	Parallel processing		712-746	746-754	
W 8/2		(Discussion: I/O & parallel processing)				
R 8/3		Final exam, 9:30-12:30		++ Note the extended time ++		

* Videotape: On Tue. 6/27 and Wed. 6/28, the instructor will be away at a technical conference. The class will be held in the usual place and time with special videotaped lectures.

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