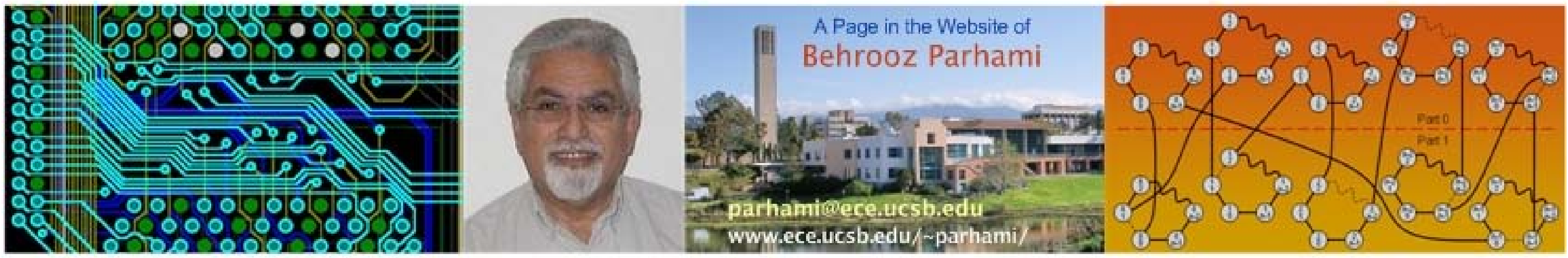


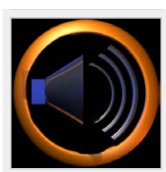
- **Home & Contact**
- **Curriculum Vitae**
- **Research**
  - Computer arithmetic
  - Parallel processing
  - Fault tolerance
  - Broader research
  - Research history
  - List of publications
- **Teaching**
  - ECE1 Freshman sem
  - ECE154 Comp arch
  - ECE252B Comp arith
  - ECE252C Adv dig des
  - ECE254B Par proc
  - ECE257A Fault toler
  - Teaching experience
  - Student supervision
  - Math + Fun!
- **Textbooks**
  - Computer arithmetic
  - Parallel processing
  - Fault tolerance
  - Comp architecture
  - Other books
- **Service**
  - Professional activities
  - Academic service
  - Community service
  - Industrial consulting
- **Files & Documents**
- **Useful Links**

Behrooz Parhami's ECE 252B Course Outline and Schedule

Computer Arithmetic, Spring 2009

Enrollment code: 11353
Prerequisite: ECE 152A and ECE 152B (or equivalents)
Class meetings: TR 12:00-1:30, Girvetz 2115
Instructor: Professor Behrooz Parhami
Open office hours: T 2:00-3:30, R 10:00-11:30, HFH 5155
Course announcements: Listed in reverse chronological order
Course calendar: Schedule of lectures, homework, and exams
Homework assignments: Four assignments, worth a total of 20%
Exams: Closed-book midterm, worth 30%
Research paper: Report and short oral presentation, worth 50%
Research paper guidlines: Brief guide to format and contents
References: Textbook and other sources (**Textbook's web page**)
Lecture slides: Available on the textbook's web page
Miscellaneous information: Motivation, catalog entry, history

Course Announcements



2009/06/18: The spring 2009 offering of ECE 252B is now officially over and course grades have been reported to the Registrar's Office. There will be no further updates to this Web page. Have a pleasant summer!
2009/05/28: All lecture slides, with the exception of those for Part VII (Chapters 25-28) of the textbook, have been updated for 2009.
2009/05/18: Research paper title and references are due this week. Paper abstract and outline are due on 6/2 (extended from 5/28). Lecture slides for Part V of the textbook have been updated.
2009/05/01: As announced in class, in preparation for the midterm exam, there will be extra instructor office hours on M 5/4, 2:00-3:30 PM. Updated lecture slides for Part IV of the textbook are now available.
2009/04/19: HW#2 has been posted below (ch. 9-12, due R 4/30). Lecture slides, available from the textbook's Web page, have been updated up to Chapter 8 and will be updated no later than T 4/21 for Chapters 9-12. Please note that preliminary references for your research topic will be due in 9 days (T 4/28).
2009/04/02: Our classroom has changed to Girvetz 2115, because the old classroom (Phelps 1437) did not provide an adequate computer projection system. Updated lecture slides for Parts I and II of the textbook (Chap. 1-8) are now available, as are lead references for each of the suggested research topics.
2009/03/27: The course lecture schedule has been modified and is now final.
2009/03/14: Welcome to the ECE 252B web page for spring 2009. The following tentative information is supplied for planning purposes only. Details will be finalized in late March 2009 and updated weekly thereafter. The course textbook is now available at the campus bookstore; bear in mind that you can usually get a much better price from on-line sources.

Course Calendar

Course lectures, homework assignments, exams, and research milestones have been scheduled as follows. This schedule will be strictly observed. Please review the first two chapters in the textbook (before the first class, if possible). These chapters contain material that you should already know. PowerPoint and pdf files of course lectures, including the skipped material in Chapters 1-2, can be found on the **textbook's web page**.

Day & Date (book chapters) Lecture/discussion topic [Homework posted/due] {Special notes}
T 03/31 (ch. 3-4) Redundant and residue representations {Introductory survey}

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Blog & books

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Poetry

Pet peeve

Virtual retirement

CE Program

ECE Department

UCSB Engineering

UC Santa Barbara

R 04/02 (ch. 5) Basic addition and counting

T 04/07 (ch. 6) Carry-lookahead adders [HW1 posted, ch. 1-8]
R 04/09 (ch. 7) Variations in fast adders

T 04/14 (ch. 8) Multioperand addition {Research topic defined}
R 04/16 (ch. 9) Basic multiplication schemes [HW1 due]

T 04/21 (ch. 10) High-radix multipliers [HW2 posted, ch. 9-12]
R 4/23 (ch. 11) Tree and array multipliers

T 04/28 (ch. 12) Variations in multipliers {Preliminary research references due}
R 04/30 (ch. 13) Basic division schemes [HW2 due]

T 05/05 (ch. 1-12) Midterm exam, closed book, 12:00-2:00 {Note the extended time}
R 05/07 (ch. 14) High-radix division

T 05/12 (ch. 15) Variations in dividers [HW3 posted, ch. 13-16]
R 05/14 (ch. 16) Division by convergence

T 05/19 (ch. 17-18) Floating-point numbers and operations {Research title and references due}
R 05/21 (ch. 19-20) Errors, precision, and certifiability [HW3 due] [HW4 posted, ch. 17-22]

T 05/26 (ch. 21) Square-rooting methods
R 05/28 (ch. 22) CORDIC algorithms {Research paper abstract and outline due}

T 06/02 (ch. 23-24) Other topics in function evaluation [HW4 due] {Instructor/course evaluation survey}
R 06/04 Research poster presentations

M 06/07 to W 06/10 {Instructor away at ARITH-19 conference}
R 06/11 {Final research paper due by midnight}

W 06/17 {Course grades to be submitted by midnight}

Homework Assignments

-Turn in solutions in class before the lecture begins.
-Because solutions will be handed out on the due date, no extension can be granted.
-Use a cover page that includes your name, course name, and assignment number.
-Staple the sheets and write your name on top of each sheet in case they are separated.
-Although some cooperation is permitted, direct copying will have severe consequences

Homework 1: Number systems and addition (ch. 1-8, due R 2009/04/16, 12:00 noon)
Do Problems 1.2, 5.5m, 6.13, and 8.13 from the textbook, and Problem 3.24 defined below.
Problem 3.24 Shifting of stored-carry numbers An unsigned binary number can be divided by 2 via a single-bit right shift. The same property holds for 1's- and 2's-complement numbers, provided that the sign bit is shifted into the vacated bit at the left end of the number (sign extension).
a. Show, by means of an example, that a stored-carry number cannot be divided by 2 via independent right shift of both the sum and carry bit-vectors [Tenc06].
b. Design a simple circuit that allows division by 2 via right shift, by supplying correct bit values to be shifted into the vacated positions at the left end.
c. Show that the modification of part b is not needed when the right-shifted stored-carry number is generated by adding an ordinary binary number to a stored-carry number.
[Tenc06] Tenca, A.F., S. Park, and L.A. Tawalbeh, "Carry-Save Representation Is Shift-Unsafe: The Problem and Its Solution," *IEEE Trans. Computers*, Vol. 55, No. 5, pp. 630-635, May 2006.

Homework 2: Multiplication (ch. 9-12, due R 2009/04/30, 12:00 noon)
Do Problems 9.7, 10.12, 10.13, 11.4, 12.13 from the textbook.

Homework 3: Division (ch. 13-16, due R 2009/05/21, 12:00 noon)
Do Problems 13.9, 13.13abc, 14.4ab, 15.5, 16.11 from the textbook.

Homework 4: Floating-point and function evaluation (ch. 17-22, due T 2009/06/02, 12:00 noon)
Do Problems 17.7, 18.9, 19.15 (correct the sign of *y* to "+"), 21.3a, 22.2c from the textbook.

Sample Exams and Study Guide

The following sample exam (from spring 2007) is meant to indicate the types and levels of problems, rather than the coverage (which is outlined in the course calendar). Students are responsible for all sections and topics (in the textbook and class handouts) that are not explicitly excluded in the study guide that follows the sample exam, even if the material was not covered in class lectures.

Sample Midterm Exam (105 minutes)
Problem 1 [15 points] Defining concepts and terms. Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [3 points each]: Manchester carry chain; Multiplier recoding; *ulp*; Conditional-sum adder; Parallel prefix graph
Problem 2 [10 points] Number representation. Show that flipping (complementing) the sign bit of *k*-bit numbers in 2's-complement format results in biased representation and determine the bias amount that characterizes this new representation.
Problem 3 [20 points] Basic design concepts. Draw diagrams showing each of the following. No explanation is necessary; the diagrams should be self-explanatory.
a. How an ordinary binary adder can be augmented to perform addition or subtraction of 2's-complement numbers under the control of an add'/sub signal (0 means "add", 1 means "subtract").
b. How 2-bits-at-a-time or radix-4 sequential multiplication might be performed at high speed without Booth's recoding and without precomputing 3 times the multiplicand.
Problem 4 [15 points] Carry-skip addition.
a. Show that the optimal block width *b* in a fixed-block carry-skip adder is proportional to the square root of the word width *k*. [10 points]
b. Briefly discuss why carry-skip adders are of interest at all, given that faster logarithmic-time adders are available. [5 points]
Problem 5 [15 points] Multioperand addition. The following describes a multioperand addition process in tabular form:

0 0 8 8 8 8 8 8 8 8

0 2 6 6 6 6 6 6 6 4

0 4 4 4 4 4 4 4 3 2

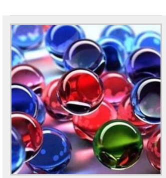
1 3 3 3 3 3 3 3 2 1

2 2 2 2 2 2 2 2 1 1

a. Explain the process described by this table. [5 points]
b. In the hardware implementation implied by the table, what component types are used and how many of each? Be as precise as possible in specifying the components used. [10 points]
Problem 6 [25 points] Two's-complement multiplication.
a. Represent $x = 3$, $y = -3$, and $z = 5$ as 4-bit 2's-complement numbers. [5 points]
b. Using the right-shift algorithm, perform *x* times *z*, using the representations of part a, to get the 8-bit product $p = 15$. [10 points]
c. Using the left-shift algorithm, perform *y* times *z*, to get the 8-bit product $p' = -15$. [10 points]

Midterm Exam Study Guide
The following textbook sections are excluded from the midterm exam: 3.4-3.6, 4.4-4.6, 6.3, 7.2, 10.5

Research Paper and Presentation



Each student will review a subfield of computer arithmetic or do original research on a selected and approved topic. A tentative list of research topics is provided below; however, students should feel free to propose their own topics for approval. A publishable report earns an "A" for the course, regardless of homework and midterm grades. See the course calendar for schedule and due dates and **Research Paper Guidlines** for formatting tips.

01. Modulo-(2^a+1) Number Representations and Arithmetic (Assigned to: TBD)

H. T. Vergos and C. Efstathiou, "Efficient Modulo 2^n + 1 Adder Architectures," *Integration, the VLSI J.*, Vol. 42, pp. 149-157, 2009.

G. Jaberipur and B. Parhami, "Unified Approach to the Design of Modulo-(2^n±1) Adders Based on Signed-LSB Representation of Residues," *Proc. 19th IEEE Int'l Symp. Computer Arithmetic*, 8-10 June 2009, to appear. [Preprint available via B. Parhami's publications Web page.]

02. Number representation with discrete logarithms (Assigned to: TBD)
A. Fit-Florea, L. Li, M. A. Thornton, and D. W. Matula, "A Discrete Logarithm Number System for Integer Arithmetic Modulo 2^k: Algorithms and Lookup Structures," *IEEE Trans. Computers*, Vol. 58, No. 2, pp. 163-174, February 2009.

03. A Survey of Hardware Multipliers in Microprocessors (Assigned to: TBD)
G. Colon-Bonet and P. Winterrowd, "Multiplier Evolution: A Family of Multiplier VLSI Implementations," *Computer J.*, Vol. 51, No. 5, pp. 585-594, 2008.

04. Dedicated hardware multipliers on FPGA chips (Assigned to: **Derek Spadaro**)
Using Embedded Multipliers in Spartan-3 FPGAs

05. Radix-16 SRT Division in Intel's New Penryn Processor (Assigned to: TBD)
[Intel's] New Radix-16 Divider

06. Augmenting FPGAs for Faster Arithmetic Operations (Assigned to: **C.-T. Tim Huang**)
H. Parandeh-Afshar, P. Brisk, and P. Ienne, "A Novel FPGA Logic Block for Improved Arithmetic Performance," *Proc. Int'l Symp. Field Programmable Gate Arrays*, 2008, pp. 171-180.

07. Cube Roots: Hardware Algorithms and Applications (Assigned to: **Jing Fu**)
A. Pineiro, J. D. Bruguera, F. Lamberti, and P. Montuschi, "A Radix-2 Digit-by-Digit Architecture for Cube Root," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 562-566, April 2008.
Cube-Roots via Newton-Raphson Method

08. Accurate Summation of Sets of Floating-Point Numbers (Assigned to: TBD)
A. Eisinberg and G. Fedele, "Accurate Floating-Point Summation: A New Approach," *Applied Mathematics and Computation*, Vol. 189, pp. 410-424, 2007.
T. Ogita, S. M. Rump, and S. Oishi, "Accurate Sum and Dot Product," *SIAM J. Scientific Computing*, Vol. 26 , No. 6, pp. 1955-1988, 2005.

09. Function Evaluation by Piecewise Linear Approximation (Assigned to: TBD)
N. Takagi, "Powering by a Table Look-Up and A Multiplication with Operand Modification," *IEEE Trans. Computers*, Vol. 47, No. 11, pp. 1216-1222, Nov. 1998.
O. Gustafsson and K. Johanson, "Multiplierless Piecewise Linear Approximation of Elementary Functions," *Proc. 40th Asilomar Conf. Signals, Systems, and Computers*, October 2006.

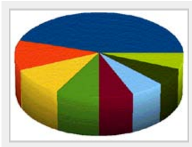
10. Smaller Lookup Tables via Nonuniform Segmentation (Assigned to: **Crystal H.-F. Wei**)
D.-U Lee, R. C. C. Cheung, W. Luk, and J. D. Villasenor, "Hierarchical Segmentation for Hardware Function Evaluation," *IEEE Trans. VLSI Systems*, Vol. 17, No. 1, pp. 103-116, January 2009.
T. Sasao, S. Nagayama, and J. T. Butler, "Numerical Function Generators Using LUT Cascades," *IEEE Trans. Computers*, Vol. 56, No. 6, pp. 826-838, June 2007.

11. Arithmetic in the European Logarithmic Microprocessor (Assigned to: TBD)
J. N. Coleman, et al., "The European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 532-546, April 2008.
J. N. Coleman, E. I. Chester, C. I. Softley, and J. Kadlec, "Arithmetic on the European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 49, No. 7, pp. 702-715, July 2000.

12. Arithmetic in IBM's Blue Gene/L Parallel Supercomputer (Assigned to: **S.-H. Brady Lin**)
J. Lorenz, S. Kral, F. Franchetti, and C.W. Ueberhuber, "Vectorization Techniques for the Blue Gene/L Double FPU," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 437-446, March/May 2005.

S. Chatterjee, et al., "Design and Exploitation of a High-Performance SIMD Floating-Point Unit for Blue Gene/L," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 377-391, March/May 2005.

Grade Statistics



All grades listed are in percent.
HW1 grades: Range = [67, 90], Mean = 75, SD = 09, Median = 71
HW2 grades: Range = [47, 75], Mean = 66, SD = 11, Median = 69
HW3 grades: Range = [50, 93], Mean = 74, SD = 16, Median = 75
HW4 grades: Range = [82, 92], Mean = 88, SD = 04, Median = 89
Midterm grades: Range = [35, 88], Mean = 70, SD = 22, Median = 75
Research paper and presentation grades: Range = [30, 85], Mean = 62, SD = 21, Median = 60

References

Required text: B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, Oxford University Press, 2000. Publisher's list price $139.00, UCSB Bookstore price $125.00/new, $93.75/used. The bookstore has been instructed to order the fourth or a newer printing of the textbook in which many of the early errors have been corrected. If you obtain a used copy of the third or earlier printing, make sure that you visit the **textbook's web page** which contains an errata. Lecture slides are also available there.

Some useful books (not required):
Deschamps/Bioul/Sutter, *Synthesis of Arithmetic Circuits: ...* , Wiley, 2006 (TK7895.A65D47)
Ercegovac/Lang, *Digital Arithmetic*, Morgan Kaufmann, 2004 (QA76.9.C62E73)
Swartzlander, *Computer Arithmetic*, vols. 1-2, IEEE Computer Society Press, 1990 (QA76.6.C633)
Koren, *Computer Arithmetic Algorithms*, 2nd ed., A K Peters, 2002 (QA76.9.C62K67)
Omondi, *Computer Arithmetic Systems: ...* , Prentice-Hall, 1994 (QA76.9.C62O46)
Ercegovac/Lang, *Division and Square Root: ...* , Kluwer, 1994 (QA76.9.C62E73)
Oklobdzija, *High-Performance System Design*, IEEE Press, 1999 (TK7871.99.M44037)
Waser/Flynn, *Intro. Arithmetic for Digital Systems Designers*, HR&W, 1982 (TK7895.A65W37.1982)
Knuth, *The Art of Computer Programming: Seminumerical Algorithms*, Wiley, 1981 (QA76.6.K64 vol 2)
Kulisch/Miranker, *Computer Arithmetic in Theory and Practice*, Academic Press, 1981 (QA162.K84)

Research resources:
Proc. IEEE Symp. Computer Arithmetic, 1969, 72, 75 78, 81 and subsequent odd years; ARITH-19, June 2009
On-line proceedings for IEEE Symp. Computer Arithmetic, 1969-2007
IEEE Trans. Computers, particularly special issues or sections on computer arithmetic (8/70, 6/73, 7/77, 4/83, 8/90, 8/92, 8/94, 7/98, 7/00, 3/05, 2/09)
UCSB library's electronic journals, collections, and other resources
UCSB library's research guide in ECE

Miscellaneous Information

Motivation: Computer arithmetic is a subfield of digital computer organization. It deals with the hardware realization of arithmetic functions to support various computer architectures as well as with arithmetic algorithms for firmware/software implementation. A major thrust of digital computer arithmetic is the design of hardware algorithms and circuits to enhance the speed of various numeric operations. Thus much of what is presented in this course complements the architectural and algorithmic speedup techniques covered as part of the advanced computer architecture (ECE 254A/B/C) sequence.

Catalog entry: **252B. Computer Arithmetic. (4) PARHAMI.** *Prerequisites: ECE 152A-B. Lecture, 4 hours*. Standard and unconventional number representations. Design of fast two-operand and multioperand adders. High-speed multiplication and division algorithms. Floating-point numbers, algorithms, and errors. Hardware algorithms for function evaluation. Pipelined, digit-serial and fault-tolerant arithmetic processors.

History: Professor Parhami took over the teaching of ECE 252B from the late Dr. James Howard in the winter quarter of 1989. By covering sequential machines, computer arithmetic, and advanced microprocessor-based design, the graduate course sequence ECE 252A/B/C was meant to provide a firm foundation in the theories and techniques of advanced digital design. During the first few offerings of ECE 252B, Professor Parhami gradually modified the content to increase both its coverage and research orientation (ECE 252A and 252C later underwent similar transformations by Professor Kwang-Ting Cheng and Professor Parhami, respectively). In 2000, based on a decade of experience in teaching this course, Professor Parhami published a graduate-level textbook, ***Computer Arithmetic: Algorithms and Hardware Designs*** (Oxford University Press), which is being used at many universities worldwide. The second edition of this textbook will appear in 2010.

Offerings of ECE 252B from 2000 to 2008 (PDF file)