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Behrooz Parhami's ECE 252B Course Page for Spring 2011

Computer Arithmetic

Enrollment code: 11312

Prerequisite: ECE 152A and ECE 152B (or equivalents)

Class meetings: TR 10:00-11:30, Girvetz 1108

Instructor: Professor Behrooz Parhami

Open office hours: M 11:00-12:30, W 12:00-1:30, HFH 5155

Course announcements: Listed in reverse chronological order

Course calendar: Schedule of lectures, homework, and exams

Homework assignments: Four assignments, worth a total of 20%

Exams: Closed-book midterm, worth 30%

Research paper: Report and short oral presentation, worth 50%

Research paper guidelines: Brief guide to format and contents

Poster presentation tips: Brief guide to format and structure

Policy on academic integrity: Please read very carefully

Grade statistics: Range, mean, etc. for homework and exam grades

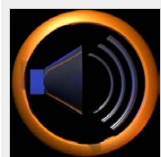
References: Textbook and other sources ([Textbook's web page](#))

Lecture slides: Available on the textbook's web page

Miscellaneous information: Motivation, catalog entry, history



Course Announcements



2011/06/15: The spring 2011 offering of ECE 252B is officially over and course grades have been reported to the Registrar. Comments on research papers will be e-mailed to students over the next few days (by 6/20). There will be no further updates to this Web page.

2011/05/24: Lecture slides for Part VI of the textbook have been updated for the spring 2011 quarter. Remember that, per the course schedule, research paper abstract and outline are due on R 5/26; it would be okay to e-mail these items to me by 8:00 AM on Sat. 5/28, as I plan to

read them over the weekend. As for the question about square-rooting with subnormal IEEE 754 numbers, one would normalize the subnormal operand by an even shift amount (for example, if the significand is 2^{-23} in short format, a 24-bit left shift is applied). The originally even exponent of -126 will remain even after the corresponding adjustment, while the significand will be in [1, 4). Then, the square-root is extracted as usual, with the resulting significand in [1, 2) and the halved exponent in [-63, -75] for short format and in [-63, -89] for long format. That is, the resulting square root is derived as a normalized number in all cases.

2011/05/10: Homework assignments 3 and 4 have been posted below. Remember that your finalized research title and reference list are due next week (T 5/17).

2011/04/25: Lecture slides for Parts IV and V of the textbook have been updated for the spring 2011 quarter. Remember that the preliminary list of references for your research paper is due tomorrow (T 4/26).

2011/04/16: Homework 2 has been posted and lecture slides for Part III of the textbook have been updated for the spring 2011 quarter.

2011/04/12: Research topics have been assigned according to submitted preferences. In two cases, the assignments are tentative. I am awaiting further information from the students involved before finalizing their topics.

2011/04/06: Research topics and associated references have been updated. Please e-mail me a list of at least three topics, in order of your preference, by T 4/12. As a rule, topics chosen by different students should be distinct.

2011/03/30: Lecture slides for Parts I and II of the textbook have been updated for the spring 2011 quarter. Homework 1 will be posted over the next weekend.

2011/03/24: Welcome to the Web page for the graduate course ECE 252B in spring 2011. Information on the

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CE Program

ECE Department

UCSB Engineering

UC Santa Barbara

spring 2010 and earlier offerings of the course is available via PDF files accessible under the "History" section at the end of this page. Throughout the spring 2011 quarter, this "Announcements" section will alert you to significant additions or changes to the ECE 252B Web page.

Course Calendar



Course lectures, homework assignments, exams, and research milestones have been scheduled as follows. This schedule will be strictly observed. Please review the first two chapters in the textbook (before the first class, if possible). These chapters contain material that you should already know. PowerPoint and pdf files of course lectures, including the skipped material in Chapters 1-2, can be found on the [textbook's web page](#).

Day & Date (book chapters) Lecture/discussion topic [Homework posted/due] {Special notes}

T 03/29 (ch. 3-4) Redundant and residue representations {Introductory survey}

R 03/31 (ch. 5) Basic addition and counting

T 04/05 (ch. 6) Carry-lookahead adders [HW1 posted, ch. 1-8]

R 04/07 (ch. 7) Variations in fast adders

T 04/12 (ch. 8) Multioperand addition {Research topic defined}

R 04/14 (ch. 9) Basic multiplication schemes [HW1 due]

T 04/19 (ch. 10) High-radix multipliers [HW2 posted, ch. 9-12]

R 04/21 (ch. 11) Tree and array multipliers

T 04/26 (ch. 12) Variations in multipliers {Preliminary research references due}

R 04/28 (ch. 13) Basic division schemes [HW2 due]

T 05/03 (ch. 1-12) Midterm exam, closed book, 10:00-12:00 {Note the extended time}

R 05/05 (ch. 14) High-radix division

T 05/10 (ch. 15) Variations in dividers [HW3 posted, ch. 13-16]

R 05/12 (ch. 16) Division by convergence

T 05/17 (ch. 17-18) Floating-point numbers and operations {Research title and references due}

R 05/19 (ch. 19-20) Errors, precision, and certifiability [HW3 due] [HW4 posted, ch. 17-22]

T 05/24 (ch. 21) Square-rooting methods

R 05/26 (ch. 22) CORDIC algorithms {Research paper abstract and outline due}

T 05/31 (ch. 23-24) Other topics in function evaluation [HW4 due] {Instructor/course evaluation survey}

R 06/02 Research poster presentations {PDF file of poster due by midnight}

R 06/09 {Final research paper due by midnight}

W 06/15 {Course grades must be submitted by midnight}

Homework Assignments



- Turn in solutions in class before the lecture begins.
- Because solutions will be handed out on the due date, no extension can be granted.
- Use a cover page that includes your name, course name, and assignment number.
- Staple the sheets and write your name on top of each sheet in case they are separated.
- Although some cooperation is permitted, direct copying will have severe consequences

Homework 1: Number systems and addition (ch. 1-8, due R 2011/04/14, 10:00 AM)

Do the following problems from the textbook: 1.4 [20 pts.], 3.2 [15], 6.15 [20], 7.28 [15], 8.1 [15], 8.14 [15]

Homework 2: Multiplication (ch. 9-12, due R 2011/04/28, 10:00 AM)

Do the following problems from the textbook: 9.4b [15 pts.], 9.14abc [20], 10.18 [15], 11.6 [15], 11.19ab

[15], 12.13 [20]

Homework 3: Division (ch. 13-16, due R 2011/05/19, 10:00 AM)

Do the following problems from the textbook: 13.8 [25 pts.], 13.12bc [10], 14.2d [15], 14.7 [10], 15.5 [20], 16.18 [20]

Homework 4: Floating-point and function evaluation (ch. 17-22, due T 2011/05/31, 10:00 AM)

Do the following problems from the textbook: 17.18 [15 pts.], 18.6bc [20], 19.10 [15], 20.21 [15], 21.3c [15], 22.20 [20]

Sample Exams and Study Guide



The following sample exam (from spring 2007) is meant to indicate the types and levels of problems, rather than the coverage (which is outlined in the course calendar). Students are responsible for all sections and topics (in the textbook and class handouts) that are not explicitly excluded in the study guide that follows the sample exam, even if the material was not covered in class lectures.

Sample Midterm Exam (105 minutes)

Problem 1 [15 points] Defining concepts and terms. Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [3 points each]: Manchester carry chain; Multiplier recoding; *ulp*; Conditional-sum adder; Parallel prefix graph

Problem 2 [10 points] Number representation. Show that flipping (complementing) the sign bit of k -bit numbers in 2's-complement format results in biased representation and determine the bias amount that characterizes this new representation.

Problem 3 [20 points] Basic design concepts. Draw diagrams showing each of the following. No explanation is necessary; the diagrams should be self-explanatory.

a. How an ordinary binary adder can be augmented to perform addition or subtraction of 2's-complement numbers under the control of an add/sub signal (0 means "add", 1 means "subtract").

b. How 2-bits-at-a-time or radix-4 sequential multiplication might be performed at high speed without Booth's recoding and without precomputing 3 times the multiplicand.

Problem 4 [15 points] Carry-skip addition.

a. Show that the optimal block width b in a fixed-block carry-skip adder is proportional to the square root of the word width k . [10 points]

b. Briefly discuss why carry-skip adders are of interest at all, given that faster logarithmic-time adders are available. [5 points]

Problem 5 [15 points] Multioperand addition. The following describes a multioperand addition process in tabular form:

```

0 0 8 8 8 8 8 8 8 8
0 2 6 6 6 6 6 6 6 4
0 4 4 4 4 4 4 4 3 2
1 3 3 3 3 3 3 2 1
2 2 2 2 2 2 2 1 1

```

a. Explain the process described by this table. [5 points]

b. In the hardware implementation implied by the table, what component types are used and how many of each? Be as precise as possible in specifying the components used. [10 points]

Problem 6 [25 points] Two's-complement multiplication.

a. Represent $x = 3$, $y = -3$, and $z = 5$ as 4-bit 2's-complement numbers. [5 points]

b. Using the right-shift algorithm, perform x times z , using the representations of part a, to get the 8-bit product $p = 15$. [10 points]

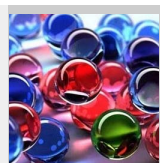
c. Using the left-shift algorithm, perform y times z , to get the 8-bit product $p' = -15$. [10 points]

Midterm Exam Study Guide

The following textbook sections are excluded from the midterm exam: 3.4-3.6, 4.4-4.6, 6.3, 7.2, 10.5

Research Paper and Presentation

Each student will review a subfield of computer arithmetic or do original research on a selected and approved topic. A list of research topics is provided below ("N/A" designates topics that are



not available for the current quarter); however, students should feel free to propose their own topics for approval. A publishable report earns an "A" for the course, regardless of homework and midterm grades. See the course calendar for research milestones and due dates. Consult [Research Paper Guidelines](#) for formatting tips.

Topics for Part I of the Textbook: Number Representation

01. Implementation of Arithmetic Operations in Mechanical Calculators (**N/A**)
02. The Need for, and Practicality of, Decimal Computer Arithmetic in Hardware (**N/A**)
03. Practical Implementations of Ternary Computer Arithmetic (**N/A**)
04. A Comparison of Carry-Save and Borrow-Save Number Representation Systems and Arithmetic (**N/A**)
05. Modulo- (2^a+1) Number Representations and Arithmetic (Assigned to: **TBD**)
 H. T. Vergos and C. Efstathiou, "Efficient Modulo $2^n + 1$ Adder Architectures," *Integration, the VLSI J.*, Vol. 42, pp. 149-157, 2009.
 G. Jaberipur and B. Parhami, "Unified Approach to the Design of Modulo- $(2^n \pm 1)$ Adders Based on Signed-LSB Representation of Residues," *Proc. 19th IEEE Int'l Symp. Computer Arithmetic*, 8-10 June 2009, to appear. [Preprint available via B. Parhami's publications Web page.]
06. Number Representation with Discrete Logarithms (Assigned to: **S. Joshi**)
 A. Fit-Florea, L. Li, M. A. Thornton, and D. W. Matula, "A Discrete Logarithm Number System for Integer Arithmetic Modulo 2^k : Algorithms and Lookup Structures," *IEEE Trans. Computers*, Vol. 58, No. 2, pp. 163-174, February 2009.

Topics for Part II of the Textbook: Addition/Subtraction

07. Variable-Block Carry-Lookahead Adders (Assigned to: **TBD**)
 V. Kantabutra, "A Recursive Carry-Lookahead/Carry-Select Hybrid Adder," *IEEE Trans. Computers*, Vol. 43, No. 12, pp. 1495-1499, December 1993.
08. Parallel-Prefix Ling Adders (Assigned to: **A. Ghofrani**)
 N. Burgess, "Implementation of Recursive Ling Adders in CMOS VLSI," *Proc. 43rd Asilomar Conf. Signals, Systems, and Computers*, November 2009, pp. 1777-1781.
09. Design of Optimal Adders with Input Timing Profile (**N/A**)
10. Saturating Two-Operand and Multioperand Adders (**N/A**)
11. Saturating Parallel Counters and Compressors (**N/A**)
12. Nonbinary Parallel Counters: The Ternary Example (Assigned to: **TBD**)
 M. De and B. P. Sinha, "Fast Parallel Algorithm for Ternary Multiplication Using Multivalued 1^2L Technology," *IEEE Trans. Computers*, Vol. 43, No. 5, pp. 603-607, May 1994.
13. Implementation of Parallel Counters by Means of Sorting Networks (**N/A**)
14. Counting Networks: Design Methods and Applications (**N/A**)

Topics for Part III of the Textbook: Multiplication

15. Trade-offs in Compensation Methods for Truncated Multipliers (Assigned to: **TBD**)
 N. Petra, D. De Caro, V. Garofalo, E. Napoli, and A. G. M. Strollo, "Truncated Binary Multipliers with Variable Correction and Minimum Mean Square Error," *IEEE Trans. Circuits and Systems I*, Vol. 57, No. 6, pp. 1312-

1325, June 2010.

16. Truncated Squarers and Cubers (Assigned to: K. Cox)

E. G. Walters, M. J. Schulte, and M. G. Arnold, "Truncated Squarers with Constant and Variable Correction," *Advanced Signal Processing Algorithms, Architectures, and Implementations XIV* (Proc. SPIE Conf. 5559), 2004, pp. 40-50.

17. Multimode Multiplication and Squaring Circuits (Assigned to: TBD)

K. E. Wires, M. J. Schulte, L. P. Marquette, and P. I. Balzola, "Combined Unsigned and Two's Complement Squarers," *Proc. 33rd Asilomar Conf. Signals Systems and Computers*, 1999, pp. 1215-1219.

18. Design of Cubing Circuits (N/A)

19. Generalized Recursive Multipliers Built of Possibly Nonsquare Modules (N/A)

20. Merged Arithmetic: The Case of Add-Multiply-Add Circuits (Assigned to: S. Kelgeri)

E. Hakkennes and S. Vassiliadis, "Multimedia Execution Hardware Accelerator," *J. VLSI Signal Processing*, Vol. 28, No. 3, pp. 221-234, July 2001.

21. A Comparison of Hardware Multipliers Used in Microprocessors (Assigned to: H. Sharma)

G. Colon-Bonet and P. Winterrowd, "Multiplier Evolution: A Family of Multiplier VLSI Implementations," *Computer J.*, Vol. 51, No. 5, pp. 585-594, 2008.

22. A Survey of Multiplier Circuits in Digital Signal Processors (Assigned to: TBD)

J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of Low-Error Fixed-Width Multipliers for DSP Applications," *IEEE Trans. Circuits and Systems II*, Vol. 46, pp. 836-842, June 1999.

S. J. Jou, M.-H. Tsai, and Y.-L. Tsao, "Low-Error Reduced-Width Booth Multipliers for DSP Applications," *IEEE Trans. Circuits and Systems I*, Vol. 50, No. 11, pp. 1470-1474, November 2003.

Topics for Part IV of the Textbook: Division

23. Radix-16 SRT Division: Algorithm and Implementations (Assigned to: TBD)

[Intel's] New Radix-16 Divider

24. A Survey of the Applications of Reciprocal and Square-Rooting (N/A)

25. Combinational Circuits for Fast Approximate Reciprocal (Assigned to: TBD)

P.-M. Seidel, "High-Speed Redundant Reciprocal Approximation," *Integration, The VLSI Journal*, Vol. 28, No. 1, pp. 1-12, September 1999.

26. On-the-Fly Conversion of Redundant Quotients into Nonredundant Form (N/A)

27. Practical Hardware Implementation of Montgomery Modular Multiplication (N/A)

27a. Convergence Division with Faster-than-Quadratic Convergence (Assigned: TBD)

I. Kong and E. E. Swartzlander, "A Goldschmidt Division Method with Faster than Quadratic Convergence," *IEEE Trans. VLSI Systems*, Vol. 19, No. 4, pp. 696-700, April 2011.

Topics for Part V of the Textbook: Real Arithmetic

28. History of Floating-Point Number Representation Formats and Associated Standards (N/A)

29. Level-Index Number Representation and Arithmetic (N/A)

30. Sign/Logarithmic Arithmetic and the European Logarithmic Microprocessor (Assigned to: TBD)

J. N. Coleman, et al., "The European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 532-546, April 2008.

J. N. Coleman, E. I. Chester, C. I. Softley, and J. Kadlec, "Arithmetic on the European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 49, No. 7, pp. 702-715, July 2000.

31. Residue Logarithmic Number Representation and Arithmetic (N/A)**32. Accurate Summation of Sets of Floating-Point Numbers (Assigned to: TBD)**

A. Eisinger and G. Fedele, "Accurate Floating-Point Summation: A New Approach," *Applied Mathematics and Computation*, Vol. 189, pp. 410-424, 2007.

T. Ogita, S. M. Rump, and S. Oishi, "Accurate Sum and Dot Product," *SIAM J. Scientific Computing*, Vol. 26, No. 6, pp. 1955-1988, 2005.

33. Multiprecision Arithmetic on Media Processors (N/A)**Topics for Part VI of the Textbook: Function Evaluation****34. Combinational Circuits for Fast Approximate Square-Rooting (N/A)****35. Cube Roots: Hardware Algorithms and Applications (Assigned to: TBD)**

A. Pineiro, J. D. Bruguera, F. Lamberti, and P. Montuschi, "A Radix-2 Digit-by-Digit Architecture for Cube Root," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 562-566, April 2008.

Cube-Roots via Newton-Raphson Method**36. Argument Reduction for Faster, More Accurate Function Evaluation (Assigned to: TBD)**

S. Boldo, M. Daumas, and R.-C. Li, "Formally Verified Argument Reduction with a Fused Multiply-Add," *IEEE Trans. Computers I*, Vol. 58, No. 8, pp. 1139-1145, August 2009.

N. Brisebarre, et al., "A New Range-Reduction Algorithm," *IEEE Trans. Computers*, Vol. 54, No. 3, pp. 331-339, March 2005.

37. Function Evaluation by Piecewise Linear Approximation (Assigned to: TBD)

N. Takagi, "Powering by a Table Look-Up and A Multiplication with Operand Modification," *IEEE Trans. Computers*, Vol. 47, No. 11, pp. 1216-1222, Nov. 1998.

O. Gustafsson and K. Johanson, "Multiplierless Piecewise Linear Approximation of Elementary Functions," *Proc. 40th Asilomar Conf. Signals, Systems, and Computers*, October 2006.

38. Smaller Lookup Tables by Exploiting Symmetry and Nonuniform Segmentation (Assigned to: TBD)

D.-U Lee, R. C. C. Cheung, W. Luk, and J. D. Villasenor, "Hierarchical Segmentation for Hardware Function Evaluation," *IEEE Trans. VLSI Systems*, Vol. 17, No. 1, pp. 103-116, January 2009.

T. Sasao, S. Nagayama, and J. T. Butler, "Numerical Function Generators Using LUT Cascades," *IEEE Trans. Computers*, Vol. 56, No. 6, pp. 826-838, June 2007.

Topics for Part VII of the Textbook: Implementation Topics**39. Pipelined Arithmetic in Vector Supercomputers (N/A)****40. Online or Digit-Pipelined Arithmetic with Carry-Save Operands (N/A)****41. Low-Power Full-Adder Cells and Their Applications (Assigned to: M. Mapara)**

K. Navi, et al., "A Novel Low-Power Full-Adder Cell for Low Voltage," *Integration, the VLSI J.*, Vol. 42, No. 4, pp. 457-467, September 2009.

M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," *IEEE Trans. VLSI Systems*, Vol. 19, No. 4, pp. 718-721, April 2011.

42. Low-Power Design Techniques for Multipliers (Assigned to: TBD)

I. S. Abu-Khater, A. Bellaouar, and M. I. Elmasry, "Circuit Techniques for CMOS Low-Power High-Performance Multipliers," *IEEE J. Solid-State Circuits*, Vol. 31, pp. 1535-1546, October 1996.

S. S. Mahant-Shetti, P. T. Balsara, and C. Lemonds, "High Performance Low Power Array Multiplier Using Temporal Tiling," *IEEE Trans. VLSI Systems*, Vol. 7, No. 1, pp. 121-124, March 1999.

43. Dedicated Hardware Multipliers on FPGA Chips (Assigned to: S. Masooman)**Using Embedded Multipliers in Spartan-3 FPGAs**

44. Design Methodologies for Implementing Wider Multipliers Using Embedded Multipliers in FPGAs (Assigned to: TBD)

S. Gao, D. Al-Khalili, and N. Chabini, "Efficient Realization of Large Size Two's Complement Multipliers Using Embedded Blocks in FPGAs," *Circuits, Systems, and Signal Processing*, Vol. 27, No. 5, pp. 713-731, October 2008.

J.-L. Beuchat and A. Tisserand, "Small Multiplier Based Multiplication and Division Operators for Virtex-II Devices," *Proc. 12th Int'l Conf. Field-Programmable Logic and Applications*, 2002, pp. 513-522.

45. Augmenting FPGAs for Faster Arithmetic Operations (Assigned to: TBD)

H. Parandeh-Afshar, A. K. Verma, P. Brisk, and P. Ienne, "Improving FPGA Performance for Carry-Save Arithmetic," *IEEE Trans. VLSI Systems*, Vol. 18, No. 4, pp. 578-590, April 2010.

General Research Topics Spanning Multiple Parts**46. A Survey of Arithmetic Circuits in Electronic Scientific Calculators (Assigned to: TBD)**

References TBD.

47. Arithmetic in Early Supercomputers: IBM System/360 Model 91 and CDC 6600 (N/A)**48. Arithmetic and Energy Economy Provisions in IBM Blue Gene/L Parallel Supercomputer (Assigned to: TBD)**

J. Lorenz, S. Kral, F. Franchetti, and C.W. Ueberhuber, "Vectorization Techniques for the Blue Gene/L Double FPU," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 437-446, March/May 2005.

S. Chatterjee, et al., "Design and Exploitation of a High-Performance SIMD Floating-Point Unit for Blue Gene/L," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 377-391, March/May 2005.

49. Implementation of Arithmetic Operations in Graphics Processors (Assigned to: M. Lastras)

D. De Caro, N. Petra, and A. G. M. Strollo, "High-Performance Special Function Unit for Programmable 3-D Graphic Processors," *IEEE Trans. Circuits and Systems I*, Vol. 56, No. 9, pp. 1968-1978, September 2009.

D. Blythe, "Rise of the Graphics Processor," *Proc. IEEE*, Vol. 96, No. 5, pp. 761-778, May 2008.

50. Number Crunching for Computer Games: History and Techniques (N/A)**51. Arithmetic Operations for Elliptic Curve Cryptography (Assigned to: TBD)**

C. K. Koc (ed.), *Cryptographic Engineering*, Springer, 2009.

S. Kumar, *Elliptic Curve Cryptography for Constrained Devices*, VDM Verlag, 2008.

J. Solinas, "Generalized Mersenne numbers," Tech. Report CORR 99-39, Dept. C&O, U. Waterloo, 1999.

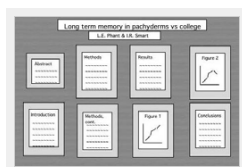
52. Implementation of Ultrahigh-Precision Arithmetic on Parallel Computers (Assigned to: TBD)

D. Takahashi, "Parallel Implementation of Multiple-Precision Arithmetic and 2,576,980,370,000 Decimal Digits of Pi Calculation," *Parallel Computing*, Vol. 36, No. 8, pp. 439-448, August 2010.

53. A Comparison of Synchronous and Asynchronous Arithmetic Circuits (N/A)**54. Implementing Arithmetic Operations with Neuronlike Hardware Elements (N/A)****55. Computer Arithmetic with Emerging Technologies (Assigned to: V. Shivakumar)**

G. Bourianoff, "The Future of Nanocomputing," *IEEE Computer*, Vol. 36, No. 8, pp. 44-53, August 2003.

Y. Brun, "Arithmetic Computation in the Tile Assembly Model: Addition and Multiplication," *Theoretical Computer Science*, Vol. 378, No. 1, pp. 17-31, June 2007.

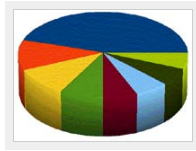
Poster Presentation Tips

Here are some guidelines for preparing your research poster. The idea of the poster is to present your research results and conclusions thus far, get oral feedback during the session from the instructor and your peers, and to provide the instructor with something to comment on before your final report is due. Please send a PDF copy of the poster via e-mail by midnight on the poster presentation day.

Posters prepared for conferences must be colorful and eye-catching, as they are typically competing with

dozens of other posters for the attendees' attention. Here is an [example of a conference poster](#). Such posters are often mounted on a colored cardboard base, even if the pages themselves are standard PowerPoint slides. In our case, you should aim for a "plain" poster (loose sheets, to be taped to the wall in our classroom) that conveys your message in a simple and direct way. Eight to 10 pages, each resembling a PowerPoint slide, would be an appropriate goal. You can organize the pages into 2 x 4 (2 columns, 4 rows), 2 x 5, or 3 x 3 array on the wall. The top two of these might contain the project title, your name, course name and number, and a very short (50-word) abstract. The final two can perhaps contain your conclusions and directions for further work (including work that does not appear in the poster, but will be included in your research report). The rest will contain brief description of ideas, with emphasis on diagrams, graphs, tables, and the like, rather than text which is very difficult to absorb for a visitor in a very limited time span.

Grade Statistics



Homework grades are in the [0, 4] range; other grades are in percent.

HW1 grades: Range = [2.0, 4.0], Mean = 3.0, SD = 0.6, Median = 3.0

HW2 grades: Range = [3.3, 4.3], Mean = 3.9, SD = 0.3, Median = 4.0

HW3 grades: Range = [2.0, 4.3], Mean = 3.1, SD = 0.9, Median = 3.0

HW4 grades: Range = [2.0, 4.0], Mean = 2.8, SD = 0.8, Median = 3.0

Midterm grades: Range = [44, 96], Mean = 74, SD = 19, Median = 83

Research & presentation grades: Range = [70, 95], Mean = 76, SD = 9, Median = 75

References



Primary textbook (required):

Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, Oxford, 2nd ed., 2010.

Verilog descriptions of arithmetic circuits (recommended):

This course does not involve a lab component or implementation projects. For those interested in pursuing practical circuit implementations, the following book may be useful:

Cavanagh, *Computer Arithmetic and Verilog HDL Fundamentals*, CRC Press, 2010.

Other useful books (not required):

Ercegovac/Lang, *Digital Arithmetic*, Morgan Kaufmann, 2004 (QA76.9.C62E73)

Koren, *Computer Arithmetic Algorithms*, 2nd ed., A K Peters, 2002 (QA76.9.C62K67)

Swartzlander, *Computer Arithmetic*, vols. 1-2, IEEE Computer Society Press, 1990 (QA76.6.C633)

Deschamps/Bioul/Sutter, *Synthesis of Arithmetic Circuits: ...*, Wiley, 2006 (TK7895.A65D47)

Omondi, *Computer Arithmetic Systems: ...*, Prentice-Hall, 1994 (QA76.9.C62O46)

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Waser/Flynn, *Intro. Arithmetic for Digital Systems Designers*, HR&W, 1982 (TK7895.A65W37.1982)

Knuth, *The Art of Computer Programming: Seminumerical Algorithms*, Wiley, 1981 (QA76.6.K64 vol 2)

Kulisich/Miranker, *Computer Arithmetic in Theory and Practice*, Academic Press, 1981 (QA162.K84)

Research resources:

Proc. IEEE Symp. Computer Arithmetic, 1969, 72, 75 78, 81 and subsequent odd years; ARITH-20, July 2011

On-line proceedings for IEEE Symp. Computer Arithmetic, 1969-2009

IEEE Trans. Computers, particularly special issues or sections on computer arithmetic (8/70, 6/73, 7/77, 4/83, 8/90, 8/92, 8/94, 7/98, 7/00, 3/05, 2/09, 2/11)

UCSB library's electronic journals, collections, and other resources

UCSB library's research guide in ECE

Miscellaneous Information

Motivation: Computer arithmetic is a subfield of digital computer organization. It deals with the hardware realization of arithmetic functions to support various computer architectures as well as with arithmetic algorithms for firmware/software implementation. A major thrust of digital computer arithmetic is the design of hardware algorithms and circuits to enhance the speed of various numeric operations. Thus much of what is presented in this course complements the architectural and algorithmic speedup techniques covered as part of the advanced computer architecture (ECE 254A/B/C) sequence.

Catalog entry: 252B. Computer Arithmetic. (4) PARHAMI. *Prerequisites: ECE 152A-B. Lecture, 4 hours.* Standard and unconventional number representations. Design of fast two-operand and multioperand adders. High-speed multiplication and division algorithms. Floating-point numbers, algorithms, and errors. Hardware algorithms for function evaluation. Pipelined, digit-serial and fault-tolerant arithmetic processors.

History: Professor Parhami took over the teaching of ECE 252B from the late Dr. James Howard in the winter quarter of 1989. By covering sequential machines, computer arithmetic, and advanced microprocessor-based design, the graduate course sequence ECE 252A/B/C was meant to provide a firm foundation in the theories and techniques of advanced digital design. During the first few offerings of ECE 252B, Professor Parhami gradually modified the content to increase both its coverage and research orientation (ECE 252A and 252C later underwent similar transformations by Professor Kwang-Ting Cheng and Professor Parhami, respectively). In 2000, based on a decade of experience in teaching this course, Professor Parhami published a graduate-level textbook, *Computer Arithmetic: Algorithms and Hardware Designs* (Oxford Univ. Press), which is being used at many universities worldwide. The 2nd edition of this textbook appeared in 2010.

[Offering of ECE 252B in spring 2010 \(PDF file\)](#)

[Offering of ECE 252B in spring 2009 \(PDF file\)](#)

[Offerings of ECE 252B from 2000 to 2008 \(PDF file\)](#)