Spiking Neuromorphic Networks with Metal-Oxide Memristors

M. Prezioso[1*], Y. Zhong[1,2], D. Gavrilov[3], F. Merrikh-Bayat[1], B. Hoskins[1], G. Adam[1], K. Likharev[3†], and D. Strukov[1‡]

[1] UC Santa Barbara, Santa Barbara, CA 93106-9560, U.S.A.
[2] Huazhong University of Science and Technology, Wuhan 430074, China
[3] Stony Brook University, Stony Brook, NY 11794-3800, U.S.A.
Email: *mprezioso@ece.ucsb.edu, †konstantin.likarev@stonybrook.edu, ‡strukov@ece.ucsb.edu.

***Abstract* – This is a brief review of our recent work on memristor-based spiking neuromorphic networks. We first describe the recent experimental demonstration of several most biology-plausible spike-time-dependent plasticity (STDP) windows in integrated metal-oxide memristors and, for the first time, the observed self-adaptive STDP, which may be crucial for spiking neural network applications. We then discuss recent theoretical work in which an analytical, data-verified STDP model was used to simulate operation of a spiking classifier of spatial-temporal patterns, and the capacity-to-fidelity tradeoff and noise immunity of spiking spatial-temporal associative memories with local and global recording was evaluated.**

Keywords— Spiking neural networks; Memristor; CrossNets; Spike-time-dependent plasticity; Spatial-temporal associative memories

I. Introduction

Most studies of neuromorphic networks and their hardware implementations have been focused on the firing-rate models [1, 2], in which neuron spiking activity is represented only by its average rate. However, there is a general consensus that an explicit modeling of spiking activity increases the signal information contents [3-5], improves the energy efficiency [6, 7], and enables coordinated processing of spatial and temporal information [8, 9]. This is especially important in large-scale networks, which may be implemented in hardware as CrossNets [10] based on hybrid CMOS/memristor crossbar circuits [11] (Fig. 1). A necessary step in the adaptive spiking network development is an efficient implementation of STDP [12], i.e. of the synaptic weight (memristor conductance) change ΔG, properly dependent on the time interval Δt between the pre- and post-synaptic spikes (Fig. 2).

II. Experimental Work

We have recently experimentally demonstrated the implementation of several most common STDP "windows" $\Delta G(\Delta t)$, using Pt/Ti/TiO_{2-x}/Al_2O_3/Pt memristors [13, 14] integrated in crossbar circuits. Fig. 3 shows the main characteristics of such devices. (See Ref. [15] for their fabrication details and other test results.) For the STDP demonstration, memristor's low-voltage conductance G, which represents the synaptic weight, was first set to some initial value G_0 [16]. Then pre- and post-synaptic voltage pulses of appropriate waveforms [17] (Fig. 4a-c) were applied to the memristor with certain delay Δt between the pulses, and the resulting conductance change was measured. The experiment has been performed for many different values of Δt, and repeated several times for each Δt, every time resetting the device to G_0.

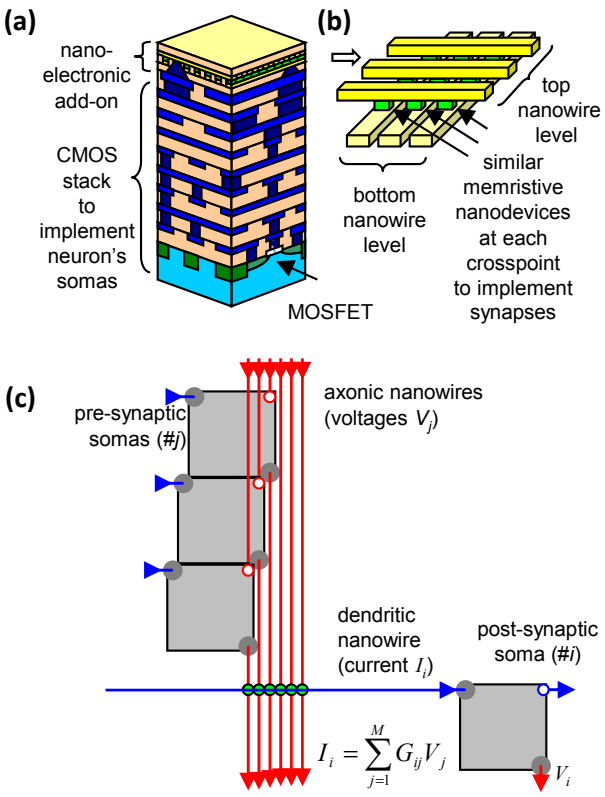


Fig. 1. Hybrid neuromorphic circuits ("CrossNets") [10, 11]: (a) the general idea of a hybrid CMOS/memristor circuit, (b) its crossbar-based add-on layer, and (c) the topology of the simplest (feedforward) CrossNet. On panel (c), the nanowires mimicking biological axons are shown red, while those playing the role of dendrites, are shown blue, even though they may be physically similar. For clarity, only the synapses (memristors) that contribute to one post-synaptic signal I_i, are shown (with green circles).

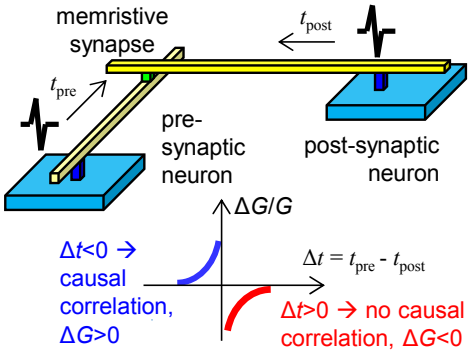


Fig. 2. General idea of implementation of spike-time dependent plasticity (STDP) in a CrossNet, and one of the most common STDP windows, corresponding to Hebbian adaptation.

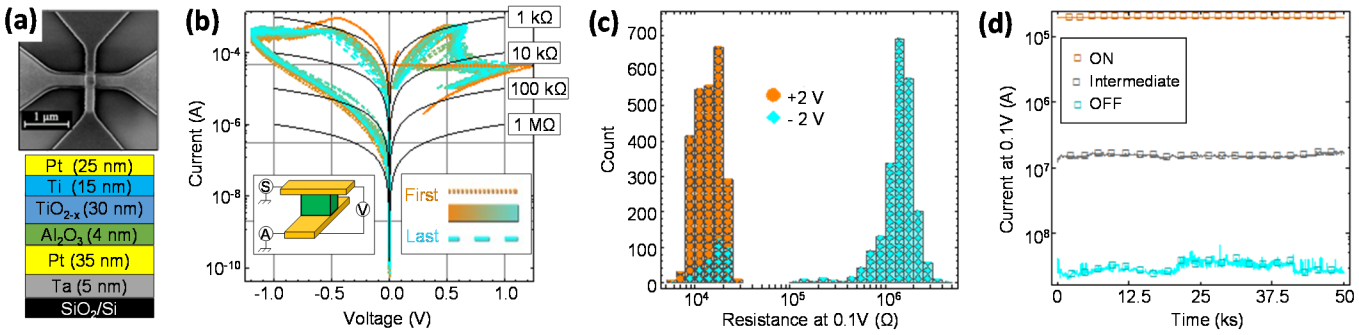


Fig. 3. Pt/Ti/TiO_{2-x}/Al_2O_3/Pt memristors [15]: (a) a single device micrograph and stack structure; (b) the typical switching and electroforming behavior of a single device; (c) its switching endurance statistics (>5,000 cycles) under a stream of ±2 V, 500-μs pulses, and (d) the retention of three different initial states at 350 K. To highlight the long-term retention trends, larger markers on panel (d) highlight the results of every 1,000th measurement.

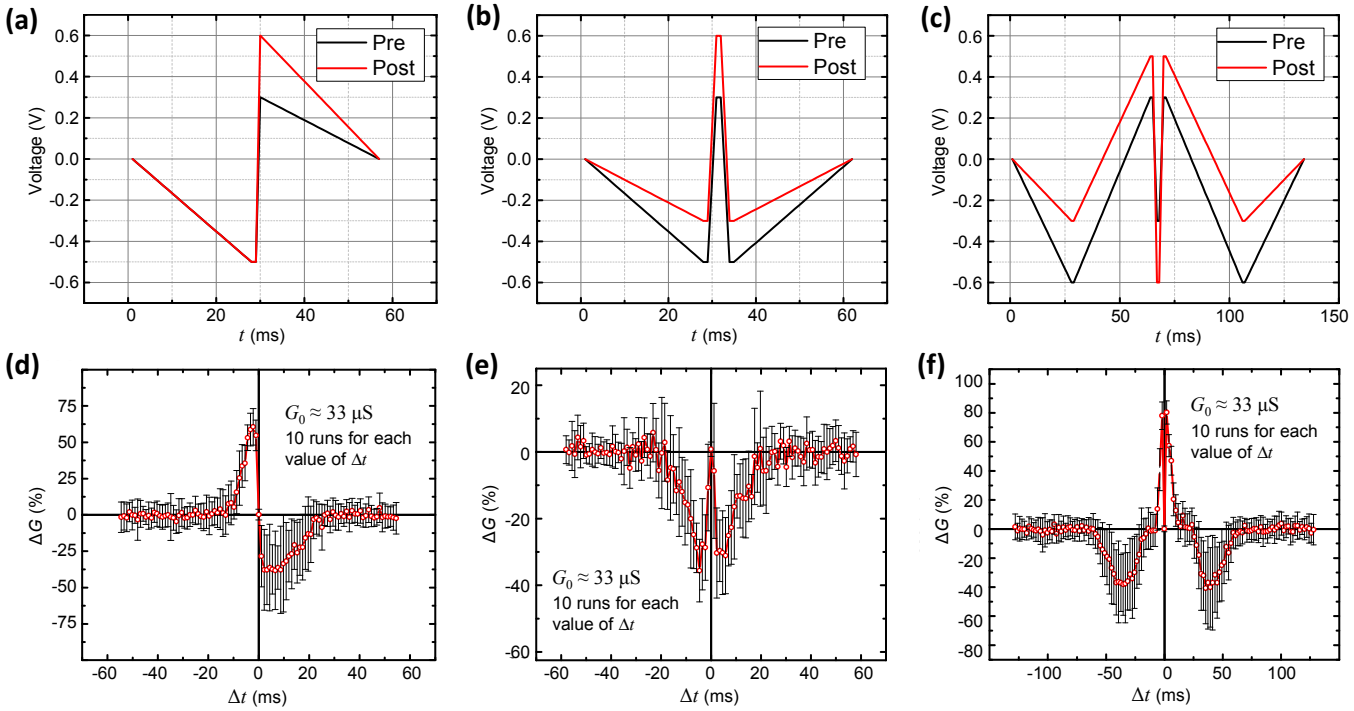


Fig. 4. Experimental demonstration of the STDP windows similar to those observed in biology: in layer 5 (the left column) and layer 4 (the middle column) of the neocortex, and GABAergic synapses (the right column) [18]. (a-c) The waveforms of pre-synaptic $V_{pre}(t)$ and post-synaptic $V_{post}(t)$ pulses used for adaptation. (d-f) The experimentally measured STDP "windows", i.e. the memristor conductance changes as functions of the relative delay Δt between the pre- and post-synaptic pulses. The red points and error bars show, respectively, the averages and the standard deviations of the results for each argument Δt.

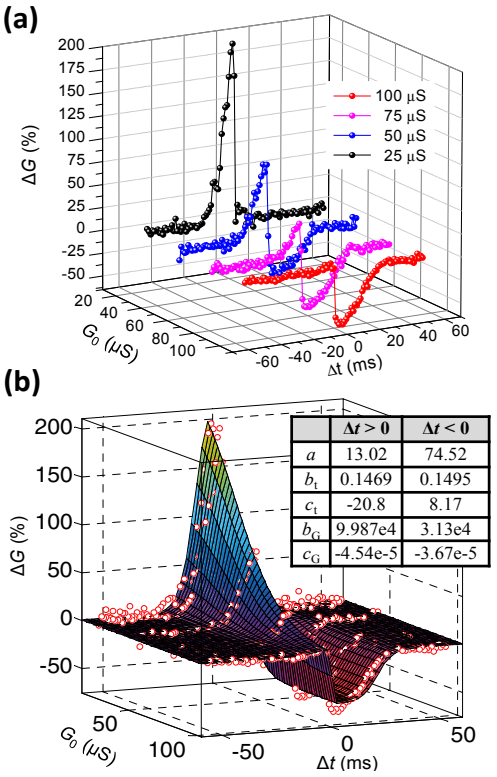
The resulting STDP windows (Fig. 4d-f) can be explained semi-quantitatively by analyzing the applied voltages, and the fact that the shape of STDP strongly depends on G_0, with conductance changes vanishing when G_0 is close to its extreme values (Fig. 5a), which is natural considering the saturation in switching dynamics [14]. Such state-dependent STDP behavior was fitted with a product of functions of Δt and G_0 for one of the considered STDP windows (Fig. 5b) using the following equations:

$$\Delta G = \Lambda_G \Lambda_t, \qquad (1)$$

$$\Lambda_G \equiv \begin{cases} 1+\tanh\left[b_G^+\left(G_0+c_G^+\right)\right], \Delta t > 0, \\ 1-\tanh\left[b_G^-\left(G_0+c_G^-\right)\right], \Delta t < 0. \end{cases} \qquad (2)$$

$$\Lambda_t \equiv \begin{cases} a^+\left\{\tanh\left[b_t^+\left(\Delta t + c_t^+\right)\right]-1\right\}, \Delta t > 0, \\ a^-\left\{\tanh\left[b_t^-\left(\Delta t + c_t^-\right)\right]+1\right\}, \Delta t < 0, \end{cases} \qquad (3)$$

where $a^{\pm}$, $b_t^{\pm}$, and $b_G^{\pm}$ are fitting parameters – see Fig. 5b.



	Δt > 0	Δt < 0
a	13.02	74.52
b_t	0.1469	0.1495
c_t	-20.8	8.17
b_G	9.987e4	3.13e4
c_G	-4.54e-5	-3.67e-5

Fig. 5. Modeling STDP [18]: (a) the experimentally measured window function (same as in Fig. 4d) for several initial conductance values, and (b) the results of its fitting with equations (1-3). The inset table in panel (b) shows the used fitting parameters.

III. Modeling of Spiking Networks

Using the derived model within a simulated generic spiking network, we have shown that the STDP window may automatically self-adapt to a virtually optimal shape, independent on its initial state [18].

In addition, we have adapted this STDP model to simulate a spiking network (Fig. 6a) performing classification of spatial-temporal patterns [19]. The network was trained by a teacher system, whose objective was to force the network to spike at the times when a specific pulse trains were applied to its inputs (Fig. 6c) [8] using the Remote Supervised Method ("ReSuMe") (Fig. 6b), which is formally described by the following equation:

$$\frac{dG}{dt} = S^{d}(t)\int_{0}^{\infty} W^{d}(x)S^{in}(t-x)dx - S^{o}(t)\int_{0}^{\infty} W^{o}(x)S^{in}(t-x)dx, \quad (4)$$

where $S^{d}(t)$, $W^{d}(t)$, and $W^{o}(t)$ are teacher, output (backward), and input spikes, respectively.

The network operation was tested, in particular, on a randomly generated 200-ms-long spike sequence with 3 Hz average firing rate and a specific teacher spike sequence with 20 Hz average firing rate (Fig. 6c), which was repeatedly applied to the input and teacher neurons. The optimized network's output converged to the desired value after about 15 training epochs, where one epoch corresponds to a 200 ms spike sequence (Fig. 6c-d). The classification performance was similar to the software-simulated one with ideal STDP windows, and was very robust with respect to various simulated variations and defects of the memristors (Fig. 6e).

We have also used numerical simulations to characterize the capacity-to-fidelity tradeoff of associative, asynchronous spatial-temporal memories (Fig. 7a) [3, 4, 20], which may record and then restore from noise, for example, B/W movies, with frames mapped on the CrossNet plane (Fig. 7b-c). The memories may be recorded using a local, STDP-plausible Hebb-like rule:

$$G_{ij} = G_0 f\left(\frac{1}{Pd^2}\sum_{p=1}^{P} b_i^{(p)} b_j^{(p+1)} - 1\right) \quad (5)$$

where index p numbers sequential patterns ("movie frames") to be recorded, P is their total number, binary numbers $b_i^{(p)}$ represent black and white pixels of the p^{th} frame, $d < 1$ is the "duty cycle" of the images, i.e. the average fraction of active pixels (with $b = 1$), while f (with $|f| \le 1$) is a function describing weight saturation. Alternatively, a global rule, which requires an external tutor, may be used for training. So far, the best results for the capacity (Fig. 7d) and noise contamination immunity (Fig. 7e) have been obtained with the global recording method, while the optimization of the local recording is still in progress.

IV. Summary

To conclude, we have experimentally demonstrated and modeled STDP adaptation of metal-oxide memristors, and verified its practicality via simulations of representative spiking network tasks, including recording/restoration and classification of spatial-temporal patterns. While this is not the first time the STDP has been demonstrated with metal-oxide memristors [21-24], our results are much less noisy, apparently because we fix the initial state G_0 explicitly for each window. A rather high tolerance of analog neuromorphic applications to memristor imperfections, the main impediment for applications of these devices in digital memory and logic circuits [14], indicates exciting prospects for memristor applications, in particular in spiking networks.

V. Acknowledgements

This work was supported by the AFOSR under the MURI grant FA9550-12-1-0038, by DARPA under HR0011-13-C-0051UPSIDE via BAE Systems, by the ARO under W15QKN-15-C-0008, and by China Scholarship Council. Useful discussions with L. Sengupta and X. Guo are gratefully acknowledged.

VI. References

[1] G. Indiveri *et al.*,"Neuromorphic silicon neuron circuits", *Frontiers in Neuroscience*, vol. 5, art. 73, 2011.

[2] J. Hasler and B. Marr, "Finding a roadmap to achieve large neuromorphic hardware systems", *Frontiers in Neuroscience*, vol.7, art. 118, 2013.

[3] W. Gerstner, R. Ritz, and J. L. van Hemmen, "Why spikes? Hebbian learning and retrieval of time-resolved excitation patterns", *Biological Cybernetics* vol. 69, pp. 503-515, 1993.

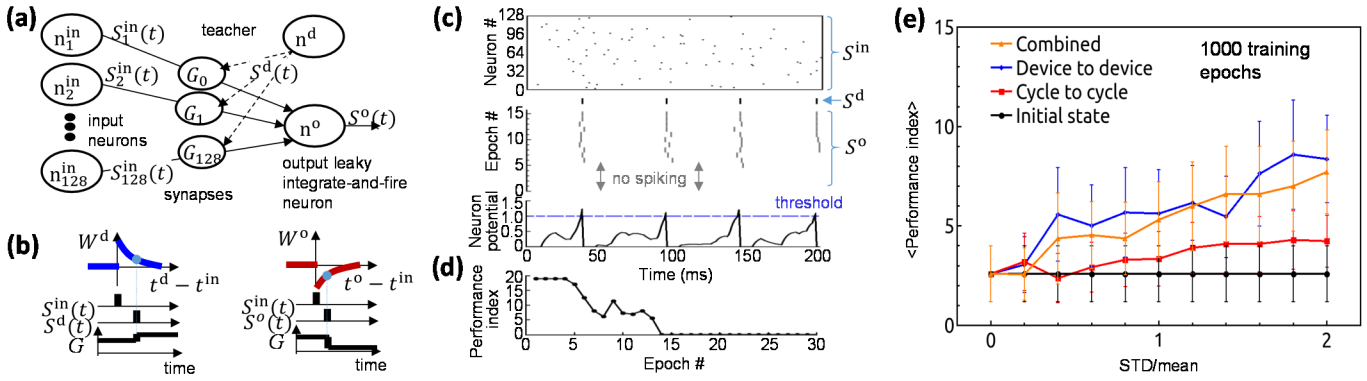


Fig. 6. Simulated spatial-temporal pattern classification by a spiking neural network at supervised training [19]: (a) the analyzed network, (b) the weight update using the ReSuMe algorithm [8], (c) a fragment of the set of input, output, and teaching spike trains and the corresponding potential of the output neuron, (d) the dynamics of the classification performance index [8], a measure of distance between the teaching and output spike trains, and (e) its sensitivity to variations in synapses and their initial states. On panel (e), error bars show one standard deviation (over a set of 10 independent runs). The variations have been modeled by adding Gaussian noise to the initial conductance and/or to each conductance update. Random variables are initialized before each run when modeling device-to-device and initial-state variations, and at every conductance update for the cycle-to-cycle variations.

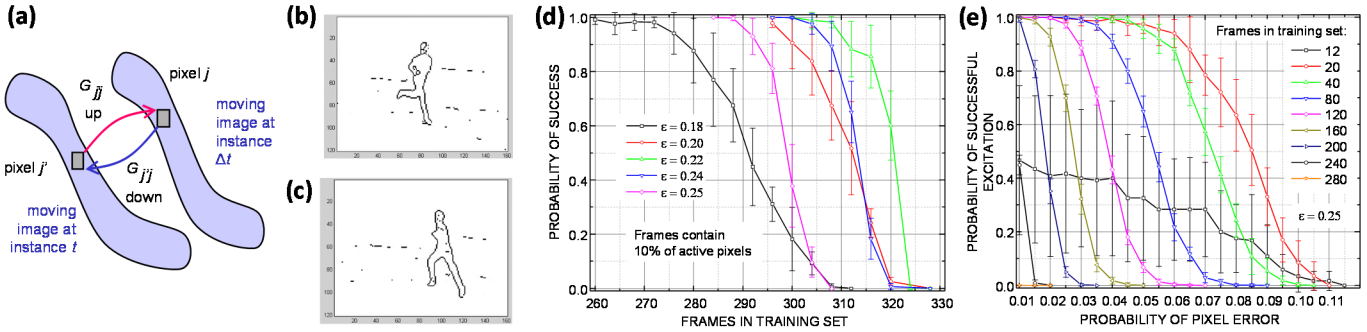


Fig. 7. Spiking spatial-temporal memory [20]. (a) The basic idea of the local recording rule (5): for each pair of sequential frames, conductances G_{ij} of all memristors leading from active pixels of a frame to those of the next frame are increased, while conductances G_{ji} of the synapses in the oppositely directed connections are decreased. (b)-(c) Two typical frames of the 4 movies used for testing in 120×160-cell arrays with ~7×10^8 synapses, (d)-(e) memory capacity simulation results for an array with (101×101) cells and connectivity $M = (21\times21 - 1)$, for global recording of random, uncorrelated patterns of B/W pixels: (d) the capacity-vs-fidelity tradeoff, for several values of the overshoot parameter ε, and (e) the noise immunity of the same network, for $\varepsilon = 0.25$.

[4] S. A. Wills, "Computation with spiking neurons", PhD Thesis, U. Cambridge, Sept. 2004.

[5] W. Maass, "Networks of spiking neurons: The third generation of neural network models", *Neural Networks*, vol. 10, pp. 1659-1671, 1997.

[6] P. Merolla *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface", *Science*, vol. 345, pp. 668-673, 2014.

[7] T. Pfeil *et al.*, "Six networks on a universal neuromorphic computing substrate", *Frontiers in Neuroscience,* vol. 7, art.11, 2013.

[8] T. Masquelier, R. Guyonneau, and S. J. Thorpe, "Spike timing dependent plasticity finds the start of repeating patterns in continuous spike trains", *PLOS One*, vol. 3(1), art. e1377, 2008.

[9] F. Ponulak and A. Kasinski, "Supervised learning in spiking neural networks with ReSuMe: Sequence learning, classification, and spike shifting", *Neural Computation*, vol. 22, pp. 467-510, 2010.

[10] K. Likharev, "CrossNets: Neuromorphic hybrid CMOS/nanoelectronic networks", *Science of Advanced Materials*, vol. 3, pp. 322-331, 2011.

[11] F. Merrikh Bayat *et al.*, "Memory technologies for neural networks", in: *Proceedings of IMW'15*, Monterey, CA, May 2015, pp. 1-4.

[12] H. Markram, J. Lubke, M. Frotscher, and B. Sakmann, "Regulation of synaptic efficacy by coincidence of postsynaptic APs and EPSPs", *Science*, vol. 275, pp. 213-215, 1997.

[13] H. Wong *et al.*, "Metal–oxide RRAM", *Proceedings of IEEE*, vol. 100, pp. 1951-1970, 2012.

[14] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing", *Nature Nanotechnology*, vol. 8, pp. 13-24, 2013.

[15] M. Prezioso *et al.*, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors", *Nature*, vol. 521, pp. 61-64, 2015.

[16] F. Alibart, L. Gao, B. D. Hoskins, and D. B. Strukov, "High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm", *Nanotechnology*, vol.23, art. 075201, 2012.

[17] C. Zamarreño-Ramos *et al.*, "On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex", *Frontiers in Neuroscience*, vol. 5, art. 26, 2011.

[18] M. Prezioso, F. Merrikh Bayat, B. Hoskins, K. Likharev, and D. Strukov, "Self-adaptive spike-time-dependent plasticity of metal-oxide memristors", *Scientific Reports*, vol. 6, art. 21331, 2016.

[19] Y. Zhong *et al.*, "Simulation of memristive spiking neural networks with experimentally-verified device plasticity models", in preparation, 2016.

[20] K. K. Likharev, "Spatial-temporal associative memory", report at DARPA's Cortical Processor Workshop, Arlington, VA, Sept. 2014.

[21] A. Subramaniam, K. D. Cantley, G. Bersuker, D. Gilmer, and E. M. Vogel, "Spike-timing-dependent plasticity using biologically realistic action potentials and low-temperature materials", *IEEE Transactions on Nanotechnology*, vol. 12, pp. 450-459, 2013.

[22] Z. Wang *et al.*, "Synaptic learning and memory functions achieved using Oxygen ion migration/diffusion in an amorphous InGaZnO memristor", *Advanced Functional Materials*, vol. 22, pp. 2759-2765, 2012.

[23] S. Mandal, A. El-Amin, K. Alexander, B. Rajendran, and R. Jha, "Novel synaptic memory device for neuromorphic computing", *Scientific Reports*, vol. 4, art. 5333, 2014.

[24] S. Saighi *et al.*, "Plasticity in memristive devices for spiking neural networks", *Frontiers in Neuroscience*, vol. 9, art. 51, 2015.