# 3-D Memristor Crossbars for Analog and Neuromorphic Computing Applications

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***Abstract*— We report a monolithically integrated 3-D metal-oxide memristor crossbar circuit suitable for analog, and in particular, neuromorphic computing applications. The demonstrated crossbar is based on Pt/$Al_2O_3$/$TiO_{2-x}$/TiN/Pt memristors and consists of a stack of two passive 10 × 10 crossbars with shared middle electrodes. The fabrication process has a low, less than 175 °C, temperature budget and includes a planarization step performed before the deposition of the second crossbar layer. These features greatly improve yield and uniformity of the crosspoint devices and allows for utilizing such a fabrication process for integration with CMOS circuits as well as for stacking of multiple crossbar layers. Furthermore, the integrated crosspoint memristors are optimized for analog computing applications allowing successful forming and switching of all 200 devices in the demonstrated crossbar circuit, and, most importantly, precise tuning of the devices' conductance values within the dynamic range of operation. We believe that the demonstrated work is an important milestone toward the implementation of analog artificial neural networks, specifically, those based on 3-D CMOL circuits.**

***Index Terms*— 3-D integrated circuits, analog processing circuits, memristors, nonvolatile memory.**

## I. Introduction

DUE to excellent scalability, compatibility with conventional semiconductor fabrication technology, and fast write and read speed combined with long retention, metal-oxide resistive switching devices [1] (also called metal-oxide memristors [2] or ReRAM [3]) are very promising emerging components for a variety of memory and computing applications [4], [5]. Successful demonstrations of digital memory and logic applications based on metal-oxide ReRAM are abundant in the literature [6]–[14]. However, one of the most exciting applications of such devices could be in neuromorphic computing [15]–[20] due to the potential for tuning the memory state, i.e., device conductance, with very high (<1%) precision [21]. Because of an ionic memory mechanism, analog memory functionality is sustained upon aggressive scaling [22], [23] making such devices ideal candidates for the implementation of artificial synapses, the most numerous elements of artificial neural networks [15], [24]. The potentially high integration density for artificial synapses and their tight integration with other elements of the circuit would eliminate costly OFF-chip communications and is crucial for low-energy operation of memristor-based artificial neural networks. An example of such a circuit is the CMOL (Cmos + MOLecular) [4]–[6], [15] concept, in which the CMOS subsystem implements neurons' soma functionality, while back-end-of-line-integrated passive memristive crossbar circuits with analog tuning capability mimic synapses' functionality and routing among neurons.

In 3-D CMOL, [25] the most advanced version of CMOL circuits, multiple crossbar layers are utilized to further increase the effective density of synapses and connectivity among neurons. Obviously, monolithic integration of multiple crossbar layers comes with additional fabrication challenges, while the analog tuning requirement enforces tighter margins on the permissible variations in the memristors. Though there have already been demonstrations of multilayer crossbar circuits, the primary target applications were digital memories [7], [9]–[13], [26]–[28] and typically, only very limited characterization statistics were reported. Statistics about the device behavior across the entire crossbar are needed to understand if the system shows the tight switching variations needed to successfully implement neuromorphic networks. The sidewall-integrated vertical memristive architecture allows for cost-effective multilevel functionality, but it has only been shown so far in small linear arrays [29], [30] not crossbars. Moreover, such an approach is not suitable for CMOL circuit integration and may not be readily scalable to large numbers of layers because of the required high aspect ratios during deposition [31] or even due to the low current drivability of the vertical selector [32].

A particular challenge for 3-D circuits is the presence of thermal effects that can play an important role during the fabrication and operation of multilayer systems [33], [34].

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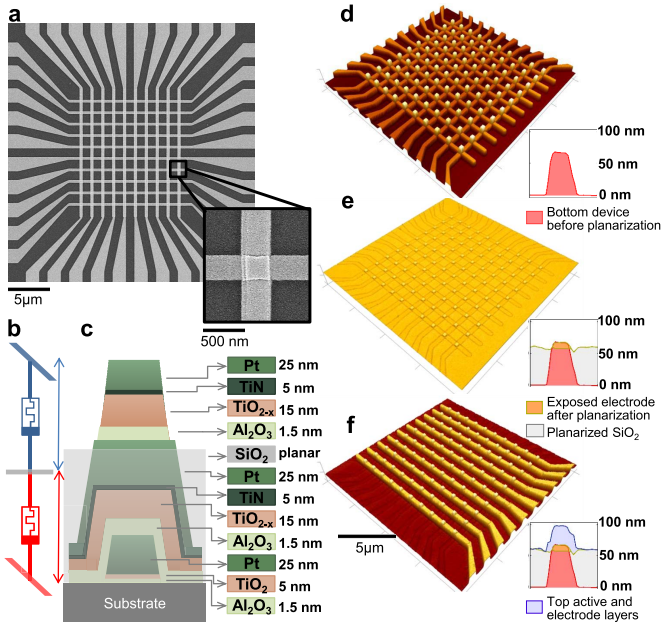


Fig. 1. Fabrication details. (a) Scanning electron microscopy top-view image of the fabricated circuit with a zoom on a stacked device to highlight the clean electrode edges. (b) Equivalent circuit for two memristors in the stacked configuration, in particular, highlighting that the middle electrode (gray) is shared between bottom (red) and top (blue) devices. (c) Cartoon of device's cross section showing the material layers and their corresponding thicknesses. AFM images and step heights of the crossbar devices during different stages of fabrication, in particular, showing (d) bottom crossbar, (e) planarization to reduce step height, and (f) top crossbar.

A low temperature budget is needed during fabrication in order to preserve the material properties of the already fabricated layers. The use of high temperatures during deposition or photoresist baking can lead to interlayer diffusion and decrease the control over the dopant concentration and nonstoichiometry. Additionally, the switching mechanism for the most practical metal-oxide memristors involves significant Joule heating. Maximum temperatures during the switching might be fairly high, exceeding 700 K [35]. This can cause disturbances in the state of a vertical neighbor if such devices are separated by a thin middle electrode from the device in question. A recent theoretical work [36] suggested that the thermal crosstalk in 3-D ReRAM stacks can deteriorate device performance and produce failures—a problem particularly severe during the power intensive reset step.

This paper reports the first 3-D monolithic back-end-of-line integration of two $TiO_{2-x}$-based passive crossbars for analog computing applications, which we believe is an important step toward energy-efficient neuromorphic circuits, in particular 3-D CMOL networks [15].

## II. Fabrication and Characterization

Two memristive crossbar circuits were monolithically integrated in a conventional configuration, with middle lines shared between the bottom and top crossbar circuits (Fig. 1). (This is in contrast to the recently demonstrated sidewall vertical integration approach [30]–[32].) Devices were fabricated on a Si wafer coated with 200-nm thermal $SiO_2$ and had ~350 nm × 350 nm feature sizes. Circuit fabrication involved four lithography steps using an ASML S500/300 DUV stepper with a 248-nm laser. A stack of nondevelopable antireflective coating (DUV-42P-6 from Brewer Science, spin speed 2500 rpm, bake 175 °C, thickness ~60 nm) and positive photoresist (UV210-0.3 from Dow, spin speed 2500 rpm, bake 135 °C, thickness ~300 nm) together with the AZ300MIF developer from Clariant was used for patterning. An $O_2$-based plasma (100 W, 300-mTorr pressure for 75 s) was then used to etch the nondevelopable antireflective coating and to clean any organic residue. An AJA ATC 2000-F sputter system with Ti, Al, and Pt targets and Ar, $O_2$, and $N_2$ gases was used to deposit in blanket the material stacks for the: 1) the bottom electrodes; 2) bottom active layer and middle electrodes; and 3) top active layer and top electrodes. $TiO_{2-x}$ with nonstoichiometry precisely controlled during the reactive dc sputtering deposition was used as an active layer for both crossbar circuits due to its excellent analog switching properties. The $Al_2O_3$ barrier layer, the $TiO_{2-x}$ active layer, and the TiN and Pt layers together with an $Al_2O_3$ hard mask layer (~25 nm) were deposited *in situ* without breaking the vacuum and then patterned using an Ar ion beam etching (IBE) in an Oxford Flexal system at 30-mA source current. The active layers have similar properties, since they were deposited in the same chamber conditions a few hours apart [Fig. 1(c)].

The particular reason for using Ar IBE for patterning the metal layers is that the structures with clean edges are crucial for multilayer stacking. "Rabbit ear" and other formations can easily appear during lift-off processes of sputtered films due to side-wall redeposition and they pose the risk of electrical shorts. In comparison with the previously used lift-off techniques [20], [37], [38], the IBE has the advantage of allowing *in situ* deposition of the stack and provide clean metal electrodes.

To control the shape of the electrode, we investigated three different Ar ion beam incident angles. Etching with no tilt (beam angle 0°) created an electrode with a 40.2° slope. When tilt was used, the electrode slope decreased to −22.8° for partial tilt (i.e., with no tilt initially and then milling at a 40° angle) and to 12.8° for purely tilted (40° angle). Partially tilted conditions were chosen, since they provided lower electrode slope while preserving the feature sizes. After IBE, the remaining traces of $Al_2O_3$ hard mask were removed in AZ300MIF developer, and the sample was cleaned thoroughly in solvents.

The top stack of active layer and metal was deposited only after a planarization step in order to minimize the risks of shorts and large variations due to the high step height, ~69 nm on average [Fig. 1(d)–(f)]. The first step in the planarization process was to deposit ~750 nm of $SiO_2$ in an advanced vacuum plasma-enhanced CVD Vision 310 system from Veeco at a temperature of 175 °C using 600 sccm of $SiH_4$ as precursor and 1640 sccm of $O_2$. This $SiO_2$ layer was used with a dual purpose: as the sacrificial layer for planarization and as an isolation layer between the devices. In the second step, fast chemical mechanical polishing (CMP) using a Logitech Orbis system was used to achieve global planarization. The developed recipe (platen rotation 80 rpm

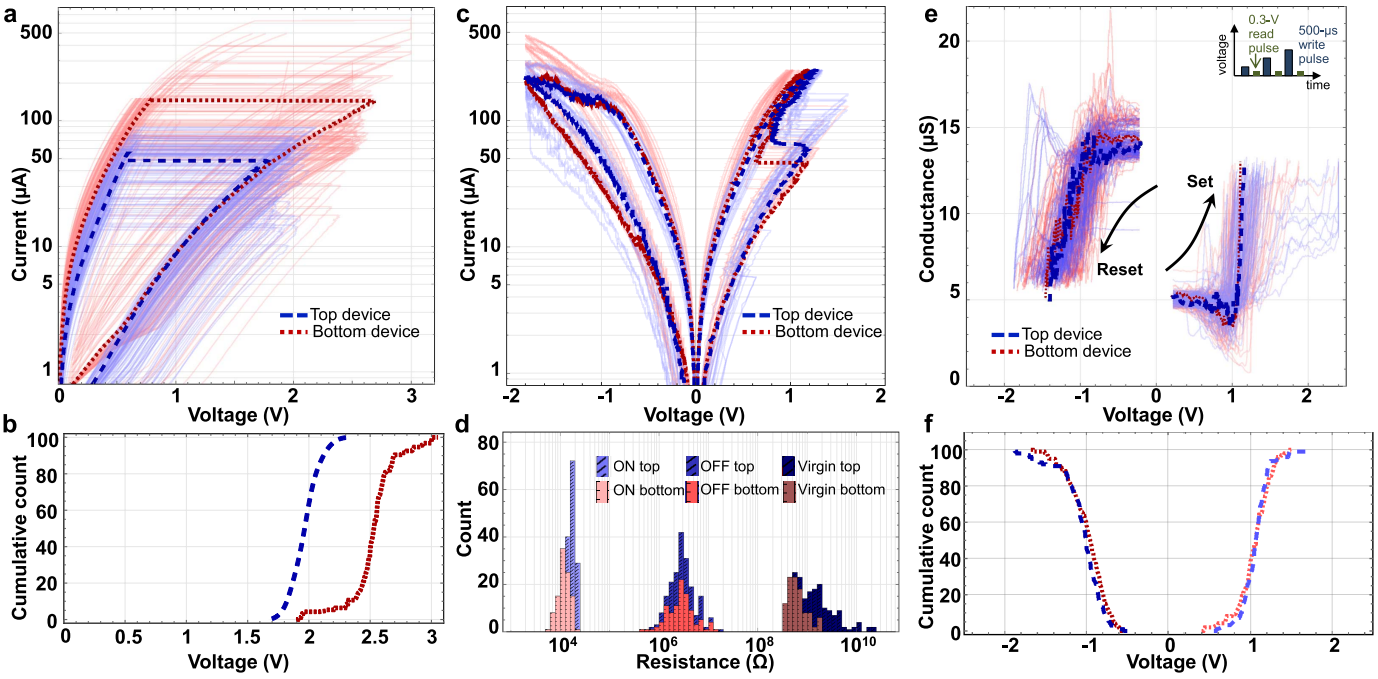


Fig. 2. Forming, switching, and tuning characteristics. (a) *I–V* curves for forming process for all devices with two representative curves being highlighted for comparison. Red dotted line: bottom device. Blue dashed line: top device. (b) Cumulative histogram counts of forming voltages, which are defined as the sum of all previous counts up to the current forming voltage. (c) *I–V*s for all 2 x 10 x 10 devices with two representative curves being highlighted for comparison. (Red dotted line: bottom device. Blue dashed line: top device.) obtained by applying quasi-dc current ramp 300 $\mu$A and reset voltage of –1.8 V. (d) Cumulative histogram for the devices' on- and off-state conductances, measured at 0.3 V, when using quasi-dc current ramp with 300 $\mu$A for set and quasi-dc voltage ramp with –2.4 V for reset transition. (e) Device conductance evolution, measured at 0.3 V, under applied write voltage ramps of opposite polarities. (f) Cumulative counts for the effective threshold voltages for set and reset transition for both bottom (red dotted line) and top crossbars (blue dashed line). All the devices in both layers were characterized. The average threshold set voltages for bottom and top layer were 1.04 and 1.06 V, respectively, with a corresponding standard deviations of 0.2 and 0.17 V. For the threshold reset voltage, the averages for bottom and top layer were –0.98 and –1.04 V, respectively, with a corresponding standard deviations of 0.22 and 0.25 V.

and slurry rate 50 sccm) etched ~450 nm of $SiO_2$ in 2 min and provided a planar surface with a good uniformity across the 4-in wafer. The middle electrode was partially exposed in a controlled fashion using dry etch and atomic force microscope (AFM) as explained further. We used short dry-etching steps in a $CHF_3$ atmosphere in a Panasonic E626I inductively coupled plasma chamber to remove the remaining $SiO_2$. AFM imaging with a Bruker ICON AFM in the tapping mode was used to test after each etching step if the middle electrode was exposed so that no extra etching steps would be required. This planarization technique had ~74% yield across the wafer, as 74 out of 100 crossbar dies had the middle electrode properly exposed and the remaining dies had the middle electrode still covered with $SiO_2$ due to CMP nonuniformities. The step of the exposed middle electrode varied slightly from die to die, with an average of 11.8 nm and a maximum of 24 nm. The top device layers were deposited using reactive sputtering and patterned with DUV lithography and Ar IBE similarly to the bottom ones. The top electrode was patterned a few nanometers wider, to ensure complete coverage of the exposed middle electrode. Finally, the pads of the bottom and middle electrodes were exposed through a $CHF_3$ etch of the sacrificial $SiO_2$, which was used for planarization. The photoresist was then stripped in the 1165 solvent (from Shipley Microposit) for 24 h at 80 °C. To facilitate the wireboding, the pads of the bottom and middle electrodes were filled with 15 nm of Cr and 450 nm of Au deposited using a four pocket electron beam evaporator from Sharon Vacuum Co.

All the electrical characterizations were performed at room temperature using an Agilent B1500A Semiconductor Device Parameter Analyzer and an Agilent B1530A Waveform Generator/Fast Measurement Unit together with a low-leakage Agilent E5250A Switch Matrix. The crossbar was wirebonded and mounted on a custom made board connected to the Agilent measurement tools. The setup was controlled through a computer via General Purpose Interface Bus (GPIB) and custom Visual C++ code. Three different modes of operation were utilized for crossbar circuit testing and characterization [39]. A "ground configuration" was used for a state read at 0.3 V, a "floating configuration" was used for forming and I–V sweeps, and finally, a "V/2-biasing configuration" was used for state tuning.

## III. Results

Both bottom and top crossbar layers have similar electrical behavior and satisfactory device-to-device uniformity. In particular, the virgin (preforming) devices have an average conductivity and standard deviation, respectively, of 1.7 and 0.62 nS for the bottom crossbar and 0.56 and 0.38 nS for the top one [Fig. 2(d)]. The bottom crossbar has a slightly higher conductivity despite the fact that the bottom and top active layers were deposited in the same chamber conditions. A likely reason for this slight difference is the sample heating in an $O_2$

atmosphere at 175 °C during the sacrificial $SiO_2$ deposition, which might have caused minor stoichiometry or crystallinity shifts in the bottom active layer.

All 10 × 10 devices in both layers were successfully formed [Fig. 2(a) and (b)]. The forming was done sequentially by applying quasi-dc current ramps with a 3 V compliance provided by the measurement tool to the selected column, first for the bottom devices and then for the top ones. Immediately after successful forming, the device was turned OFF using a quasi-dc voltage of −2.4 V. The average forming voltage was ∼2.5 V for the bottom devices and ∼2 V for the top ones. The difference is probably due to the different virgin conductances as explained above. Initially, devices were formed at ∼10–50 $\mu$A, though the forming current increased to ∼100–700 $\mu$A as more devices were getting formed due to the increased leakage. The thermal crosstalk was negligible during the forming process with the devices adjacent to the device being formed maintaining their virgin or OFF state.

The bottom and top devices have similar electrical characteristics as shown by the $I$–$V$ curves for all the 100 bottom and 100 top devices of the crossbars [Fig. 2(c)]. These curves are taken by applying a conservative −1.8 V reset voltage and 300-$\mu$A set current more desirable for analog switching behavior, and show an ON/OFF current ratio of ∼10 at small biases. The application of more aggressive reset voltage of −2.4 V increases the ON/OFF ratios to >100 [Fig. 2(d)].

The device-to-device variations in switching behavior were investigated by characterizing the effective switching thresholds for all devices in the circuit. Each device was first tuned to a high conductive state of 200 kΩ. The device was then set to 70 kΩ using write voltage pulses of gradually increasing positive amplitude, and after that reset back to 200 kΩ using write voltage pulses of gradually increasing negative amplitude [Fig. 2(e)]. The bottom and top devices have similar threshold distributions, as shown in Fig. 2(f), which show set and reset threshold voltages calculated as the smallest voltages at which the cumulative changes in resistance were at least 10%. For all tuning measurements, 500-$\mu$s-long write voltage pulses were applied in a V/2-biasing configuration, while read measurements were performed in ground configuration with 0.3 V read pulses.

The most exciting feature of the developed memristive crossbar circuits is their analog memory property. The devices in both layers show good analog tunability. For example, Fig. 3(a) and (b) shows the results of tuning of the selected bottom and top layer devices to a 20-$\mu$S desired conductance with an excellent accuracy and state uniformity. Fig. 4(a) and (b) shows results of tuning individual device to 16 clearly distinguishable states equally spaced in the 2–32-$\mu$S range. The devices were tuned to 1% precision using the tuning algorithm presented in [21] with 500-$\mu$S-long voltage pulses of maximum amplitudes ±2.6 V and a step of ±0.01 V. The ultimate precision was not investigated, but the previous work [21] showed that it is dependent on the noise level and on the state. Moreover, there is no noticeable drift in conductance at room temperature over a measured ∼5 h period [Fig. 4(c)]. Low frequency (1/f) noise is rather high for some devices [Fig. 4(d)], however, it was only observed in a small fraction (∼20%) of the devices, and was more pronounced in the top-layer crossbar, probably due to surface defects introduced during the planarization process.

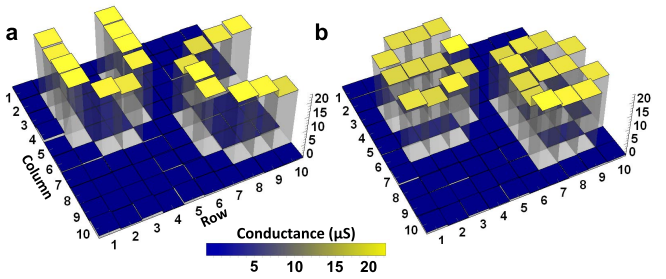


Fig. 3. Crossbar programming. (a) Results of tuning 19 bottom crossbar devices to 20 $\mu$S. Average device conductance and its standard deviation were 21.33 and 1.08 $\mu$S, respectively. (b) Results of tuning 25 devices in the top crossbar to 20 $\mu$S with 10% precision. Average device conductance and its standard deviation were 19.52 and 1.13 $\mu$S, respectively. The tuning was performed using previously developed algorithm [21] with 500-$\mu$s voltage pulses with maximum ±2.6 V and a step of ±0.01 V, which was extended to crossbar circuits by applying write voltages in V/2-bias configuration [20], [39].

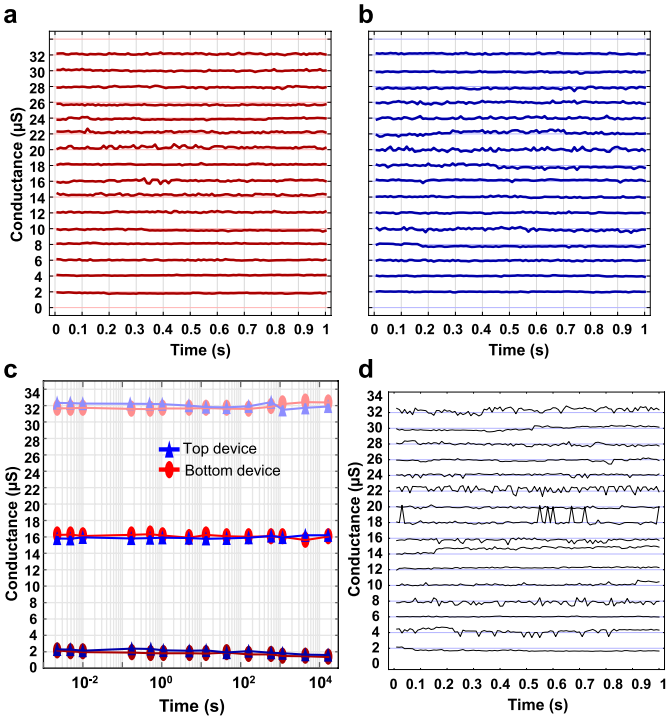


Fig. 4. Multistate tuning and retention. (a) and (b) Tuning results to 16 different conductive states with 1% precision using the algorithm in [21] and Fig. 3, equally spaced from 2 to 32 $\mu$S, for (a) R2C2 bottom and (b) R2C2 top devices. The state was read in virtual ground configuration every 10 ms by applying 500-$\mu$s-long 0.3 V high-voltage pulse for a total of 100 readouts. (c) Retention of the OFF (dark), ON (light), and intermediate states (medium brightness) for bottom and top devices, measured at room temperature. (d) Representative worst case low frequency (1/f) noise for a top device.

The high switching temperature and the thin shared middle electrode posed a risk for thermal crosstalk in the structure. Forming and switching of the bottom and top devices did not disturb the state of others (Fig. 5), thus suggesting that thermal crosstalk is negligible.

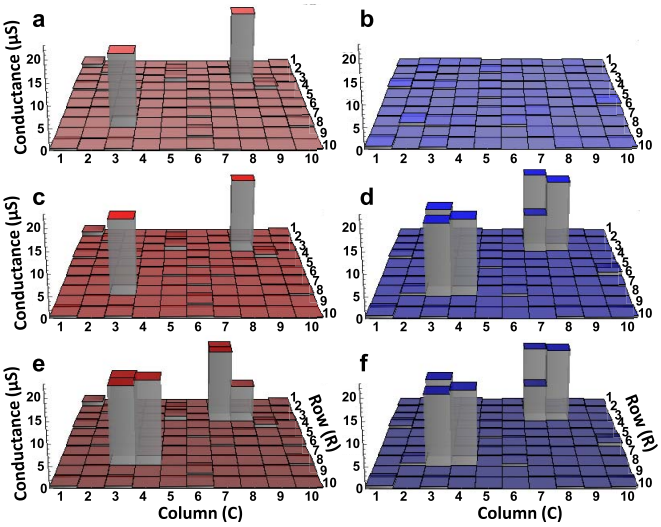


Fig. 5. Reliable crossbar operation, free of thermal crosstalk. (a) and (b) Switching ON two bottom devices—R3C8 and R8C3 [see (a)]. The neighboring device states are unaffected. (c) and (d) Switching ON six top devices—R2C7, R3C7, R3C8, R7C3, R8C3, and R8C4 [see (d)]. The neighboring device states are unaffected. (e) and (f) Switching ON four more bottom devices—R2C7, R3C7, R7C3, and R8C4 [see (e)]. The neighboring device states are unaffected, but the R3C8 device state is changed slightly, probably due to the half-select problem. The conductance maps were read at 0.3 V in the "virtual ground" configuration. Left: bottom crossbar conductances. Right: top crossbar conductances.

## IV. Discussion

We believe that the presented results are encouraging in that fully functional two-layer memristive crossbar circuits with analog memory functionality that can be fabricated in academic settings. The fabrication process has a low temperature budget, with the highest temperature being 175 °C during the sacrificial $SiO_2$ deposition for planarization. Therefore, such a developed process is compatible with back-end-of-line integration with CMOS circuits and can be extended to the fabrication of multiple ($>2$) crossbar layers.

By utilizing industry-grade fabrication tools, it should be straightforward to increase the scale, lateral density, and the number of layers. Indeed, the crossbar line pitch in this paper was limited by the resolution of the available DUV patterning tool. Recent studies showed that similar metal-oxide devices based on the same bilayer stack of materials could be scaled to $<10 \times 10$ nm$^2$ dimensions and still preserve excellent analog memory functionality [22], [40]. In fact, many memristor characteristics, which are particularly important for increasing the crossbar size, are improved upon scaling down the device's lateral dimensions. For example, switching threshold variations and switching currents have been shown to reduce upon scaling in metal-oxide devices [23], [40] likely due to reduced parasitic leakage and secondary switching [41].

Some of the immediate future works could be targeted on improving fabrication process to further reduce device variations in multilayer crossbar circuits. For example, a better wafer scale yield for planarization could be achieved through a back-end-of-line polishing technique [42], [43], which removes all the sacrificial dielectric while only slightly polishing the metal lines, and thus making sure that all the middle electrodes are fully exposed before the deposition on the new crossbar layer. The impact of the electrode slope on the device performance should be further investigated.

Finally, let us mention that though we have not tried to optimize device $I$–$V$ nonlinearity in this paper, it was not absolutely crucial for the considered crossbar size. Selector functionality is not essential for the operation of neuromorphic circuits. During operation, all crossbar lines are biased to certain voltages, and currents from all devices are collected, so that there are no leakage or stray currents flowing in the circuit [20]. It might be beneficial to have selector functionality to reduce leakages in the half-selected devices during the write operation, i.e., upon tuning, to avoid voltage drops across wires. However, this problem can also be solved by reducing line resistance, which should be possible with industrial-grade fabrication tools. By comparison with previous lift-off techniques, the developed fabrication process could be modified to increase metal line thickness through the use of a thicker hard mask for the Ar IBE.

## V. Conclusion

In summary, we have experimentally demonstrated analog memory functionality in a passive stack of two monolithically integrated $10 \times 10$ $TiO_2$-based memristor crossbar circuits. To ensure reliable stacking and compatibility with a CMOS process, a $<175$ °C temperature budget was used during the fabrication. The active layers of precisely controlled stoichiometry were deposited *in situ* via reactive sputtering and patterned with Ar ion beam milling. The bottom crossbar layer was planarized to reduce the step height and to provide a smooth surface for the top device deposition. As a result, 74% die yield was achieved across the 4-in wafer.

All of the 100 bottom and 100 top devices were formed and switched successfully. The devices in the two layers showed fairly similar behavior and threshold characteristics with good retention for the ON, OFF, and intermediate states. The devices were tuned to 16 clearly distinguishable states equally spaced in the 2–32-$\mu$S range showing good analog behavior. The demonstrated results are an important step toward multilayer passive memristive crossbar circuits that can be efficiently integrated with CMOS circuits, in particular of the 3-D CMOL variety, for neuromorphic and analog computing applications.

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