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Wafer-scale integration of two-dimensional materials in high-density memristive crossbar arrays for artificial neural networks

Shaochuan Chen[1,2], Mohammad Reza Mahmoodi[2], Yuanyuan Shi[3], Chandreswar Mahata[1], Bin Yuan[1], Xianhu Liang[1], Chao Wen[1], Fei Hui[4], Deji Akinwande[5], Dmitri B. Strukov[2] and Mario Lanza[1]✉

Two-dimensional materials could play an important role in beyond-CMOS (complementary metal–oxide–semiconductor) electronics, and the development of memristors for information storage and neuromorphic computing using such materials is of particular interest. However, the creation of high-density electronic circuits for complex applications is limited due to low device yield and high device-to-device variability. Here, we show that high-density memristive crossbar arrays can be fabricated using hexagonal boron nitride as the resistive switching material, and used to model an artificial neural network for image recognition. The multilayer hexagonal boron nitride is deposited using chemical vapour deposition, and the arrays exhibit a high yield (98%), low cycle-to-cycle variability (1.53%) and low device-to-device variability (5.74%). The devices exhibit different switching mechanisms depending on the electrode material used (gold for bipolar switching and silver for threshold switching), as well as characteristics (such as large dynamic range and zeptojoule-order switching energies) that make them suited for application in neuromorphic circuits.

The integration of two-dimensional (2D) materials into solid-state electronic devices and circuits could help extend Moore's law and allow advanced beyond-CMOS (complementary metal–oxide–semiconductor) products to be fabricated[1,2]. While the wafer-scale synthesis of various 2D materials has been demonstrated[3,4], most circuital applications are relatively simple (such as logic gates or sensors) and rely on very large devices (transistors with channels of >100 µm, for example)[5,6]. Recently, small (<100-nm) transistors that use 2D semiconductors as the channel material have been successfully fabricated[7,8], but the devices were isolated and no applications were reported. The key limitations in the use of 2D materials in the development of high-density electronic circuits for complex applications are the low device yield and large device-to-device variability.

The use of 2D materials in the fabrication of memristors has shown particular promise, and these devices could be of use in both information storage and neuromorphic computing[9]. Such devices can exhibit properties that metal-oxide memristors do not, including high thermal stability[10], coexistence of threshold and bipolar resistive switching (RS)[11], high controllability of potentiation, depression and relaxation[12] and excellent mechanical stability and transparency[13]. However, 2D-material-based memristors are typically fabricated by mechanical exfoliation; yield and device-to-device variability are not reported and circuital applications are rarely demonstrated. RS devices made using liquid-phase-exfoliated molybdenum disulfide[14] have been demonstrated and used to build flexible pressure sensors. However, the lateral size of the metal–insulator–metal cells[15,16] presented in that work[14] is over 900 µm^2, and the high number of uncontrollable defects at the randomly oriented nanoflake junctions results in a relatively poor endurance (around 100 cycles), a problem known to occur for memristors made of liquid-phase-exfoliated materials[17].

In this Article, we report the fabrication and statistical analysis of high-density memristive crossbar arrays made of 2D layered materials, and use them to model an artificial neural network for image recognition. Our devices, which can be as small as 150 nm × 150 nm, use chemical-vapour-deposited (CVD) multilayer hexagonal boron nitride (h-BN) as the RS medium, and exhibit different switching mechanisms depending on the electrode material used (gold for bipolar RS and silver for threshold RS). By many metrics, both types of device achieve performances that are superior to state-of-the-art metal-oxide memristors, and we report a high device yield of more than 98%.

Fabrication and characterization of crossbar arrays

We used large-area multilayer h-BN grown by CVD and transferred it onto 2-inch SiO_2/Si wafers to construct memristive crossbar arrays with vertical Au/h-BN/Au and Ag/h-BN/Ag structure (see Fig. 1a–c, Supplementary Figs. 1–5 and Methods). The h-BN shows correct layered structure (Supplementary Fig. 6) with atomically wide (<1-nm) native defects embedded, which propagate vertically and form percolation paths (Fig. 1d and Supplementary Fig. 7). The average density of defects measured by transmission electron microscopy (TEM) and conductive atomic force microscopy (CAFM) is ~150 spots µm^{-1} and ~250 spots µm^{-2} respectively (Fig. 1d–f and Supplementary Figs. 8–10)—discrepancies are expected due to the shape of the CAFM tip and the voltage applied[18,19]. By applying constant voltage stresses locally with the CAFM tip we

[1]Institute of Functional Nano and Soft Materials (FUNSOM), Collaborative Innovation Center of Suzhou Nanoscience & Technology, Soochow University, Suzhou, China. [2]Electrical and Computer Engineering Department, University of California at Santa Barbara, Santa Barbara, CA, USA. [3]IMEC, Leuven, Belgium. [4]Materials Science and Engineering Department, Technion—Israel Institute of Technology, Haifa, Israel. [5]Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX, USA. ✉e-mail: mlanza@suda.edu.cn

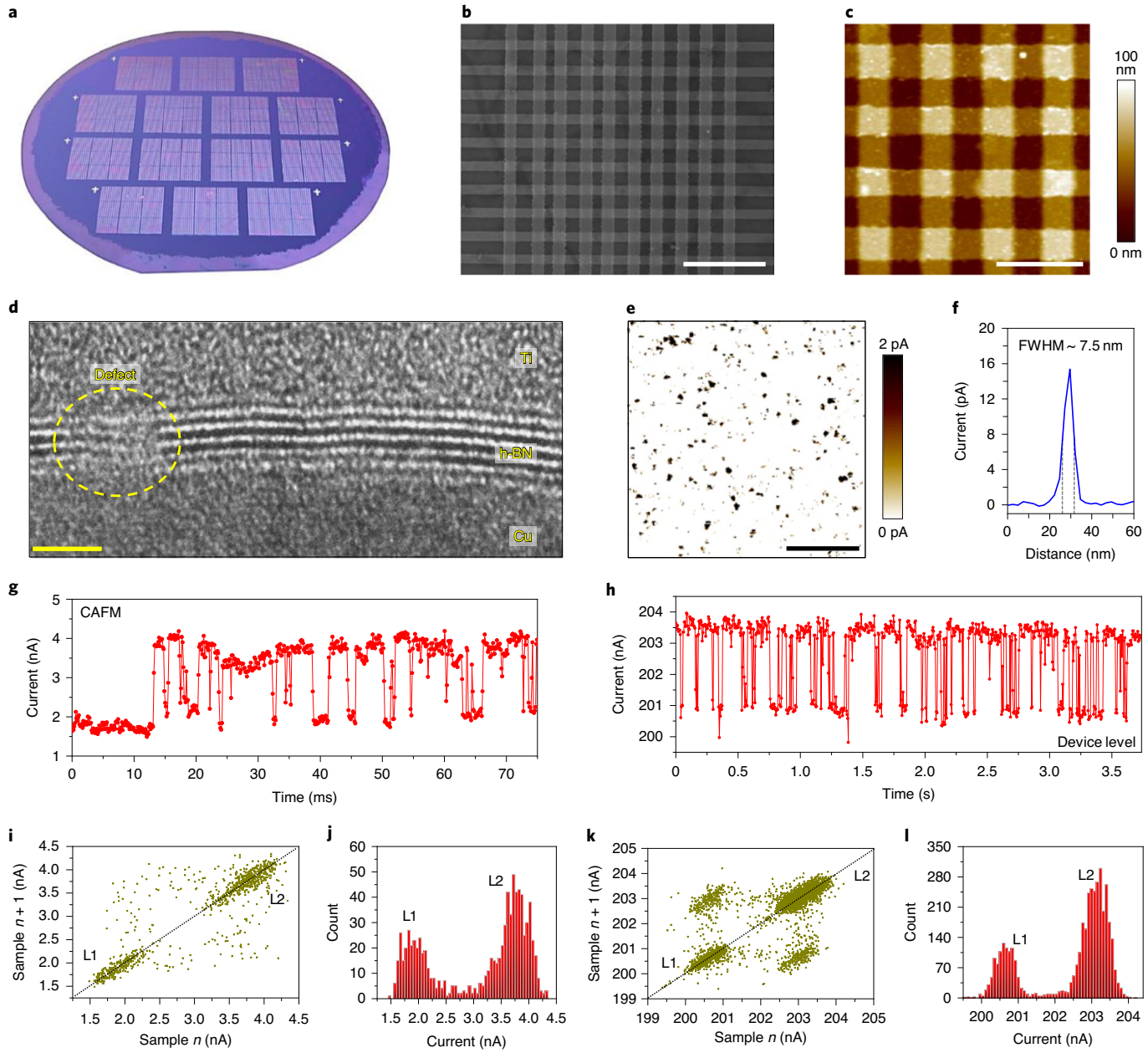

Fig. 1 | Material characterization and crossbar array fabrication. a, Photograph of a 2-inch wafer with Au/h-BN/Au memristive crossbar arrays distributed along it. **b**, Scanning electron microscopy (SEM) image of a crossbar array containing 750-nm × 750-nm Ag/h-BN/Ag memristors on the wafer. Scale bar, 4.5 µm. **c**, AFM topographic map of a part of the Ag/h-BN/Ag memristor crossbar array shown in **b**. Scale bar, 2 µm. **d**, Cross-sectional TEM image showing the layered structure of h-BN and defective paths through the layers (yellow oval area). Scale bar, 1.5 nm. **e**, Small-area CAFM map recorded inside an h-BN grain of the polycrystalline h-BN stack. Scale bar, 250 nm. The statistical analysis of the h-BN grain area of each conductive spot is shown in Supplementary Fig. 8. **f**, Cross-section of a representative conductive spot inside the h-BN domains, indicating the diameter (~7.5 nm) calculated via the full-width at half-maximum (FWHM) method. **g**,**h**, Current versus time (*I*–*t*) curves collected with the tip of the CAFM placed on a conductive spot by applying $V = 5$ V, and with the probe station in 5-µm × 5-µm metal/h-BN/metal devices (respectively). **i**,**j** and **k**,**l**, The random telegraph noise analysis of **g** and **h** (respectively). L1, Level 1; L2, Level 2.

observe that (1) the conductive spots show characteristic random telegraph noise signals[20], demonstrating abundant charge trapping and detrapping (Fig. 1g,i,j and Supplementary Figs. 11–13), and (2) the insulating areas show longer time to breakdown, which moreover is irreversible. When similar tests are applied at the device level, random telegraph noise characteristics similar to those observed at the conductive spots have been observed (Fig. 1h,k,l), proving that the electrical characteristics of the entire devices are governed by the local defects.

Initially, all the Au/h-BN/Au memristors showed characteristic electroforming process[15] at voltages ranging between 3 V and 8 V (Supplementary Fig. 14). After this, the devices exhibited stable non-volatile bipolar RS between a high-resistance state (HRS) and a low-resistance state (LRS)[15]. Depending on the current compliance (I_{CC}) used during the set transition, the resistance of the Au/h-BN/Au cells in the LRS can be tuned (Supplementary Fig. 15), leading to $I_{LRS}/I_{HRS} > 10$ for $I_{CC} = 1$ µA and $> 10^6$ for $I_{CC} = 1$ mA (read at −0.1 V); all the resistive states are stable over time (Supplementary

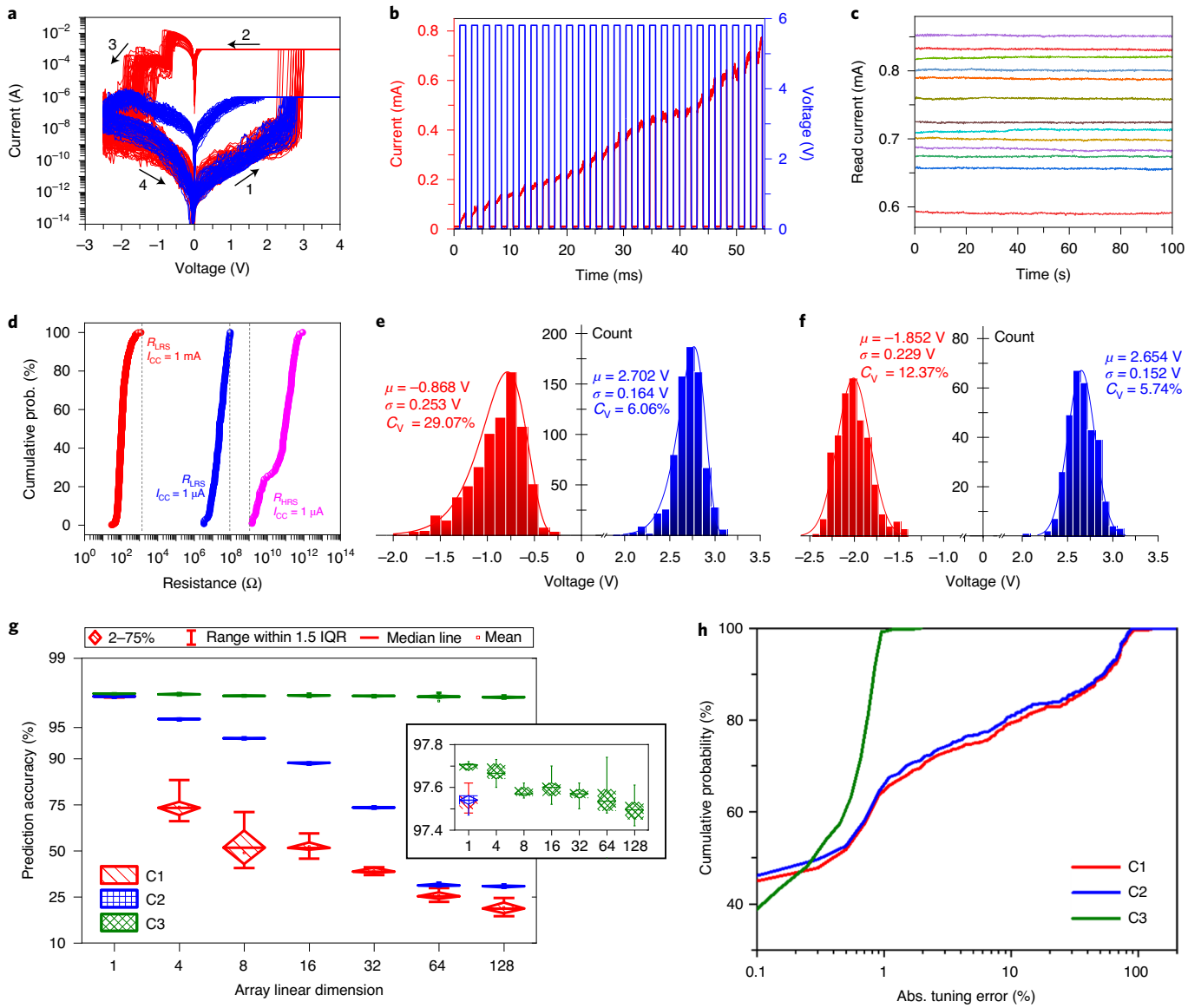

Fig. 2 | Bipolar RS in h-BN memristors and their application in neuromorphic computing. a, Representative *I*–*V* characteristics measured during 120 cycles in one single Au/h-BN/Au memristor using I_{CC} = 1 μA (blue lines) and I_{CC} = 1 mA (red lines). **b**, Sequence of PVSs (5.8 V/1 ms) showing analogue switching between two LRSs shown in **a**. **c**, *I*–*t* curves measured at 0.1 V, showing that the conductance states during the analogue transition (**b**) are stable. In total, >25 stable states have been measured for this type of memristor (Supplementary Fig. 19). **d**, Cumulative distribution plot of R_{HRS} and R_{LRS} measured over 1,500 cycles for 48 memristors. **e**, Cumulative distribution of device set voltages and reset voltages of 48 devices using 1-mA current compliance. **f**, Cumulative distribution of device set voltages and reset voltages of 16 devices using 1-μA current compliance. **g**, MNIST dataset simulation results for an ex situ-trained multilayer perceptron. The array linear dimension of 1 shows the case with no half-select disturbance, which is also representative of active (1T1R) crossbar array implementation. See Methods for more details of the neural network modelling. IQR, interquartile range. **h**, Example of device conductance statistics for a 64 × 64 crossbar array circuit, with the particular device parameters shown in Supplementary Fig. 26, after using a tuning algorithm with 1% desired tuning accuracy.

Fig. 16). When using I_{CC} = 1 μA, the devices show very low operating currents ranging from 0.2 pA to 1 nA in the HRS and from 10 nA to 500 nA in the LRS (read at −0.1 V; Supplementary Fig. 17), which strongly reduces sneak path currents and enables their use in high-performance neuromorphic circuits. The application of sequences of pulsed voltage stresses (PVSs) allowed analogue transition between the different resistive states (Fig. 2b; lower currents down to ~1 μA are shown in Supplementary Fig. 18), and >25 stable intermediate-conductance states ranging from 200 nS to 40 mS have been observed (Fig. 2c and Supplementary Fig. 19). This behaviour, never observed before in a 2D-material-based memristor, is a very important feature enabling the use of h-BN-based memristive crossbar arrays for neuromorphic applications[21].

In total, we have measured 104 Au/h-BN/Au devices from different crossbar arrays spread along the 2-inch wafer, and 102 of them showed bipolar RS characteristics very similar to those shown in Fig. 2a (Supplementary Fig. 20), implying a yield of ~98%. We statistically analysed >1,500 current versus voltage (*I*–*V*) curves collected in 48 devices (Supplementary Fig. 21), and quantified the cycle-to-cycle and the device-to-device variability of set voltage (V_{SET}) and reset voltage (V_{RESET}) by calculating the coefficient of variation (C_V) as the standard deviation (σ) divided by the mean value (μ)[22], in

absolute value. The statistical distributions of the resistances in the HRS and LRS (namely R_{HRS} and R_{LRS}) for the devices programmed at $I_{CC}=1$ mA and $I_{CC}=1$ μA are depicted in Supplementary Fig. 22. The cycle-to-cycle variability in a single device is attributed to the stochastic nature of the filamentary RS[23], and the device-to-device variability is attributed to inhomogeneity in the sample derived from the fabrication process[24,25], such as device area and thickness fluctuations, wrinkles and so on (Supplementary Figs. 23 and 24). For $I_{CC}=1$ mA, the minimum cycle-to-cycle variability of V_{SET} and V_{RESET} observed was 2.02% and 9.61% respectively, and their device-to-device variability rose to 6.06% and 29.07% when considering all 48 devices. When I_{CC} was reduced to 1 μA, the minimum cycle-to-cycle variabilities of V_{SET} and V_{RESET} observed were 1.53% and 6.21% respectively, and the device-to-device variabilities rose to 5.74% and 12.37% for a population of 16 devices. When analysing the variability of R_{HRS} and R_{LRS}, quantitative analyses calculating C_V are not so meaningful because the data are normally presented in a logarithmic scale. However, the data in Supplementary Fig. 22 indicate that the dispersion of R_{LRS} is always below 1.5 decades, and the current window is always >10, allowing reliable state distinction for all the cycles of all devices (even at low $I_{CC}=1$ μA). Furthermore, the variability of R_{LRS} from one device to another (20 devices) remains stable over long times (>1,000 s), as shown in Supplementary Fig. 25. It is worth noting that these standalone variability values have been obtained without the help of additional peripheral devices, such as a series transistor (so-called 1T1R cell), indicating that there is still room for further variability improvements[26]—although the use of series transistors remarkably increases the lateral size of each cell and reduces the integration density.

Multilayer perceptron network

To investigate potentials of using the developed technology in neuromorphic computing, we model a multilayer perceptron network based on crossbar circuits with integrated Au/h-BN/Au memristors. In particular, we considered ex situ-trained neural network circuits for neuromorphic inference[27], and modelled image classification of the Modified National Institute of Standards and Technology (MNIST) dataset, which is a typical entry benchmark for emerging devices[28–31]. We focused on the disturbance of half-selected devices at the conductance tuning process. This issue arises due to device-to-device variations in the effective switching thresholds[32], and is the major challenge for implementing neuromorphic inference accelerators based on memristive crossbar circuits[27,29]. Half-select disturbance is modelled phenomenologically, in agreement with nonlinear switching dynamics in non-volatile ionic memristive devices (Supplementary Fig. 26). The parameters of the model were chosen to reproduce measured variations in the set and reset switching thresholds (Supplementary Figs. 26 and 27).

The tuning error and classification accuracy were modelled for different array sizes and two slightly different assumptions for the tuning algorithm. Increasing linear dimensions of the crossbar array typically leads to better physical performance because of smaller peripheral circuitry overhead. However, it also results in more severe half-select disturbance and hence worse classification accuracy, as confirmed by the simulation results in Fig. 2g. Because of the higher observed variations in reset switching, we considered the case (labelled 'C3') when all devices in the crossbar circuit are reset initially to the low-conductance states before tuning. This modification of the tuning algorithm reduces the number of reset tuning pulses, and as a result leads to a smaller average tuning error and improved classification accuracy, especially for larger memory arrays, compared with the case (labelled as 'C2') with random initial conductance states (Fig. 2g,h). The most important result is that the classification accuracy for the reasonably sized (128×128) crossbar arrays[27] only drops by ~0.5% due to the device variations and is within 0.8% of the best classification accuracy (98.02%) that can be achieved with ideal, high-precision software-based implementation of the same network. Moreover, the simulation results show that such high accuracy could not have been achieved if the variations in set switching were higher, for example similar to those of reset switching (labelled with 'C1' in Fig. 2g,h).

Note that the few-microampere-scale operating current of many contemporary memristors is the other major challenge for implementing mixed-signal neuromorphic inference accelerators. High device currents result in larger energy and area overheads of sensing circuits, and could also lead to non-negligible voltage drops across crossbar lines, which significantly degrades dot-product computing precision. Because of the demonstrated wide dynamic range of currents, operating currents in the developed Au/h-BN/Au memristors can be chosen in a nanoampere range, more optimal for mixed-signal circuits.

Zeptojoule memristors for spiking neural networks

To further explore the volatile threshold RS in metal/h-BN memristive devices, Ag has been used as an active top electrode for programming the devices. The threshold RS devices are crucial in high-density three-dimensional memory crossbar arrays because they can effectively suppress the sneak current path. Moreover, recent works have shown that threshold RS devices can be also used as low-power integrate-and-fire artificial neurons in spiking neural networks, due to their self-reset process, high I_{LRS}/I_{HRS} and low energy consumption[33–35]. The h-BN memristors using Ag electrodes also exhibit excellent threshold-type RS for different I_{CC}, which can be as low as $I_{CC}=110$ fA (Fig. 3a–d, Supplementary Figs. 28 and 29 and Supplementary Table 1). In addition, Fig. 3e shows an outstanding switching slope of <0.09 mV per decade and high I_{LRS}/I_{HRS} ratios up to 10^{11} (Supplementary Table 1). The power consumption during the set transition (P_{SET}) can be as low as 44 fW (Fig. 3a), that is, $P_{SET}=I_{LRS}V_{SET}=110\,\text{fA}\times0.4\,\text{V}$, where I_{LRS} corresponds to the I_{CC} used in each experiment. By applying 5-V/2-μs pulses we statistically found that the set time (t_{SET}) is ~200 ns (Fig. 3f). Then, the value of the energy consumption per set transition (E_{SET}) in Fig. 3f can be calculated as $E_{SET}=I_{LRS}V_{SET}t_{SET}=20\,\text{nA}\times5\,\text{V}\times200\,\text{ns}=20\,\text{fJ}$. It should be highlighted that the higher electrical noise (>1 nA) of the semiconductor parameter analyser does not allow measurement of t_{SET} when using $I_{CC}=110$ fA (Fig. 3a) and $I_{CC}=1$ pA (Fig. 3b). However, E_{SET} can be estimated for $I_{CC}<1$ nA using the switching time obtained in Fig. 3f. This assumption is reasonable because the switching time from I_{HRS} to 110 fA (Fig. 3a) or from I_{HRS} to 1 pA (Fig. 3b) will surely be shorter than that between I_{HRS} and 20 nA (Fig. 3f). Consequently, E_{SET} in Fig. 3a–c may be as small as ~8.8 zJ, ~120 zJ and ~80 aJ respectively, which approaches the fundamental thermal energy at room temperature ($k_BT\sim4.1$ zJ)[36]. Such ultralow energy consumption is undoubtedly a feature that enables the use of these Ag/h-BN/Ag memristors as integrate-and-fire artificial neurons for energy-efficient spiking neuromorphic hardware[33–35].

The good stability of the threshold RS has been proved by applying PVSs, which demonstrate no degradation after more than 2,000 cycles (Fig. 3g). The application of PVSs with different amplitudes[37] also revealed that the Ag/h-BN memristive devices can be reliably operated at different current levels, and that the relaxation process is highly controllable and reproducible (Fig. 3h). The relaxation time (t_{RELAX}) increases with the pulse amplitude, and the characteristics of the devices can be fitted by the exponential decay function (Fig. 3i), which is consistent with the Kohlrausch law relaxation function[38,39], often used to emulate the short-term plasticity of biological synaptic systems[40].

The size of the Ag/h-BN/Au memristors has been reduced to 150 nm × 150 nm (Fig. 4a and Supplementary Figs. 30 and 31), and sequences of I–V curves and PVSs demonstrate stable threshold-type RS over 80,000 cycles (Fig. 4b,c) with low device-to-device variability (Fig. 4d). As explained in Supplementary Table 2, these endurance results are notable because previous works in this field showed

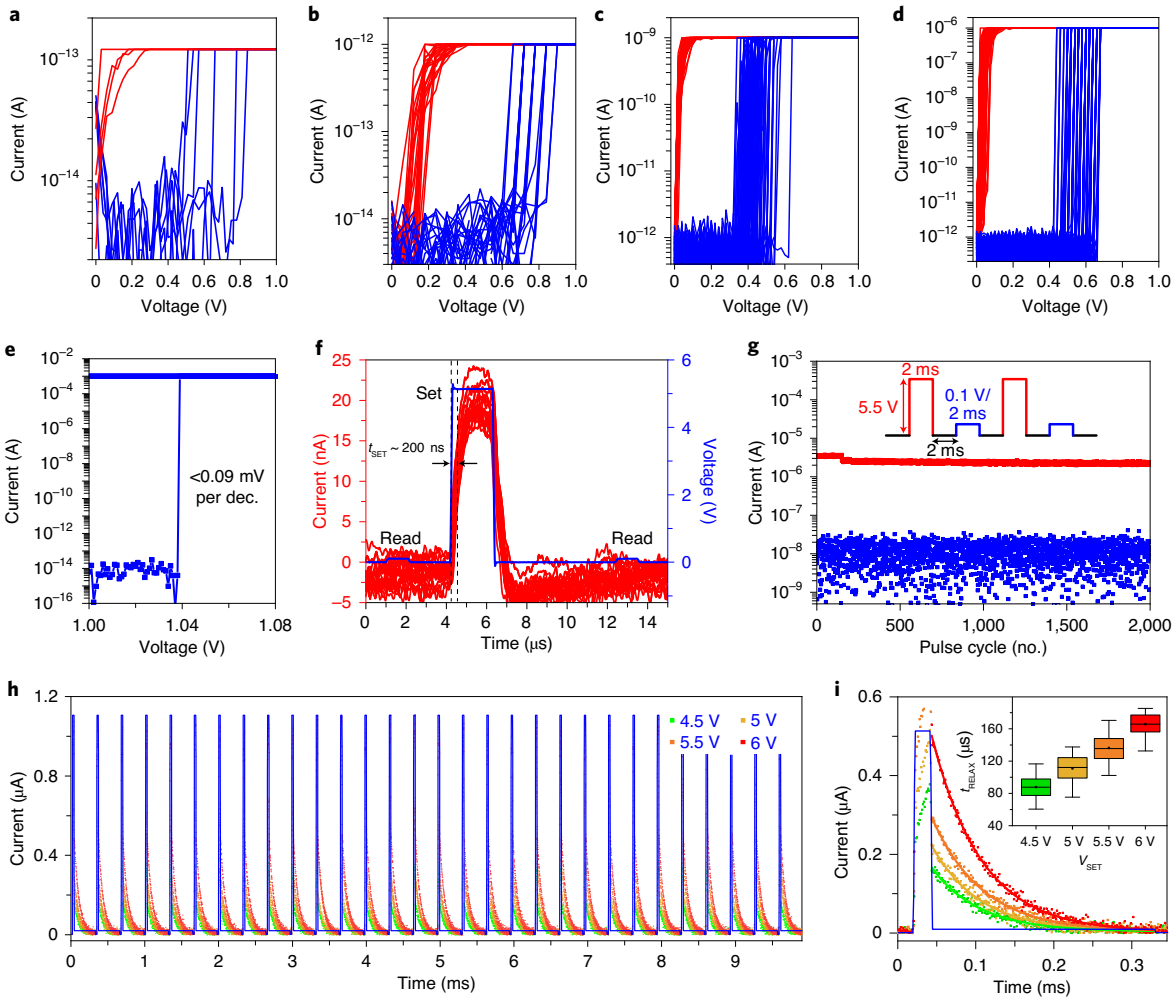

Fig. 3 | Threshold-type RS behaviour in h-BN memristors. a–**d**, Threshold-type RS characteristics of an Ag/h-BN/Ag memristor. The device exhibits high I_{LRS}/I_{HRS} current windows for ultralow I_{CC} down to 110 fA. The order of the measurements was **d** (first), **c** (second), **b** (third) and **a** (fourth), indicating excellent resistance recovery. **e**, Threshold-type RS characteristic measured in an Ag/h-BN/Ag memristor under $I_{CC}=1$ mA, exhibiting $I_{LRS}/I_{HRS}>10^{11}$ and switching slope of <0.09 mV per decade (Supplementary Table 1). **f**, Statistical calculation of t_{SET} using fast a.c. pulse measurements (that is 0.1-V/2-μs read pulse, 2-μs interval, 5-V/2-μs set pulse, 6-μs interval and 0.1-V/2-μs read pulse). To make the measurement more reliable, the experiment has been repeated 28 times (the number of red lines). As shown, t_{SET} ~ 200 ns. **g**, Endurance test of an Ag/h-BN/Ag memristor showing >2,000 cycles of operation. The inset shows the applied waveform, which consists of a 5.5-V/2-ms set pulse followed by a 0.1-V/2-ms read pulse. The interval between the set and read pulses is 2 ms. **h**, Reproducible multilevel operation of potentiation and relaxation in a 150-nm × 150-nm Ag/h-BN/Au threshold memristor under different pulse amplitudes. The potentiation of the device is achieved using a 20-μs set pulse, and the relaxation process is read using a 0.1-V/286-μs pulse. **i**, Zoom-in plot of one cycle shown in **h**; scattered symbols are experimental measurements, and solid lines are fittings to the exponential decay model, $I(t)=I_0\exp(-t/\tau)$, which is similar to the Kohlrausch law function, $I(t)=I_0\exp(-t/\tau)^{\beta}$ (where I_0 is the initial current before relaxation, β is a stretching index ranging from 0 to 1 and τ is a parameter with the dimensions of time[39,40]). Therefore, the current relaxation of Ag/h-BN/Au device can be fitted by the Kohlrausch law using $\beta=1$. Inset: the statistical distribution of the relaxation time for each pulse amplitude.

interesting electrical characteristics in 10-μm × 10-μm memristors (fabricated via photolithography), but the performances demonstrated in similar devices with sizes below 1 μm × 1 μm (fabricated via electron-beam lithography) were much worse[41,42]. Furthermore, the value of I_{HRS} and I_{LRS} in Fig. 4c,d is read in each cycle, which is the only correct method to characterize long endurance of memristors made of novel materials, as described in ref. [24].

Finally, extreme downscaling has been analysed in Ag/h-BN/Pt and Pt/h-BN/Pt memristors with nanodot-like top electrodes (see Fig. 4e,f, Methods and Supplementary Fig. 32). This methodology is very interesting for experimental purposes because it avoids the use of ultrathin metallic wires, which can easily melt due to the high current densities registered in the LRS—a recent report presented the fabrication of 2-nm × 2-nm memristor crossbar arrays[43], but only eight RS cycles with large variability of V_{SET} ranging between −2 V and −5 V were presented. Ag/h-BN/Pt devices show lower V_{SET} and higher switching slope than those using Pt top electrodes (see Fig. 4g,h and Supplementary Fig. 33b), in agreement with the lower dielectric breakdown time (T_{DB}) observed when applying constant voltage stress (Supplementary Fig. 34). Indeed, this experiment indicates that the threshold-type RS is dominated by the penetration of metal ions from top electrodes.

Conclusions

We have reported the fabrication of high-density crossbar arrays of Au/h-BN/Au memristors with a yield of 98%. The devices exhibit analogue switching within a large dynamic range of conductance (from 200 nS to 40 mS), ultralow cycle-to-cycle variability (down to

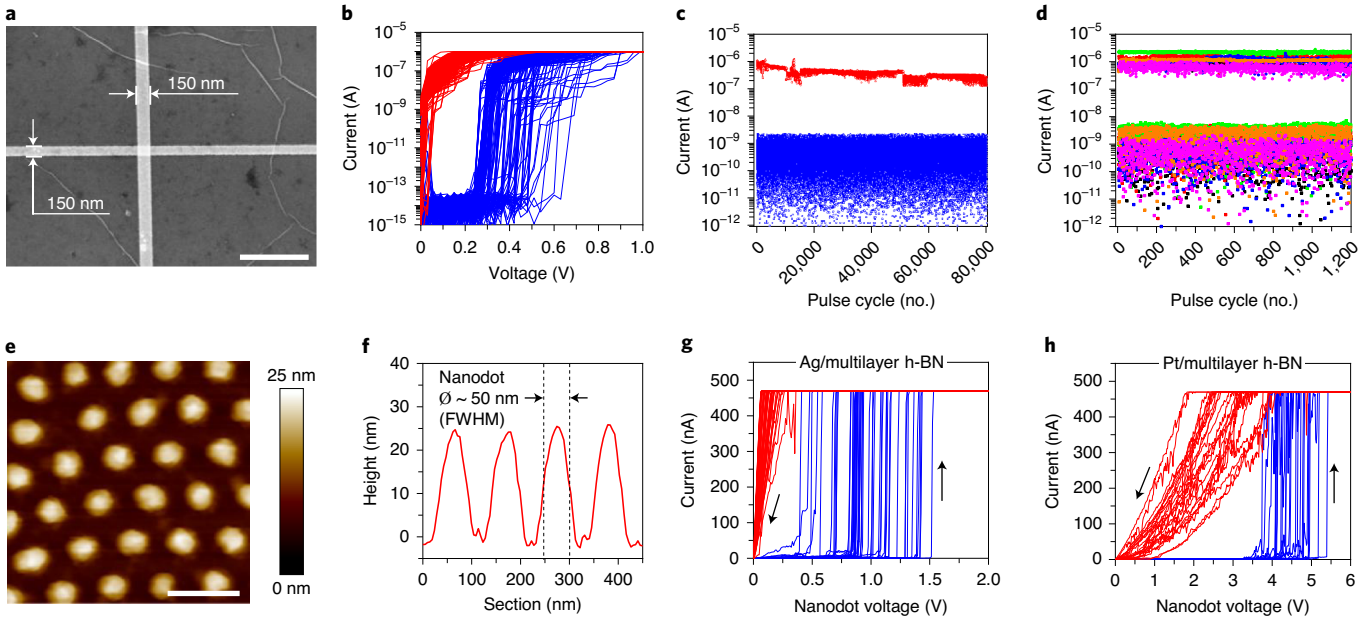

Fig. 4 | RS characteristics of nanoscale crossbar and nanodot memristors. a, Top-view SEM image of a 150-nm × 150-nm Au/Ag/h-BN/Au memristor. Scale bar, 800 nm. **b**, Threshold-type RS observed in a 150-nm × 150-nm Au/Ag/h-BN/Au memristor. **c**, Pulse endurance test of 150-nm × 150-nm Au/Ag/h-BN/Au memristor showing over 80,000 programming cycles. The applied set and read pulses are 4 V/2 ms and 0.1 V/2 ms, respectively. The interval between the set and read pulses is 2 ms. **d**, First 1,200 programming cycles measured during pulse endurance tests in six different 150-nm × 150-nm Au/Ag/h-BN/Au memristive devices, showing very low device-to-device variations. **e**, AFM topographic map (collected in tapping mode) of the nanodot-like Ag electrodes on the surface of the h-BN sheet. Scale bar, 150 nm. **f**, FWHM cross-section of the nanodots shown in **e**. **g**,**h**, Threshold-type RS characteristics of an Ag/h-BN/Pt and a Pt/h-BN/Pt nanodot memristor, respectively.

1.53%) and excellent standalone device-to-device variability (down to 5.74%). Simulation results for an ex situ-trained MNIST image classifier based on mixed-signal Au/h-BN/Au memristive hardware show that the measured I–V uniformity is sufficiently good for matching the accuracy of the ideal software-based implementation. Furthermore, when using silver electrodes, our h-BN memristors show multilevel threshold-type RS with ultralow switching energy in the zeptojoule regime and a very stable relaxation process that fits the exponential Kohlrausch-law function, which enables their potential application in spiking neuromorphic hardware. Our work is a step towards the development of high-density electronic circuits based on 2D materials, and could help accelerate the deployment of 2D materials in semiconductor fabrication lines.

Methods

h-BN growth. A multilayer h-BN sheet has been grown by chemical vapour deposition on Cu foils using ammonia borane as precursor. The detailed CVD growth process is exhaustively described in ref. [12].

TEM characterization. Directly after CVD growth, 20 nm Ti and 40 nm Au were deposited by electron-beam evaporation on the h-BN/Cu stacks to enhance the contrast during TEM inspection and protect against oxidation, respectively. The resulting Au/Ti/h-BN/Cu sample was cut into thin (~40-nm) lamellas using a focused ion beam (Helios NanoLab 450S, FEI), and the layered structure of the h-BN stacks was confirmed by TEM (JEM-2100, JEOL).

Fabrication of memristor crossbar arrays. The metal/h-BN/metal memristor crossbar arrays were fabricated on n-type Si wafers covered by 300 nm of thermal SiO_2. First, the bottom electrodes were patterned using photolithography (MJB4 Mask Aligner, SÜSS MicroTec) or electron-beam lithography (Raith ELPHY VII integrated with Supra 55 SEM); the devices with sizes of 3 μm × 3 μm were patterned via photolithography, and the devices with sizes of 750 nm × 750 nm and 150 nm × 150 nm were patterned via electron-beam lithography. Second, the metallic film was deposited by electron-beam evaporation (PVD 75 evaporator, Lesker), and the photoresist was removed by lift-off (that is via acetone bath for 1 h). Third, the layered h-BN stack was transferred onto the bottom electrodes (detailed transfer process in next section). Fourth, the top electrodes were deposited using a methodology identical to that for the bottom electrode (that is lithography, metal evaporation and lift-off). Several samples with different device sizes, h-BN thicknesses and metallic electrodes were fabricated. Sample 1 contained multiple memristive crossbar arrays (device size 3 μm × 3 μm) fabricated using 50 nm Au as bottom and top electrodes, leading to Au/h-BN/Au cells. Sample 2 contained crossbar arrays (device size 3 μm × 3 μm) fabricated using 20-nm Ag/10-nm Ti bottom electrodes and 30-nm Au/20-nm Ag top electrodes, leading to Au/Ag/h-BN/Ag/Ti structure cells. Sample 3 contained multiple 10 × 10 memristive crossbar arrays (device size 750 nm × 750 nm) fabricated using 30 nm Ag/10 nm Ti as bottom electrodes and 50 nm Ag as top electrodes, leading to Ag/h-BN/Ag/Ti structure devices. Sample 4 contained multiple 150-nm × 150-nm devices fabricated using 30 nm Au/10 nm Ti as bottom electrodes and 30 nm Au/10 nm Ag as top electrodes, leading to Au/Ag/h-BN/Au/Ti structure devices.

Transfer of h-BN. To transfer h-BN onto the bottom electrodes, liquid poly(methyl methacrylate) (PMMA) was spin-coated on the surface of multilayer h-BN grown on Cu foil. The spin-coating process consisted of 500 r.p.m. for 6 s and 3,500 r.p.m. for 30 s. Then, the device was baked at 100 °C for 3 min to solidify the PMMA and improve its adhesion to the h-BN stack. After baking, the Cu foil was etched using iron III chloride ($FeCl_3$, 0.1-g-ml^{-1}) liquid for 5 h, and the resulting PMMA/h-BN stack was cleaned in hydrochloric acid (HCl, 2 wt%) for 30 min and deionized water for 1 h. Next, the PMMA/h-BN stack was picked up with the target substrate (that is the SiO_2/Si wafer with bottom electrodes patterned) and dried at 60 °C for 5 min. Finally, the substrate was immersed in acetone (≥99%) for 12 h to remove the PMMA.

Fabrication of metal/h-BN/metal nanodot memristor. n^{++}Si wafers were first cleaned using 1% HF/H_2O solution to remove the native SiO_x layer. After cleaning, 50 nm Pt was deposited on top by an electron-beam evaporator, and the h-BN was transferred onto the Pt/n^{++}Si substrate. An ultrathin alumina membrane (UTAM) film with 300-nm thickness, 80-nm pore diameter and 100-nm interpore distance was purchased from Shenzhen Top Membranes Technology. The PMMA supporting layer attached to the UTAM film was first removed by acetone, and then the UTAM film was transferred onto the h-BN surface. After being washed with acetone three times, 25-nm Ag or 25-nm Pt electrodes were deposited on top via electron-beam evaporation. After deposition of the top metal layer, UTAM films were finally peeled off using polyimide (Kapton) tape.

Optical and SEM characterization. Morphology and structure information on the devices was obtained using a fluorescence optical microscope from Leica Microsystems (model DMi8) and a Supra 55 scanning electron microscope from Zeiss.

AFM characterization. The surface topography of memristor crossbar arrays and nanodot devices was characterized using an atomic force microscope from Bruker (Dimension Icon) working in ambient atmosphere. The topographic maps were collected in tapping mode using NanoWorld POINTPROBE tips (model NCH). The *I*–*V* characteristics of nanodot devices were collected in contact mode using standard Pt probes (tip radius < 20 nm) from Rocky Mountain Nanotechnology (model 25Pt300B). The bias was applied to the top nanodot electrodes, while keeping the sample substrate grounded.

Electrical characterization. The CAFM electrical analysis of h-BN was conducted via a Park NX-Hivac atomic force microscope working in a high-vacuum environment (~10^{-6} torr) and using solid Pt probes from Rocky Mountain Nanotechnology (model RMN-25PT300B). Electrical characterization of the memristor crossbar devices was performed using two measurement set-ups. The first one is a Cascade probe station (model M150) connected to a Keithley 4200-SCS semiconductor parameter analyser. The second one is a Lake Shore Cryogenic Probe Station connected to a Keysight B1500A semiconductor parameter analyser. Pulsed measurements were carried out using Keysight B1530A waveform generator fast measurement units (WGFMUs); a 1-MΩ resistor was connected in series to the memristors during the endurance test to limit the ON-state current. In all devices the voltage stress was applied to the top electrodes, while keeping the bottom electrodes grounded. In this investigation, the total number of devices measured via ramped voltage stress and pulse voltage stress is 550.

Artificial neural network simulations. A 784×64×10 multilayer perceptron network with hyperparameters similar to those in ref. [21] was simulated using a phenomenological model for half-select disturbance with a specific window function (Supplementary Fig. 26). Classification accuracy is reported for 10 runs, with randomly generated device variations used in each run, for different crossbar array sizes, and three different cases (C1–C3). For each run, classification accuracy is assessed after writing conductances to the same set of desired values using a tuning algorithm with 1% target accuracy[44]. The desired values were determined by mapping the weights, obtained by training the neural network in the software, to the differential pair of conductances. One of the memristors in a pair, depending on the sign of the weight, is always set to the smallest possible conductance G_{min}. When the crossbar size is smaller than required by the neural network algorithm, accurate summation of the partial dot products is assumed, which for example could be implemented with combination of local and global sensing circuitry. In C2 and C3, set and reset variations of the utilized half-select disturbance model were fitted to those observed in the experimental work. In C1, larger set variations, similar to the ones observed for reset switching, were modelled to highlight the impact of the variations. In C1 and C2, all conductances were randomly initialized in the dynamic range before applying the tuning algorithm. In C3, all devices were set initially to the low-conductance state (G_{min}). The devices were always tuned individually, in the same fixed order. The number of tuning iterations, that is the sequences of pulses with increasing write amplitudes, was limited to 10 to bound the tuning time.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

M.L. conceived the idea and designed the experiments. S.C., B.Y. and X.L. fabricated the memristor crossbar arrays. S.C., B.Y., X.L., Y.S., C.W. and F.H. characterized the memristor crossbar arrays. C.M. fabricated and characterized the nanodot memristors. M.R.M. and D.B.S. developed the neural network simulation. M.L., S.C., D.A. and D.B.S. wrote the manuscript. All authors discussed the data and revised the text.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to M.L.

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