Compact Models and Model Standard for 2.5D and 3D Integration

Qiaosha Zou, Yuan Xie
Computer Science and Engineering
The Pennsylvania State University
{qszou, yuanxie}@cse.psu.edu

ABSTRACT

3D integration is an emerging interconnect technology that can enable the continuation of performance scaling and the reduction of form factors. There are various approaches for 3D integration, including system-in-package (SiP), TSV-based 3D ICs, monolithic 3D ICs, and inductance/capacitance coupling 3D ICs, among which TSV-based 3D IC is the most promising one. This paper provides a summary of previous work on electrical modelings for 3D IC, with an emphasis on two key interconnect approaches: TSVs and RDLs. Based on prior work, we describe a compact model standard to facilitate a generic modeling approach for future 3D ICs.

1. INTRODUCTION

By utilizing the high density through-silicon vias (TSVs), three dimensional integrated circuits (3D ICs) and 2.5D designs are promising solutions to handle problems with continuously transistor scaling according to Moore's law, pushing circuit designs into the "More-than-Moore" regime. In additional to the low latency and high bandwidth vertical interconnects, 3D ICs can also provide the benefits of smaller footprint, improved packaging density, and heterogeneous stacking [4, 18, 6]. On the other hand, 2.5D circuits that once treated as an intermediate technology before realizing 3D integrations has now become a practical alternative implementation of true 3D IC designs. The interposer in 2.5D designs can provide high density and low latency connections between chips and I/O with affordable design cost and complexity overhead [14]. The disruptive Xilinx Virtex-7 is the first commercial 2.5D FPGA design using interposer. There are four metal layers and the trace width of each layer is $2\mu m$ [2]. As a comparison, for the connections with PCB (printed circuit board) for DDR4, the trace thickness and width for the signal layer are $0.6mil$ (a mil is 1/1000 of an inch) and $6mil$, respectively, and the corresponding single-ended impedance is about $39ohms$.

There are several enabling components in 3D and 2.5D ICs, including through-silicon-vias (TSVs), redistribution layers (RDLs), micro-bumps, monolithic 3D ICs, and inductance/capacitance coupling 3D ICs. Among these components, the high aspect-ratio TSVs, providing the connections between active dies, is the key technology for 3D/2.5D ICs. These newly introduced components influence the circuit performance in a way that traditional 2D electrical models cannot capture. Simple and accurate 3D interconnect models are required for better circuit performance predictions and design exchanges. Plenty of previous work have been done to explore the electrical, mechanical, and thermal characteristic of TSVs, however, these work are based on specific assumptions and the conclusions are limited to the corresponding assumptions (TSV size, connection methods, etc.). In practical, diverse fabrication processes, geometries, and materials have impacts on the characteristics of interconnect components, such as electrical properties, mechanical properties and thermal properties [4, 15]. Moreover, most of the 3D electrical behavior studies rely on the time-consuming multi-physics analysis tools. A compact 3D/2.5D model standard for electrical behavior is urgently needed to aid electronic design automation tools for 3D design modeling and design validation.

In this survey paper, previous work on electrical modelings of 3D designs are reviewed, emphasizing on two key indispensable interconnect components: TSVs and RDLs. The models of TSVs are categorized into two levels according to the model complexity and accuracy. Three types of RDL transmission lines are discussed and one equivalent circuit model is introduced for model simplicity. Modeling and verification methods are explained briefly as well as the given specific assumptions for better understanding.

The following sections are organized as belows. Section 2 introduces previous TSV electrical models in both low frequency and high frequency region. Section 3 illustrates the electrical characteristic of three types of RDL in interposers and briefly introduces the modeling of micro-bumps. In section 4 we describe our proposed 3D compact model based on the previous studies.

2. REVIEW OF TSV ELECTRICAL MODELINGS

The geometry of TSVs influences the final modeling accuracy. Most papers treat the TSV as equivalent cylindrical structure [12, 9, 16, 19]. The assumption of abstracting TSV structure into a simple cylindrical structure is examined by Savidis *et al.* [12]. This study compares the electrical parameters extracted from a cylinder structure contains both top and bottom copper landing to the proposed simple structure without landing by using Ansoft electromagnetic simulation tool. The results show that only less than a 7% difference in the final RLC (resistance, inductance, and capacitance) value, indicating that using simple cylindrical structure is sufficient for accurate TSV modeling. However, this paper only tested results with frequency as high as 1GHz under

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certain temperature. The conclusion may not be applicable for higher frequency beyond this point.

For circuit performance (delay, power consumption, heat dissipation) estimation, RLC model is the most straight forward modeling method by viewing the device as an equivalent circuit. The RLC model for single TSV and coupled TSVs with closed-form expressions are given for various analysis and design purposes [8, 5, 12, 16]. In these models, the resistance and inductance are in serial and the capacitance exists between the TSV and the substrate. However, these models treat silicon substrate as an ideal conductor (RC model) or dielectric (RLC model) which may bias the electrical value. The skin effect and eddy currents in silicon should be taken into consideration for the TSV modeling at AC and high frequencies [20]. Skin effect means the current density drops by a certain factor below the surface of a conductor. It has significant impact on the high frequency resistance. Under this circumstance, the RLCG model is usually used for high frequency TSV modeling [20, 11]. This model contains two components: admittance per unit TSV height which consists of conductance and susceptance; impedance per unit TSV height which is composed of resistance and reactance. In this section, both the RLC and RLCG models are introduced. In the RLC modeling, in addition to an isolated TSV, the scenario of coupling between TSVs are also considered.

2.1 The RLC model for Single TSV

For a single TSV (without considering the influence from other TSVs), the RLC model is shown in Figure 1(a). Capacitances exist between the TSV and the adjacent substrate while resistance and inductance are in serial along the TSV. Considering the model accuracy and complexity, the resistance modeling is directly derived from the equivalent transmission line. Since the silicon has finite conductivity and the oxide dielectric layer, the modeling of capacitance between TSV and the silicon substrate should consider the MOS (metal-oxide-semiconductor) effect. For the inductance, an empirical close-form equation is given.

The resistance can be described as a function of TSV conductivity (σ), TSV length (l), and radius (r):

$$R_{tsv} = \frac{l_v}{\sigma \pi r_v^2} \tag{1}$$

The effective capacitance in TSV is the depletion capacitance (C_{dep}) and the oxide capacitance (C_{ox}) acting in serial.

$$C_{TSV} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \tag{2}$$

The oxide capacitance is related to the permittivity of silicon and oxide and the TSV gemometry, which can be capture as follows:

$$C_{ox} = \frac{2\pi \varepsilon_{Si} \varepsilon_{ox} L_{TSV}}{ln(1 + \frac{T_{tox}}{R_{TSV}})} \tag{3}$$

Nevertheless, the depletion capacitance is infeasible to express in a single close-form equation. The value is determined on the depletion region width, which relies on the flat bend voltage and the bias voltage in silicon substrate. In general, the depletion capacitance is given as follows while

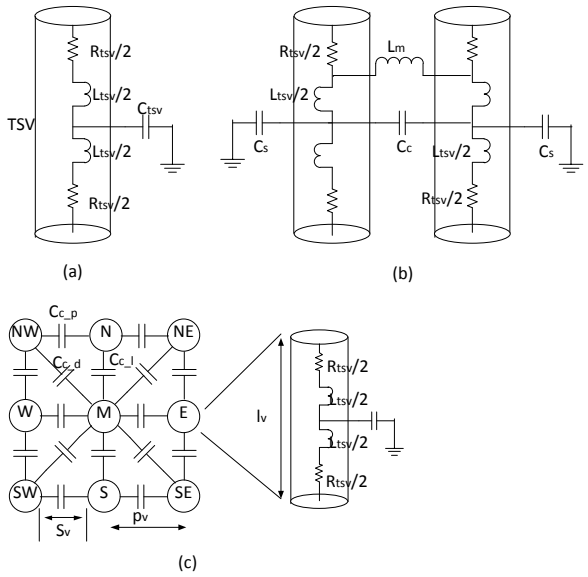


Figure 1: The resistance, inductance, and capacitance model for (a) A single TSV; (b) Two coupled TSVs; (c) A TSV bundle[16].

the flat bend voltage calculation can refer to the MOS effect.

$$C_{dep} = \frac{2\pi \varepsilon_{Si} L_{TSV}}{ln(1 + \frac{T_{tox} + W_{dep}}{R_{TSV}}) \sqrt{1 + \frac{V_{tsv}}{V_{th}}}} \tag{4}$$

The final effective capacitance is a function of its geometry and the effective permittivity (ϵ_0) of surrounding dielectric liner. The following expression is based on empirical value which assumes the thickness of dielectric layer is smaller than $1\mu m$ [16]:

$$C_{tsv} = \frac{63.36 \varepsilon_0 l_v}{ln\left(1 + 5.26 \frac{l_v}{r_v}\right)} \tag{5}$$

When the TSV is treated as a lossy transmission line in the model, the inductance has great impact on signal propagation delay. The propagation delay study by Khalil *et al.* [9] shows that without the presence of inductance in TSVs, the average error is 55.2% higher than RLC model with the value of the distributed RLC. The inductance of an isolated TSV is depended on the geometry parameters. It can be expressed as follows [16]:

$$L_{tsv} = \frac{\mu l_v}{2\pi} ln\left(1 + \frac{2.84}{\pi} \frac{l_v}{r_v}\right) \tag{6}$$

All the above empirical closed-form equations predict the RLC values within maximum 6% error verified by a 3D/2D quasi-static electromagnetic-field solver tool. By using these closed-form expressions, the resistance, capacitance, and inductance values in a single TSV can be easily calculated for fast circuit simulation.

2.2 The RLC Model for Coupled TSVs

The equivalent RLC circuit of two coupled TSVs and a TSV bundle is shown in Figure 1(b) and (c), respectively. For coupled TSVs, the resistance expression is the same as the R in an isolated single TSV since coupling effect has

no impact on the resistance. But for the inductance and capacitance, the inter-via coupling plays an important role. Capacitance and inductance are divided into two parts: self parameter and mutual parameter.

The capacitance terms of the whole coupled bundle TSV can be expressed as follows [16]:

$$C_{bundle} = \begin{bmatrix} C_{1,1} & -C_{1,2} & ... & -C_{1,n} \\ -C_{2,1} & C_{2,2} & ... & -C_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n,1} & -C_{n,2} & ... & C_{n,n} \end{bmatrix} \quad (7)$$

The diagonal elements represent the sum of self and inter-via coupling capacitances. This capacitance matrix is sparse because only diagonal elements and elements for nearest neighbors contain meaningful values. From the experiments, in a 7 x 7 TSV bundle, coupling effects among nearest neighbors are much significant than those that are non-adjacent.

The self capacitance formula is different from the isolated TSV, which is given as:

$$C_s = C_{TSV} - k_1 C_{TSV} e^{(k_2 \frac{p_v}{r_v} + k_3 \frac{p_v}{l_v})} \left[k_4 \left(\frac{L_v}{r_v} \right)^{k_5} + k_6 \left(\frac{p_v}{r_v} \right)^{k_7} + k_8 \right] \quad (8)$$

where the parameters from k_1 to k_8 are empirical constants. However, these constants are based on the simulation results and vary with different TSV configurations, making it difficult to be directly applied in circuit simulations. When k_2 and k_3 are negative and p_v approaches infinity, C_s equals to C_{TSV}.

The formula for the coupling capacitance where $i \neq j$ in the matrix is given as follows. This model has maximum 6% error from the simulation results.

$$C_{coupled} = \frac{k_1 \epsilon_0 l_v}{ln(k_2 \frac{pv}{rv})} \left[1 + k_5 \left(\frac{L_v}{r_v} \right)^{k_6} + k_3 \left(\frac{p_v}{r_v} \right)^{k_4} + k_7 \left(\frac{p_v}{l_v} \right)^{k_8} \right] \quad (9)$$

The coupling inductance can also be defined by the matrix similar to the coupling capacitance. Different from the capacitance, inductive coupling has longer range so the matrix is not sparse. The mutual inductance between any two TSVs can be captured with the following formula:

$$L_m = 0.199 \mu l_v ln \left(1 + 0.438 \frac{d_v}{l_v} \right) \quad (10)$$

where d_v is the center-to-center distance between two TSVs. The maximum error for coupling inductance is within 8%.

2.3 The RLCG Model for A Pair of TSVs

The equivalent distributed circuit model is shown in Figure 2(a), the simplified model is given in Figure 2(b). The impedance, which is represented by Z, is similar to the resistance and inductance in serial in RLC model. Capacitance exists inside the depletion region between the TSV and the silicon substrate. Admittance, which is represented by Y, exists in the silicon substrate between two adjacent TSVs. In this figure, Y_{open} is the input admittance between ports 1 and 2 if ports 3 and 4 are open while Z_{short} represents the impedance between ports 1 and 2 when ports 3 and 4 are short circuited.

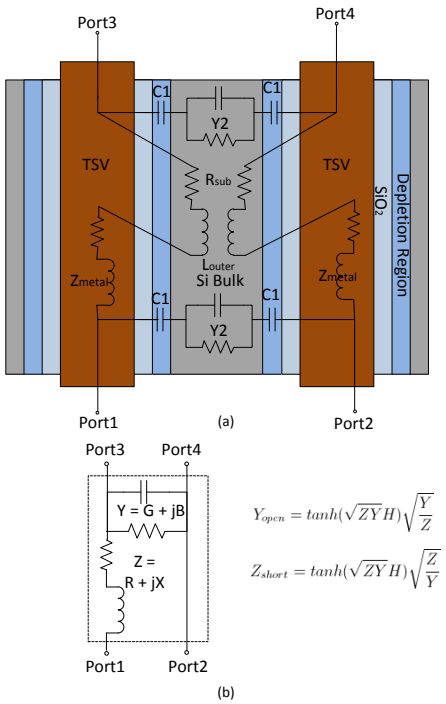


Figure 2: The RLCG model for TSVs: (a) the equivalent distributed RLCG model of two coupled TSVs; (b) a simplified distributed transmission line model [20].

Admittance of TSV in RLCG model. The admittance (CG) per unit TSV height can be treated as two components functioning in serial: one is the silicon depletion region (C_1) and the other is the coupling admittance (Y_2) in the bulk silicon. The admittance formula is shown in the following equation:

$$Y = [2(j\omega C_1)^{-1} + Y_2^{-1}]^{-1} \quad (11)$$

where ω is the radial frequency. Since there are two TSVs contribute to C_1 in serial with Y_2, the equation contains a factor of 2 before C_1.

The capacitance in the depletion region (C_1) can be captured with the following formula:

$$C_1 = [\frac{1}{2\pi\varepsilon_{OX}} \cdot ln \left(1 + \frac{t_{OX}}{r_{via}} \right) + \frac{1}{2\pi\varepsilon_{Si}} \cdot ln \left(1 + \frac{\omega_{dep}}{r_{via} + t_{OX}} \right)]^{-1} \quad (12)$$

where ε_{OX} and ε_{Si} represent the permittivity of dielectric and silicon substrate, respectively. The geometrical parameters r_{via}, t_{OX}, and ω_{dep} are the via radius, isolation layer thickness and silicon depletion width.

The coupling admittance in Si bulk can be illustrated with following equation (σ_{Si} is the conductivity of silicon):

$$Y_2 = \pi(\sigma_{Si} + j\omega\varepsilon_{Si}) / arccosh \left(\frac{d}{2} / (r_{via} + t_{OX} + \omega_{dep}) \right) \quad (13)$$

The CG model is verified with a 2-D quasi-electrostatic simulation tool. The results suggest that at low frequencies, if the depletion region is not considered, the error is not negligible. However, the difference is not so significant at high frequencies.

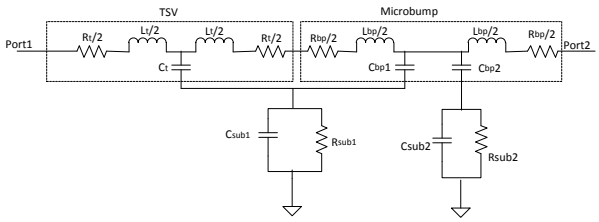


Figure 3: The RLC model of micro-bumps[17].

Impedance of TSV in RLCG model. The serial impedance (RL) per unit height is not so straight forward. The final expression results are shown without detail deduction steps. For simplicity, the serial impedance can be treated as the sum of three components: the inner impedance of TSV (Z_{metal}); the outer inductance (L_{outer}); and the resistance due to eddy currents in silicon substrate (R_{sub}):

$$Z = 2Z_{metal} + j\omega L_{outer} + R_{sub} \tag{14}$$

The equations for these three components are given as followings:

$$Z_{metal} = \frac{(1-j)\cdot J_0((1-j)r_{via}/\delta_{metal})}{\sigma_{metal}\cdot 2\pi r_{via}\delta_{metal}\cdot J_1((1-j)r_{via}/\delta_{metal})} \tag{15}$$

$$R_{sub} \approx \frac{\omega\mu}{2}\cdot \tag{16}$$
$$Re\left[H_0^{(2)}\left(\frac{1-j}{\delta_{Si}}9r_{via} + t_{OX} + \omega_{dep} - H_0^{(2)}\left(\frac{(1-j)d}{\delta_{Si}}\right)\right)\right]$$

$$L_{outer} \approx \frac{\mu}{\pi} ln\left(\frac{r_{via}+t_{OX}+\omega_{dep}}{r_{via}}\right) + \frac{\mu}{2}\cdot \tag{17}$$
$$Im\left[H_0^{(2)}\left(\frac{1-j}{\delta_{Si}}(r_{via}+t_{OX}+\omega_{dep}\right) - H_0^{(2)}\left(\frac{(1-j)d}{\delta_{Si}}\right)\right]$$

where μ is the permeability in either TSV or silicon, J_0 is the 0th order Bessel function of the first type, $H_0^{(2)}$ is the 0th order Hankel function of the second type, δ_{metal} and δ_{Si} are the damping parameters for TSV and silicon, respectively.

The results are compared with simulation results, indicating that taking the skin effect into consideration is of great importance for high frequency analysis since the higher frequency resistance is dominant.

As technology scales, the diameter and pitch of TSVs is expected to reduce. However, the substrate thickness almost remains the same as predicted by the International Technology Roadmap for Semiconductors (ITRS). When the radius of TSVs is reduced, C, G, and L do not change much due to the proportional scaling of geometrical parameters. Nevertheless, resistance increases significantly when the frequency grows from 1GH to 100GHz due to the reduced TSV cross area.

In terms of circuit performance sensitivity, capacitance has the most important impact on circuit behavior while resistance is of the least importance. The circuit exhibits the short-transmission line behavior on signal propagation, which indicates that simple RLC model is enough for delay and signal rise/fall calculation. However, the L and G are crucial factors for the estimation of voltage variations in V_{DD} and GND. More accurate whole circuit performance evaluation can only be done with all RLCG components.

2.4 Model Validation Methods

The proposed analytical models require model validation either from measurement results or well-established simulation results. In general, four validation methods are applied in the previous studies: 2D/3D electromagnetic solver [9, 12, 4, 16, 19, 10, 13]; 3D electrostatic simulator [3, 20]; vector network analyzer for frequency domain [5]; and ground-signal-ground (GSG) probing [7, 11].

3. REVIEW OF RDL AND MICRO BUMP ELECTRICAL MODELING

Although TSV is the key enabling component in 2.5D/3D structures, electrical models of other components (micro-bumps, RDLs, C4, etc.) are necessary for full chip and full package analyses. Several work have been done to model these components [17, 3, 10, 7, 13].

Among these components, RDL is the most important one to enable the submicron width and spacing for high density connection in the silicon interposer. The fabrication process of RDL is similar to the back-end-of-line (BEOL) process. There are three different types of transmission lines in RDL, namely microstrip line, stripline, and coplanar waveguide (CPW) line. The major difference rises from the relative position and orientation of signal and ground lines. These three types exhibit diverse insertion loss and return loss [7]. In general, Microstrip line and CPW line have better electrical performance and lower cost. From the performance evaluation, it is found that the dielectric layer thickness is more important than the trace width in terms of the trace impedance.

The metal trace in RDLs can be treated as traditional metal layers for signal transmission with resistance and capacitance. The theoretical values of resistance for RDL can be calculated as follows [10]:

$$R_{Th} = R_{RDL} + \frac{R_{Ground}}{2} = \alpha\frac{1}{w_{RDL} * t_{RLD}}\frac{3}{2} \tag{18}$$

where w_{RDL} and t_{RDL} are the width and the oxide thickness of the metal layers. The resistance value of BEOL can be obtained in the similar way. The capacitance of RDLs has not been deliberately studied in the previous work. However, for simplicity, we can only consider the oxide capacitance due to the dielectric layer.

Micro-bump cannot be simply treated as metal layers due to its unique geometry. In previous study [17], the micro-bump is modeled as an equivalent RLC circuit similar to the TSV modeling. This model uses the same equations that are used in TSV RC calculation. The micro-bump model contains resistance and inductance in serial along the structure from input to output port as shown in Figure 3. Two capacitances exist between micro-bump and connected tiers. One of the capacitance represents the capacitance between micro-bump and substrate of the first tier while the other captures the capacitance between micro-bump and the substrate of the second tier. However, this micro-bump model is not accurate because the geometry properties is ignored. Different from metal trace and TSVs, micro-bump is a sphere-like structure which cannot be simply treated as a transmission line or a cylinder.

Most of the previous work focus on modeling micro-bumps, RDL, and BEOL in a separate fashion, the full chip modeling and analysis with all these components has not been fully explored yet. The resistance path of TSV-RDL-bump and the corresponding insertion loss and return loss are evaluated [13]. The resistance discontinuity has great influence on the impedance and return loss. Therefore, a modified ground-shape is proposed to smooth the impedance profile.

4. 2.5D/3D INTERCONNECT COMPACT MODEL PARAMETERS

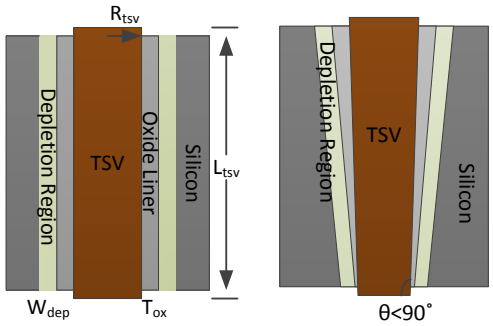
In this section, the extracted parameters are listed for both geometry and electrical modeling of interconnect components. The geometry parameters of interconnect components are one of the dominant factors in the 2.5D/3D electrical compact modeling. Most of the analytical modelings are based on the extracted geometry parameters. The commonly used extracted geometry parameters of through-silicon vias, micro-bumps, and transmission lines (RDLs and BEOLs) are given for the reference of further electrical modeling. Most of the electrical parameters are closely depended on the interconnect component materials, such as the electrical conductivity and permittivity. Both the extracted parameters used as model input and the calculated values as model output are given for circuit simulation.

4.1 Parameters of Through-Silicon Vias

The key vertical interconnect component in 2.5D/3D is through-silicon vias (TSVs). The TSV structure contains three parts: metal filling, insulator layer, and silicon substrate. Dielectric layer made from oxide material is surrounding the TSVs metal filling. Between the liner and silicon substrate, depletion region is formed due to the increased bias voltage when the bias voltage is larger than flat bend voltage. The surrounding layers of the filling metal in TSVs have great influence on the electrical behavior. Therefore, during structure extraction, these layers should also be considered and modeled.

In the ideal case, the TSVs shape can be simply extracted as cylindrical structure, which is demonstrated in Figure 4(a). Practically, considering the process variation and manufacturing limitation, real TSV should be modeled as cone structure as shown in Figure 4(b) and the assumption of this structure can be supported by the TSV SEM image from IMEC. In the cone structure, the bottom radius of TSVs is smaller than the upper radius, and the oxide layer has the similar changes (upper radius is larger) but with steeper decrement ratio. These effects are included in the process variation section. The first part of Table 1 demonstrates the TSV geometry parameters under ideal cases.

Besides the dielectric layer thickness, the trapped charges in oxide liner also influences the flat bend voltage and results in different depletion width. Due to the important role of TSVs, the electrical modeling of TSV should be accurate and sophisticated. Since in real designs, the TSV bundle that contains multiple TSVs is used for signal transmission, the coupling effect between TSVs should be carefully handled to precisely capture the circuit behavior. The second part of Table 1 lists all the electrical parameters in the model.



(a) Cylinder TSV (b) Cone TSV

Figure 4: The typical TSV structure model: (a). TSV is modeled as ideal cylinder; (b). TSV is modeled as cone considering the process limitation and variation.

4.2 Parameters of RDLs, BEOLs, and Micro-bumps

Redistribution layers (RDLs) and back-end-of-line (BEOL) can simply be treated as on-chip traditional transmission lines. The RC modeling is more applicable to on-chip interconnect than the package-level connections, such as the metal trace in PCBs. Therefore, the most important parameters include the thickness of the dielectric layer and the length of the metal layer which have impact on the resistance and capacitance as shown in Figure 6.

The extracted geometry parameters for micro-bump is similar to the TSV parameters. Since the micro-bumps are not embedded inside silicon substrate, therefore, the depletion region is not considered. Moreover, large portion of the conductor is copper post and the solder contains only small portion of height (about 1/3). Figure 5 shows the structure of micro-bumps. The geometry parameters of these three components are shown in the first part of Table 2.

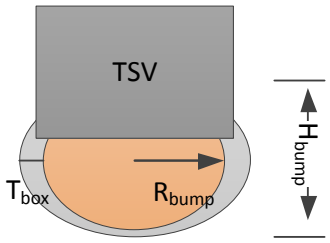


Figure 5: The structure model of micro-bumps.

Compared to TSVs, the electrical modelings of micro-bumps, RDLs, and BEOLs are relatively simpler and straight forward. Resistance and capacitance are the major factors that influence the signal transmission latency and loss, therefore, in the second part of Table 2, the electrical parameters of each component are listed.

4.3 Parameters of Process Variation

In general, the process variation affects the interconnect electrical characteristic through changing the geometry parameters. For example, the electrical modelings of TSV in cylindrical and cone structure are totally different. Moreover, due to the mechanical stress and fabrication process, the micro-bump is more similar to cubic than the ideal sphere.

Table 1: TSV geometry and electrical parameters list.

Category	Parameters	Description	Note
Geometry	L_{TSV}	TSV length	Typical aspect ratio: 1/20 - 1/4 [1]
	R_{TSV}	TSV radius	
	T_{tox}	TSV liner layer thickness	
	W_{dep}	TSV silicon depletion width	Depend on bias voltage
	D_{TSV}	Distance between two TSVs	Parameter for coupling effects
Electrical	σ_{TSV}	TSV conductivity	material related
	ε_{ox}	Oxide liner permittivity	
	ε_{Si}	Silicon permittivity	
	μ_0	Free space permeability	default value $4\pi \cdot 10^{-7} H/m$
	Q_{trap}	Trapped charges in the oxide liner	charges are between silicon and liner
	V_{tsv}	Voltage between TSV and bulk silicon	bias voltage
Models	R_t	TSV resistance	
	C_{dep}	TSV depletion capacitance	
	C_{ox}	TSV oxide capacitance	
	C_{TSV}	TSV capacitance	the serial capacitance of C_{ox} and C_{dep}
	L_t	TSV inductance	
	C_c	Coupling capacitance	coupling effect with more than two TSVs
	L_c	Coupling inductance	
	V_{FB}	TSV flat bend voltage	
	V_{th}	TSV threshold voltage	

Table 2: RDLs, BEOLs, and micro-bumps geometry and electrical parameters list.

Category	Parameters	Description	Note
Geometry	R_{bump}	Micro Bump radius	Micro bump structure extracted as cylinder
	H_{bump}	Micro Bump height	
	T_{box}	Oxide liner thickness	
	L_{line}	Length of transmission lines	influence the resistance
	W_{line}	Width of transmission lines	
	T_{lox}	Oxide thickness of transmission lines	
	L_{type}	The type of transmission line	influence the impedance behavior
	C_{shape}	Connection shape between line and TSVs	
Electrical	R_s	Sheet resistance of transmission lines	material related parameter
	ε_{ins}	Liner permittivity for lines and micro bump	
	σ_{bump}	Micro bump filling conductivity	
Models	C_{bump} / C_{lines}	Component capacitance	$C_{bump} = \frac{2\pi\varepsilon_{ins}H_{bump}}{ln\left(1+\frac{T_{box}}{R_{bump}}\right)}$
	R_b	Micro-bump resistance	$R_b = \frac{H_{bump}}{\sigma_{bump}\pi R_{bump}^2}$
	R_{lines}	Transmission line resistance	$R_{lines} = \frac{R_s L_{lines}}{W_{lines}}$

Table 3: Process variation related parameters list.

Parameters	Description	Note
R_{TSV}^m	Minimum TSV radius as cone	Variation in the TSV structure
T_{box}^m	Minimum oxide liner thickness	
R_{bump}^m	Maximum micro-bump radius under stresses	Variation in the micro-bump structure
H_{bump}^m	Minimum micro-bump height under stresses	

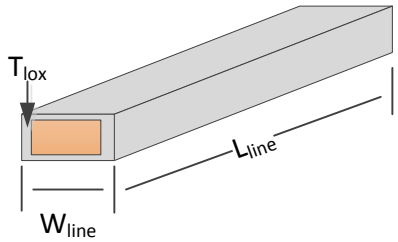


Figure 6: The structure model of transmission lines.

In addition to the geometry variations, electrical parameters are also under influence of the process variation, such as the impurity in silicon substrate. Nevertheless, these impacts can be captured with the previous listed electrical parameters. Due to the various process steps and manufacturing limitations, the major geometry differences are listed in Table 3.

5. CONCLUSION AND FUTURE WORK

Previous work of 2.5D/3D electrical modeling and validation methods are reviewed and summarized in this paper. The corresponding standard electrical model containing both geometry and electrical parameters is extracted from these previous work. This compact model standard is intended to promote the EDA tool development in 3D IC designs and the design format exchanges between different vendors and designers. Future adoption and integration of this model into existing EDA tools are remained to be explored.

6. ACKNOWLEDGEMENT

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