Yuan Xie

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Education

2002	**Princeton University** Ph.D. in Electrical Engineering	**Princeton, NJ**
1999	**Princeton University** M.S. in Electrical Engineering	**Princeton, NJ**
1997	**Tsinghua University** B.S in Electronic Engineering	**Beijing, P.R.China**

Professional Experience

2014 - now	**University of California at Santa Barbara** Professor in the Department of Electrical and Computer Engineering	**Santa Barbara, CA**
2003 - 2014	**Pennsylvania State University** Assistant/Associate/Full Professor in the Department of Computer Science Engineering	**University Park, PA**
2012 - 2013	**AMD Research Lab** Senior Manager and Principal Researcher	**Beijing, China**
05-07/2010	**IMEC (Interuniversity Microelectronics Centre)** Visiting Researcher, collaborated on 3D IC design research	**Leuven, Belgium**
2002 - 2003	**IBM Microelectronic Division** Advisory Engineer in Worldwide Design Center	**Essex Juction, Vermont**

Research Summary

Yuan Xie has published 3 books,60+ journals, and more than 200 refereed conference papers in the areas of *VLSI design, EDA, computer architecture, embedded systems*, with a focus on design automation and novel circuits/architectures for three-dimensional IC Design (3D ICs), emerging memory technologies, low power and thermal-aware design, system-level synthesis and high-level synthesis for embedded systems. He has graduated 23 Ph.D. students and is currently supervising 9 Ph.D. graduates. He has served as PI/Co-PI on 19 research grants administered by US Federal agencies (including National Science Foundation, DoE, and DARPA) and 18 research grants from industry, with total amount of $15.1 million and personal share of $6.3 million. These projects have resulted in the design of new CAD tools and optimizations, and novel architectures for emerging technologies such as 3D ICs and emerging memory technologies. He has received Best Paper Awards (HPCA 2015, ICCAD 2014, GLSVLSI 2014, ISVLSI 2012, ISLPED 2011, ASP-DAC 2008, ASICON 2001) with several Best Paper Nominations(ASP-DAC 2014, MICRO 2013, DATE 2013, ASPDAC 2010-2009, ICCAD 2006). Through extensive collaboration with industry partners (AMD, HP, Honda, IBM, Intel, IMEC, Qualcomm, Seagate, Toyota etc.), he has helped the transition of research ideas to industry.

Service Summary

Yuan Xie has been an active volunteer in the design automation, VLSI and computer architecture conferences. He served as TPC chair for MPSOC 2011, ASPDAC 2013, ISLPED 2013, and served as program committee member, track chair for leading conferences in these areas, including top EDA conferences such as DAC, ICCAD, ASP-DAC, and DATE, and top architecture conferences such as ISCA and HPCA. Currently he serves as a committee member in IEEE Design Automation Technical Committee (DATC), and serves as the Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, ACM Journal of Emerging Technologies in Computing Systems, IEEE Design and Test of Computers, and IET Computers and Design Techniques. He has given 17 tutorials in prestigious conferences and 60+ invited talks in industry/academia.

Awards and Honors

2017	ASP-DAC 2017 Best Paper Award Nomination (Paper [C2])
2016	IEEE MICRO **Top Picks**(Paper [J1])
2016	Inducted to ISCA (Intl. Symp. on Computer Architecture) Hall Of Fames
2015	Inducted to HPCA (Intl. Conf. on High Performance Computer Architecture) Hall Of Fames
2015	Intl.Symp. on High-performance Computer Architecture (HPCA) **Best Paper Award**. (Paper [C34])

2015 **IEEE Fellow** (class of 2015) for contributions in design automation and architecture for 3D ICs.
2014 ICCAD IEEE/ACM William J. McCalla ICCAD **Best Paper Award**. (Paper [C41])
2014 ACM Student Research Competition Silver Medal by advisee Ping Chi (ICCAD 2014)
2014 GLSVLSI 2014 **Best Paper Award** (Paper [C55])
2014 ASP-DAC 2014 Best Paper Award Nomination (Paper [C62])
2013 MICRO 2013 Best Paper Award Honorable Mention (Paper [C66])
2013 ACM/IEEE Design Automation and Test in Europe (DATE) 2013, Best Paper Nomination(Paper [C72])
2012 European Design Automation Association, Outstanding Dissertation Award by advisee Guangyu Sun
2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2012, Best Paper Award(Paper [C79])
2011 ACM/IEEE International Symposium on Low Power Electronics 2012, Best Paper Award(Paper [C96])
2011 ACM Student Research Competition Grand Finals by advisee Xiangyu Dong
2010 Overseas and Hong Kong, Macau Scholars Collaborative Research Award by China NSF
2010- Association for Computing Machinery(ACM) Distinguished Speaker
2010-13 IEEE Computer Society Distinguished Visitor
2010 ASP-DAC 2010 Best Paper Award Nomination (Paper [C127])
2009 Selected as one of the 7 overseas scholars in "Dragon Star" Program supported by China NSF.
2009 Penn State Engineering Society Outstanding Research Award Nomination, Penn State
2009 ASP-DAC 2009 Best Paper Award Nomination (Paper [C141])
2008 IBM Faculty Award
2008 ASP-DAC 2008 Best Paper Award (Paper [C155])
2008 Department Faculty Teaching Award, Computer Science and Engineering Department
2007 Outstanding Teaching Award Nomination, College of Engineering, Penn State
2006 **National Science Foundation Faculty Early Career Development (CAREER) Award.**
2006 Chun-Hui Outstanding Overseas Scholar Award, Chinese Ministry of Education
2006 ICCAD 2006 Best Paper Award Nomination (Paper [C170]).
2002 SRC(Semiconductor Research Corporations) Inventor Recognition Award.
2001 International Conference on ASICs, Best Paper Award (Paper [C216]).

Journal Publications

[J1]. Kaisheng Ma, Xueqing Li, Karthik Swaminathan, Yang Zheng, Shuangchen Li, Yongpan Liu, Yuan Xie, John Jack Sampson, Vijaykrishnan Narayanan. "Nonvolatile Processor Architectures: Efficient, Reliable Progress with Unstable Power." **IEEE MICRO Top Picks,**, May/June 2016.

[J2]. Cong Xu, Dimin Niu, Shimeng Yu, Yuan Xie. " Impact of Write Pulse and Process Variation on 22nm FinFET-Based STT-RAM Design: A Device-Architecture Co-Optimization Approach." To appear in *IEEE Transactions on Multi-Scale Computing Systems.*, 2016.

[J3]. Jia Zhan, Fen Ge, Jin Ouyang, Jishen Zhao, Yuan Xie. " Hybrid Drowsy SRAM and STT-RAM Buffer Designs for Dark Silicon Aware NoC." *IEEE Transactions on VLSI (TVLSI).*, pp.3041 - 3054, Vol.24, No.10, 2016.

[J4]. Chao Wang; Lei Gong; Qi Yu; Xi Li; Yuan Xie; Xuehai Zhou. "DLAU: A Scalable Deep Learning Accelerator Unit on FPGA." To appear in *IEEE Transactions on Computer-Aided Designs (TCAD).*, 2016.

[J5]. Ping Chi, Wang-Chien Lee, Yuan Xie. " Adapting B-plus Tree for Emerging Nov-volatile Memory Based Main Memory." To appear in *IEEE Transactions on Computer-Aided Designs (TCAD).*, 2016.

[J6]. Guoqing Chen, Yi Xu, Xing Hu, Xiangyang Guo, Jun Ma, Yu Hu, and Yuan Xie. "TSOCKET: Thermal Sustainable Power Budgeting." To appear in *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol.xx, No.xx, Article xx, 2016.

[J7]. Cong Xu, Dimin Niu, Shimeng Yu, Yuan Xie. "Impact of Cell Failure on Reliable Cross-point Resistive Memory." *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol.20, No. 4, Article 63, September 2015.

[J8]. Matt Poremba, Tao Zhang, Yuan Xie. "NVMain 2.0: Architectural Simulator to Model (Non-)Volatile Memory Systems." *IEEE Computer Architecture Letters*,Vol.14, No.2, pp140-143, July-December, 2015.

[J9]. Hsiang-yun Cheng, Mary Jane Irwin, Yuan Xie. " Adaptive Burst-Writes (ABW): Memory Requests Scheduling to Reduce Write-Induced Interference." *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol.21, No. 1, Article 7, November 2015.

[J10]. Kaisheng Ma, Xueqing Li, Shuangchen Li, Yongpan Liu, John Jack Sampson, Yuan Xie, Vijaykrishnan Narayanan. "Nonvolatile Processor Architecture Exploration for Energy-Harvesting Applications." *IEEE Micro*, Issue No. 05, vol. 35, pp.32-40, Sept./Oct., 2015.

[J11]. Hsiang-yun Cheng, Matt Poremba, Narges Shahidi, Ivan Stalev, Mary Jane Irwin, Mahmut Kandemir, Jack Sampson, Yuan Xie. "EECache: A Comprehensive Study on the Architectural Design for Energy-Efficient Last-Level Caches in Chip

Multiprocessors." *ACM Transactions on Architecture and Code Optimization (TACO), Vol.12, No.2, Article 17, July 2015, 22 pages.*

[J12]. Jishen Zhao, Sheng Li, Jichuan Chang, John L. Byrne, Laura L. Ramirez, Kevin Lim, Yuan Xie, and Paolo Faraboschi. "Buri: Scaling Big-memory Computing with Hardware-based Memory Expansion." *ACM Transactions on Architecture and Code Optimization (TACO), Vol.12, No.3, Article 31 (October 2015), 24 pages.*

[J13]. Jue Wang and Yuan Xie. "A Write-Aware STTRAM-Based Register File Architecture for GPGPU." *ACM Journal on Emerging Technologies in Computing Systems(JETC)*,Volume 12, No.1, Article 6 (July, 2015)

[J14]. Jishen Zhao, Cong Xu, Ping Chi, Yuan Xie. "Memory and Storage System Design with Nonvolatile Memory Technologies." *IPSJ Transactions on System LSI Design Methodology*, Vol. 8, pp.2-11, 2/2015.

[J15]. Jue Wang, Xiangyu Dong, Yuan Xie. "Building and Optimizing MRAM-Based Commodity Memories." *ACM Transactions on Architecture and Code Optimization (TACO)*, Volume 11, No.4, Article 36 (December 2014), 22 pages.

[J16]. Jue Wang, Xiangyu Dong, Yuan Xie. "Preventing STT-RAM Last-Level Caches from Port Obstruction." *ACM Transactions on Architecture and Code Optimization (TACO)*,Volume 11, No.3, Article 23 (October 2014), 19 pages

[J17]. Jing Xie, Yang Du, and Yuan Xie. " Testable cross-power domain interface (CPDI) circuit design in monolithic 3D technology. ." *ACM Journal on Emerging Technologies in Computing Systems(JETC)*,Volume 11, No.1, Article 5 (Sept 2014), 17 pages

[J18]. Jue Wang, Xiangyu Dong, Yuan Xie and Norman P. Jouppi. "Endurance-aware cache line management for non-volatile caches." *ACM Transactions on Architecture and Code Optimization (TACO)*,Volume 11, No.1, Article 24 (February 2014), 25 pages.

[J19]. Jia Zhan, N. Stoimenov, Jin Ouyang, L. Thiele, V. Narayanan, Yuan Xie . "Optimizing the NoC Slack Through Voltage and Frequency Scaling in Hard Real-Time Embedded Systems" *IEEE Transactions on Computer Aids Design (TCAD).*, pp.1632-1643, Vol. 33, No. 11, Nov. 2014.

[J20]. Wujie Wen, Y. Zhang, Yiran Chen, Yu Wang, Yuan Xie . "PS3-RAM: A Fast Portable and Scalable Statistical STT-RAM Reliability/Energy Analysis Method" *IEEE Transactions on Computer Aids Design (TCAD).*, pp.1644-1656, Vol. 33, No. 11, Nov. 2014.

[J21]. Wulong Liu, Guoqing Chen, Yu Wang, Xue Feng, Yuan Xie, Yidong Huang, Huangzhong Yang. "Exploration of Electrical and Novel Optical Chip-to-Chip Interconnects" *IEEE Design and Test*, pp.28-35, Vol. 31, No.5, Sept/Oct, 2014.

[J22]. Wulong Liu, Yu Wang, Yuchun Man, Huangzhong Yang, Yuan Xie. "Whitespace-Aware TSV Arrangement in 3-D Clock Tree Synthesis" To appear in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2014.

[J23]. Wulong Liu, Yu Wang, Yuchun Man, Huangzhong Yang, Yuan Xie. "On-Chip Hybrid Power Supply System for Wireless Sensor Nodes" *ACM Journal of Emerging Technologies in Computing Systems (JETC).*, Vol.10, No.3, Article. 23, April, 2014.

[J24]. Xiangyu Dong, Norm Jouppi, Yuan Xie. "A Circuit-Architecture Co-optimization Framework for Exploring Nonvolatile Memory Hierarchies." *ACM Transactions on Architecture and Code Optimization (TACO), Vol. 10, No. 4, 12/2013*

[J25]. Zhe Wang, Shuchang Shan, Ting Cao, Junli Gu, Yi Xu, Yuan Xie, Daniel Jimenez. "WADE: Writeback-Aware Dynamic Cache Management for NVM-based Main Memory System." *ACM Transactions on Architecture and Code Optimization (TACO) Vol. 10, No. 4, Article 51 (December 2013), 21 pages.*

[J26]. Xiaoming Chen, Yu Wang, Yu Cao, Yuan Xie, Huazhong Yang. "Assessment of Circuit Optimization Techniques under NBTI." *IEEE Computer Design and Test*, vol.30, no.6, pp.40-49, Dec. 2013

[J27]. Jishen Zhao, Guangyu Sun, Gabriel Loh, Yuan Xie. "Optimizing GPU Energy Efficiency with In-Package Graphics Memory and Reconfigurable Memory Interface." *ACM Transactions on Architecture and Code Optimization (TACO), Vol. 10, No. 4, 12/2013*

[J28]. Yibo Chen, Eren Kursun, Dave Motschman, Charles Johnson, Yuan Xie. "Through Silicon Via aware Design Planning for Thermally-efficient 3D Integrated Circuits " *IEEE Transactions on Computer Aids Design (TCAD).*, pp.1335-1346, Vol. 32, No. 9, Sept. 2013.

[J29]. Xiaoming Chen Hong Luo Yu Wang Yu Cao Yuan Xie Yuchun Ma Huazhong Yang. "Evaluation and mitigation of performance degradation under random telegraph noise for digital circuits " *IET Circuits, Devices and Systems.* pp.273-282, Vol. 7, No. 5, Sept. 2013.

[J30]. Xiangyu Dong, Cong Xu, Yuan Xie, Norm Jouppi. "NVSim: A Circuit-Level Performance, Energy, and Area Model for Emerging Non-Volatile Memory" *IEEE Transactions on Computer Aids Design (TCAD).*, pp.994 - 1007, Vol.31 , No.7, July,

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[J33]. Guangyu Sun, Huazhong Yang, and Yuan Xie. "Performance/Thermal Aware Design of 3D Stacked L2 Caches for CMPs." *ACM Transactions on Design Automation of Electronic Systems.*,Vol. 17 No. 2, April 2012

[J34]. Yu Wang, Hong Luo, Ku He, Rong Luo, Huanzhong Yang, Yuan Xie. "Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation." *IEEE Transactions on Dependable and Secure Computing (TDCS).*, Vol.8, No.5, pp.756-769. Sept.-Oct., 2011.

[J35]. Xiangyu Dong, Yuan Xie, Naveen Muralimanohar, Norm Jouppi. "Hybrid Checkpointing using Emerging Non-Volatile Memories for Future Exascale Systems." *ACM Transactions on Architecture and Code Optimization (TACO), Vol.8, No. 2, Article 5, 29 pages, July 2011*

[J36]. Vinay Saripalli, Guangyu Sun, Asit Mishra, Yuan Xie, Suman Datta, Vijaykrishnan Narayanan. "Exploiting Heterogeneity for Energy Efficiency in Chip Multiprocessors." *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*,Vol.1, No.2, pp.109-119, June 2011

[J37]. Xiangyu Dong, Xiaoxia Wu, Yuan Xie, Yiran Chen, Hai Li. "Stacking MRAM atop Microprocessors: An Architecture-Level Evaluation." *IET Computers and Digital Techniques (IET CDT), Vo.5, No.3, pp.213-220, June 2011*

[J38]. Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang. "Leakage Power and Circuit Aging Optimization by Gate Replacement Techniques." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI).* Vol. 19, No. 4, pp. 615-628, April. 2011.

[J39]. Yuan Xie. "Modeling, Architecture, and Applications for Emerging Non-volatile Memory Technologies." *IEEE Computer Design and Test*, Vol.28, No.1, pp.44-51, January 2011

[J40]. Xiaoxia Wu, Wei Zhao, Chandra Nimmagadda, Durodami Lisk, Mark Nakamoto, Sam Gu, Riko Radojcic, Matt Nowak, and Yuan Xie. "Electrical Characterization for Inter-tier Connections and Timing Analysis for 3D ICs." *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, pp.186-191, Vol. 20, No. 1, 2012.

[J41]. Shengqi Yang, Pallav Gupta, Marilyn Wolf, Dimitrios Serpanos, Yuan Xie, N. Vijaykrishnan. "Power Analysis Attack Resistance Engineering by Dynamic Voltage and Frequency Scaling." *ACM Transactions in Embedded Computing Systems (TECS)*, Vol. 11, No. 3, Sept. 2012.

[J42]. Feng Wang, Yibo Chen, Xiaoxia Wu, C. Nicopoulos, Yuan Xie, N. Vijaykrishnan. "Variation-aware Task Allocation and Scheduling for MPSoC." *IEEE Transactions on CAD (TCAD), Vol 30, No.2, pp. 259-307, 2011*

[J43]. Feng Wang and Yuan Xie. "SER Analysis for Combinational Logic Using an Accurate Electrical Masking Model." *IEEE Transactions on Dependable and Secure Computing (TDCS). Vol. 8, No. 1, 2011, pp.137-146.*

[J44]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. "Hybrid Cache Architecture with Disparate Memory Technologies." *ACM Transactions on Architecture and Code Optimization (TACO).* Vol. 7, No. 3, December 2010.

[J45]. Xiangyu Dong, Jishen Zhao, Yuan Xie. "Cost Analysis and Cost-driven Design for 3D ICs." *IEEE Transactions on CAD (TCAD), Vol 29, No. 12, pp. 1959-1972, Dec. 2010.*

[J46]. Yiran Chen, Hai Li, Cheng-Kok Koh, Guangyu Sun, Jing Li, Yuan Xie, and Kaushik Roy. "Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance." *IEEE Transactions on VLSI (TVLSI), Vol 18, No. 11, pp. 1621-1624, Nov. 2010.*

[J47]. Xiaoxia Wu, Yibo Chen, Krishnendu Chakrabarty, Yuan Xie. "Test-access mechanism optimization for core-based three-dimensional SOCs." *Microelectronics Journal, Volume 41 Issue 10, pp. 601-615, Oct. 2010*

[J48]. Gabe Loh, Yuan Xie. "3D Stacked Microprocessor: Are We There Yet?" *IEEE Micro, Volume 30 Issue 3, pp. 60-64, May. 2010*

[J49]. Wei-lun Hung, Yuan Xie, Narayanan Vijaykrishnan, Mahmut Kandemir, and Mary Jane Irwin. "Total Power Optimization for Combinational Logics Using Genetic Algorithms." *Journal of VLSI Signal Processing. Vol. 58, No. 2, pp.145-160, Feb. 2010.*

[J50]. Hong Luo, Yu Wang, Rong Luo, Huazhong Yang, Yuan Xie. "Temperature-aware NBTI Modeling Techniques in Digital Circuits." *IEICE Transactions on Electronics.*, No. 6, pp. 875-886, 2009

[J51]. Yuan Xie and Yibo Chen. "Statistical High Level Synthesis Considering Process Variations." *IEEE Computer Design and Test, Special Issue on HLS*, Vol. 26, Issue 4, pp.78-87, July-August, 2009

[J52]. Xiaoxia Wu, Paul Falkenstern, Krishnendu Chakrabarty, Yuan Xie. "Scan-chain design and optimization for three-dimensional integrated circuits." *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 5, Issue 2, pp.1-26, July, 2009

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[J55]. R. Rajaraman, V. Degalahal, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin. "Modeling Soft Errors at Device and Logic Level for Combinational Circuits." *IEEE Transactions on Dependable and Secure Computing (TDCS).*, Vol. 6, No. 3, pp.202-216, June 2009.

[J56]. C. Celik, K.Unlu, K. Ramakrishnan, R. Rajaraman, N. Vijaykrishnan, M. J. Irwin, Y. Xie. "Thermal Neutron Induced Soft Error Rate Measurement in Semiconductor Memories and Circuits." *Journal of Radioanalytical and Nuclear Chemistry.*, Vol. 278, No.2, pp.509-512, Nov 2008.

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[J60]. Chang-hong Lin, Yuan Xie, and W.Wolf. "Code Compression for VLIW Embedded Systems Using a Self-Generating Table." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 15. No. 10.*,pp.1160-1171, Oct. 2007

[J61]. Feng Wang, Mike Debole, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *IET Computer and Digital Techniques, Vol. 1, No. 5.*, pp.590-599, 2007.

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[J63]. Gabriel Loh, Yuan Xie, and Bryan Black. "Processor Design in Three-Dimensional Die-Stacking Technologies." *IEEE Micro, Vol. 27. No. 3*, pp.31-48, May/June 2007.

[J64]. Yuan Xie, Lin Li, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. "Reliability-Aware Co-synthesis for Embedded Systems." *Journal of VLSI Signal Processing, Vol. 49, No.10*, pp.87-99, March 2007.

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[J66]. Yuan Xie, Gabriel Loh, Bryan Black, and Kerry Bernstein. " Design Space Exploration for 3D Architecture." *ACM Journal of Emerging Technologies for Computer Systems, Vol. 2. No. 2*, pp.65-103, April 2006.

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[J68]. Yuan Xie, W.Wolf, and H. Lekatsas. " Code Compression Using Variable-to-fixed Coding." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 14. No. 5*, pp.525-536, January. 2006.

[J69]. Yuan Xie, Jiang Xu, W.Wolf. " Augmenting Platform-based Design with Synthesis Tools." *Journal of Circuits, Systems and Computers, Vol. 14. No. 5*, pp.525-536, April. 2003.

Book

[1]. Yuan Xie and Jishen Zhao "Die-Stacking Architecture." *Morgan Claypool Publishers. 2015*

[2]. Yuan Xie "Emerging Memory Technologies: Design, Architecture, and Applications." *Springer. 2013*

[3]. Yuan Xie, Jason Cong, Sachin Sapatnekar. "Three-dimensional IC: Design, CAD, and Architecture." *Springer. 2009*

Book Chapters

[1]. Jia Zhan and Yuan Xie. "NoC-aware Computational Sprinting." *The Dark Side of Silicon— Energy Efficient Computing in the Dark Silicon Era, Edited by Rahmani, A.M., Liljeberg, P., Hemani, A., Jantsch, A., Tenhunen, H, Published by Springer. 2017*

[2]. Yuan Xie and Qiaosha Zou. "3D Integration Technology." *More than Moore Technologies for Next Generation Computer Design. pp 23-48, Edited by Rasit Topaloglu, Springer. 2015*

[3]. Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan. "Thermal-aware 3D IC Designs." *3D Integration of Integrated Circuits. Edited by C. S. Tan, K. N. Chen and S. J. Koester, Pan Stanford Publishing Ltd. 2011*

[4]. Yuan Xie, N. Vijaykrishnan, Chita Das. "3D Network-on-chip Architecture." *Three-dimensional IC: Design, CAD, and Architecture. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. Springer. 2009.*

[5]. Yuan Xie, Xiangyu Dong. "System-level Cost Analsysis and Design Exploration for 3D ICs." *Three-dimensional IC: Design, CAD, and Architecture. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. Springer. 2009.*

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Refereed Conference Publications

[C1]. Maohua Zhu, Chao Wang, Youwei Zhuo, Wenguang Chen, Yuan Xie. "Performance Evaluation and Optimization of HBM-Enabled GPU for Data-intensive Applications." *Proceedings of IEEE/ACM Design Automation and Test in Europe (DATE), 2017.*

[C2]. Kaisheng Ma, Xueqing Li, Srivatsa Rangachar Srinivasa, Yongpan Liu, John (Jack) Sampson, Yuan Xie, Vijaykrishnan Narayanan. "Spendthrift: Machine Learning Based Resource and Frequency Scaling for Ambient Energy Harvesting Nonvolatile Processors." *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017.* **(Best Paper Candidate)**

[C3]. Liu Liu, Ping Chi, Shuangchen Li, Yuanqing Cheng, Yuan Xie . "Building Energy-Efficient Multi-Level Cell STT-RAM Caches with Data Compression." *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017.*

[C4]. Wenqin Huangfu, Lixue Xia, Ming Cheng, Xiling Yin, Tianqi Tang, Boxun Li, Krishnendu Chakrabarty, Yuan Xie, Yu Wang, Huazhong Yang . "Computation-Oriented Fault-Tolerance Schemes for RRAM Computing Systems." *Proceedings of IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2017.*

[C5]. Jia Zhan, Itir Akgun, Jishen Zhao, and Yuan Xie. "A Unified Memory Network Architecture for In-Memory Computing in Commodity Servers." *Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO), 2016.*

[C6]. Jia Zhan, Onur, Chita Das, Gabe Loh, and Yuan Xie. "OSCAR: Orchestrating STT-RAM Cache Traffic for Heterogeneous CPU-GPU Architectures." *Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO), 2016.*

[C7]. Yu Ji, Youhui Zhang, Ping Chi, Shuangchen Li, Peng Qu, Wenguang Chen, and Yuan Xie. "NEUTRAMS: Neural Network Transformation and Co-design under Neuromorphic Hardware Constraints." *Proceedings of IEEE/ACM International Symposium on Microarchitecture (MICRO), 2016.*

[C8]. Dylan Stow, Itir Akgun, Russell Barnes, Peng Gu, and Yuan Xie. "Cost Analysis and Cost-Driven IP Reuse Methodology for SoC Design Based on 2.5D/3D Integration." *Proceedings of IEEE/ACM International Conference on CAD (ICCAD), 2016.*

[C9]. Linuo Xue, Yuanqing Cheng, Jianlei Yang, and Yuan Xie. "ODESY: A novel 3T-3MTJ cell design for STT-RAM with Optimized DEnsity, Scalability and latencY." *Proceedings of IEEE/ACM International Conference on CAD (ICCAD), 2016.*

[C10]. Shuangchen Li, Liu Liu, Peng Gu, Cong Xu and Yuan Xie. "NVsim-CAM: A Circuit-Level Simulator for Emerging Nonvolatile based Context-Addressable Memory." *Proceedings of IEEE/ACM International Conference on CAD (ICCAD), 2016.*

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[C123]. Xiaoxia Wu, Guangyu Sun, Reetuparna Das, Yuan Xie, Jian Li, Chita R. Das "Cost-driven 3D Integration with Interconnect Layers." *Proceedings of Design Automation Conference (DAC). 2010. pp.150-155.* (24% acceptance rate).

[C124]. Yongsoo Joo, Dimin Niu, Guangyu Sun, Xiangyu Dong, Yuan Xie "Energy- and Endurance-Aware Design of Phase Change Memory Caches." *Proceedings of Design Automation and Test in Europe (DATE). 2010. pp.136-141.* (25% acceptance rate).

[C125]. Guangyu Sun, Yongsoo Joo, Yibo Chen, Yuan Xie, Yiran Chen, Helen Li "A Hybrid Solid-State Storage Architecture for Performance, Energy Consumption and Lifetime Improvement." *Proceedings of High Performance Computer Architecture (HPCA). 2010.* (18% acceptance rate).

[C126]. Yuan Xie "Processor Architecture Design Using 3D Integration Technology.(Invited Paper)" *Proceedings of VLSI Design. 2010.*

[C127]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach "Parametric Yield Driven Resource Binding in Behavioral Synthesis with Multi-Vth/Vdd Library." *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010. pp.781-786.* (33% acceptance rate(115/340)) (**Best Paper Nomination**).

[C128]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach "Minimizing Leakage Power in Aging-Bounded High-level Synthesis with Design Time Multi-Vth Assignment." *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC).*

2010. pp.689-694. (33% acceptance rate(115/340)).

[C129]. Dimin Niu, Yibo Chen, Xiangyu Dong, Yuan Xie "Energy and Performance Driven Circuit Design for Emerging Phase-Change Memory." *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010.* (33% acceptance rate(115/340)).

[C130]. Paul Falkstern, Yao-wen Chang, Yuan Xie, Yu Wang "Three Dimensional Integrated Circuit (3D IC) Floorplan and Power/Ground Network Co-synthesis." *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010.* (33% acceptance rate(115/340)).

[C131]. Xiangyu Dong, Naveen Muralimanohar, Norm Jouppi, Richard Kaufmann, Yuan Xie "Leveraging 3D PCRAM Technologies to Reduce Checkpoint Overhead for Future Exascale Systems." *Proceedings of International Conference on High Performance Computing, Networking, Storage and Analysis (SC). 2009.* (22% acceptance rate(59/261)).

[C132]. Xiangyu Dong, Norm Jouppi, Yuan Xie "PCRAMsim: System-Level Performance, Energy, and Area Modeling for Phase-Change RAM." *Proceedings of International Conference on Computer-Aided Design (ICCAD). 2009. pp 269-275.* (26% acceptance rate(115/438)).

[C133]. Balaji Vaidyanathan, Anthony S. Oates, Yuan Xie "Intrinsic NBTI-Variability Aware Statistical Pipeline Performance Assessment and Tuning." *Proceedings of International Conference on Computer-Aided Design (ICCAD). 2009. pp 164-171.* (26% acceptance rate(115/438)).

[C134]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. "Hybrid Cache Architecture with Disparate Memory Technologies." *Proceedings of International Symposium on Computer Architecture (ISCA)*, pp.34-45, June. 2009.

[C135]. Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang. "Gate Replacement Techniques for Simultaneous Leakage and Aging Optimization." *Proceedings of Design Automation and Test in Europe (DATE)*, pp. 324-333. April. 2009.

[C136]. Balaji Vaidyanathan, Anthony Oates, Yuan Xie, Yu Wang. "NBTI-Aware Statistical Circuit Delay Assessment." *Proceedings of Intl. Symp. on Quality Electronics Device (ISQED)*, March. 2009.

[C137]. Yu Wang, Xiaoming Chen, Wenping Wang, Varsha Balakrishnan, Yu Cao, Yuan Xie, Huazhong Yang. "On the efficacy of Input Vector Control to mitigate NBTI effects and leakage power." *Proceedings of Intl. Symp. on Quality Electronics Device (ISQED)*, March. 2009.

[C138]. Luca P. Carloni, Partha Pande, and Yuan Xie . "Networks-on-chip in emerging interconnect paradigms: Advantages and challenges." *Proceedings of 3rd ACM/IEEE Intl. Symp. on Networks-on-chip*, pp. 93-102. May. 2009.

[C139]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. "Power and Performance of Read-write aware hybrid caches with non-volatile memories." *Proceedings of Design Automation and Test in Europe (DATE)*, pp. 737-742. April. 2009.

[C140]. Guangyu Sun, Xiangyu Dong, Yuan Xie, Jian Li, Yiran Chen. "A Novel MRAM Stacking Architecture for Chip-multiprocessors (CMP)." *Proceedings of High Performance Computer Architecture (HPCA)*, pp. 239-249. Feb. 2009. *(19% acceptance rate(34/185)).*

[C141]. Xiangyu Dong and Yuan Xie. "System-level Cost Analysis and Design Exploration for 3D ICs." *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. **Best Paper Award Nomination.** *(32% acceptance rate(116/355)).*

[C142]. Mike Debole, Guangyu Sun, Yuan Xie, Vijaykrishnan Narayanan "A Criticality-Driven Microarchitectural Three Dimensional (3D) Floorplanner." *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. *(32% acceptance rate(116/355)).*

[C143]. Feng Wang, Andres Takach, and Yuan Xie. "Variation-Aware Resource Sharing and Binding in Behavioral Synthesis." *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. *(32% acceptance rate(116/355)).*

[C144]. Yibo Chen and Yuan Xie. "Tolerating Process Variations in High-Level Synthesis Using Transparent Latches." *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. *(32% acceptance rate(116/355)).*

[C145]. Mike Debole, Wenping Wang, Yu Wang, Yuan Xie, Vijay Nayaranan, Yu Cao. "A Framework for Estimating NBTI Degradation of Microarchitectural Components" *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. *(32% acceptance rate(116/355)).*

[C146]. P. Mangalagiri, S. Bae, R. Krishnan, Yuan Xie, N. Vijaykrishnan. "Thermal-Aware Reliability Analysis for Platform FPGAs " *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp. 722-727, Nov. 2008. *(122 out of 458 submissions, 27% acceptance rate).*

[C147]. Xiaoxia Wu, Yibo Chen, Krish Chakrabarty, and Yuan Xie. " Test-Access Mechanism Optimization for Core-Based Three-Dimensional SOCs." *Proceedings of International Conference on Computer Design (ICCD)*, pp.212-218 Oct. 2008.

[C148]. Yibo Chen, Feng Wang, Yuan Xie "ILP-based Scheme for Timing Variation-aware Scheduling and Resource Binding" *Proceedings of System-on-Chip Conference*, pp.27-30, Sept. 2008.

[C149]. Jin Ouyang, Yuan Xie "Power Optimization for FinFET-based Circuits Using Genetic Algorithms" *Proceedings of System-on-Chip Conference*, pp. 211-214, Sept. 2008.

[C150]. Dongkook Park, Soumya Eachempati, Reetuparna Das, Asit K. Mishra, Yuan Xie, N. Vijaykrishnan, Chita R. Das "MIRA: A Multi-Layered On-Chip Interconnect Router Architecture" *Proceedings of International Symopsium on Computer Architecture (ISCA)*, June. 2008. (37 out of 259 submissions, 14% acceptance rate)

[C151]. Xiangyu Dong, Xiaoxia Wu, Guangyu Sun, Yuan Xie, Helen Li, Yiran Chen "Circuit and Microarchitecture Evaluation of 3D Stacking Magnetic RAM (MRAM) as a Universal Memory" *Proceedings of Design Automation Conference (DAC)*, pp.554-559, June. 2008. (138 out of 639 submissions, 21% acceptance rate)

[C152]. Hai Lin, Guangyu Sun, Yunsi Fei, Yuan Xie, Anand Sivasubramaniam "Thermal-aware Design Considerations for Application-Specific Instruction Set Processor" in *Proceedings of International Symposium on Appication Specific Processors*, June. 2008. (19 out of 64 submissions, 29% acceptance rate)

[C153]. Xiangyu Dong, Xiaoxia Wu, Yuan Xie "Cost Analysis and Cost-driven EDA flow for 3D ICs" in *Proceedings of 3D-SIC Conference*, May. 2008.

[C154]. Feng Wang, Guangyu Sun, Yuan Xie. "A Variation Aware High Level Synthesis Framework." *Proceedings of Design Automation and Test in Europe (DATE)*,pp.1063-1068, Mar. 2008. (198 out of 839 submissions, 23% acceptance rate)

[C155]. Feng Wang, Xiaoxia Wu, Yuan Xie. "Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning." To appear in *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2008. **Best Paper Award.** *(29% acceptance rate for regular papers (100/351)).*

[C156]. Feng Wang, Xiaoxia Wu, C. Nicopoulos, Yuan Xie, N. Vijaykrishnan. "Variation-aware Task Allocation and Scheduling for MPSoC." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp. 138-149, Nov. 2007. *(139 out of 510 submissions, 27% acceptance rate).*

[C157]. Xiaoxia Wu, Paul Falkenstern, and Yuan Xie. "Scan Chain Design for Three-dimentional(3D) ICs." *Proceedings of International Conference on Computer Design (ICCD)*, pp.208-214, Oct. 2007. *(88 out of 259 submissions, 33% acceptance rate).*

[C158]. S. Srinivasan, P. Mangalagiri, Yuan Xie, N. Vijaykrishnan. "FPGA Routing Architecture Analysis Under Variations." *Proceedings of International Conference on Computer Design (ICCD)*, pp.152-157, Oct. 2007. *(88 out of 259 submissions, 33% acceptance rate).*

[C159]. H. Luo, Y. Wang, K. He, R. Luo, H. Yang, and Yuan Xie. "A Novel Gate-level NBTI Delay Degradation Model with Stacking Effect." *To appear in Proceedings of International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS)*, Sept. 2007.

[C160]. J. Kim, C. Nicopoulos, D. Park, R. Das, Yuan Xie, N. Vijaykrishnan, C. Das. "A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures." *Proceedings of the Annual International Symposium on Computer Architecture (ISCA)*, pp. 138-149, June 2007. *(46 papers accepted out of 204 submissions. 23% acceptance rate)*

[C161]. Alex K. Jones, Steven Levitan, Rob A. Rutenbar, and Yuan Xie. "Collaborative VLSI-CAD Instruction in the Digital Sandbox." *Proceedings of IEEE International Conference on Microelectronic Systems Education*, pp. 141-142, June 2007.

[C162]. Feng Wang, Yuan Xie, and Hai Ju. "A Novel Criticality Computation Method in Statistical Timing Analysis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1611-1616, April 2007. *(208 papers accepted out of 933 submissions. 22% acceptance rate)*

[C163]. Y. Wang, H. Luo, K. He, R. Luo, Yuan Xie, and H. Yang. "Temperature-aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 546-551, April 2007. *(208 papers accepted out of 933 submissions. 22% acceptance rate)*

[C164]. R. Krishnan, R. Ramanarayanan, S. Srinivasan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Variation Impact on SER of Combinatorial Circuits." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 911-916, March 2007. *(93 papers accepted out of 292 submissions. 31% acceptance rate)*

[C165]. A. Mupid, M. Mutyam, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Variation Analysis of CAM Cells." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 333-338, March 2007. *(93 papers accepted out of*

292 submissions. 31% acceptance rate)

[C166]. H. Luo, Y. Wang, K. He, R. Luo, H. Yang, Yuan Xie. "Modeling of PMOS NBTI Effect Considering Temperature Variation." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 139-144, March 2007. *(93 papers accepted out of 292 submissions. 31% acceptance rate)*

[C167]. Feng Wang and Yuan Xie. "Soft Error Rate Analysis for Combinational Logic Using An Accurate Electrical Masking Model." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2007. *(141 papers accepted out of 432 submissions. 32% acceptance rate)*

[C168]. Balaji Vaidyanathan, W-L. Hung, Feng Wang, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Architecting Microprocessor Components in 3D Design Space." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 103-108, Jan. 2007. *(141 papers accepted out of 432 submissions. 32% acceptance rate)*

[C169]. Balaji Vaidyanathan, Yuan Xie, N. Vijaykrishnan, R. Luo. "Leakage Optimized DECAP Design for FPGAs." *Proceedings of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 560-563, Dec. 2006.

[C170]. Wei-lun Hung, Xiaoxia Wu, Yuan Xie. "Guaranteeing Performance Yield in High-Level Synthesis." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp.303-309, Nov. 2006. **Best paper award nomination**.*(130 papers accepted out of 537 submissions. 24% acceptance rate).*

[C171]. Qian Ding, R. Luo, H. Wang, H. Yang and Yuan Xie. "Modeling the Impact of Process Variation on Critical Charge Distribution." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 243-237, Sept. 2006. *(58 regular papers accepted out of 177 submissions. 31% acceptance rate)*

[C172]. Balaji Vaidyanathan and Yuan Xie. "Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 93-97, Sept. 2006. *(58 papers accepted out of 177 submissions. 31% acceptance rate)*

[C173]. Xiaoxia Wu, Feng Wang, and Yuan Xie. "Analysis of Subthreshold Finfet Circuit for Ultra-low Power Design." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 91-93, Sept. 2006.

[C174]. S. Srinivasan, M. Prasanth, S. Karthink, Yuan Xie, N. Vijaykrishnan. "FLAW: FPGA Lifetime Awareness." *Proceedings of the 43rd Design Automation Conference (DAC)*, pp. 630-635, July. 2006. *(209 papers accepted out of 865 submissions. 24% acceptance rate)*

[C175]. F. Li,C. Nicopoulos, T. Richardson, Yuan Xie, N. Vijaykrishnan, M. Kandemir. "Design and Management of 3D Chip Multiprocessors using Network-in-memory." *Proceedings of the Annual International Symposium on Computer Architecture (ISCA)*, pp. 130-141, June. 2006. *(31 papers accepted out of 234 submissions. 13% acceptance rate)*

[C176]. Feng Wang, Yuan Xie. "An Accurate and Efficient Model of Electrical Masking Effect for Soft Errors in Combinatorial Logic." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C177]. B. Vaidyanathan, Yuan Xie, N. Vijaykrishnan. "Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C178]. R. Ramanarayanan, R. Krishnan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Temperature and Voltage Scaling Effects on Electrical Masking." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C179]. Wei-lun Hung, G. Link, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Interconnect and Thermal-aware Floorplanning for 3D Microprocessors." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 98-104, March. 2006. *(93 papers accepted out of 256 submissions. 36% acceptance rate)*

[C180]. Feng Wang, Yuan Xie, N. Vijaykrishnan and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 850-855, March 2006. *(233 papers accepted out of 834 submissions. 28% acceptance rate)*

[C181]. Feng Wang, Yuan Xie, K. Bernstein and Y. Luo. "Dependability Analysis of Nano-scale FinFET Circuits." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 399-404, March 2006.

[C182]. M. Mutyam, M. Eze, N. Vijaykrishnan, Yuan Xie. "Delay and Energy Efficient Data Transmission for On-Chip Buses." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 355-360, March 2006.

[C183]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Reliability-Aware SOC Voltage Islands Partition and Floorplan." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 343-348, March 2006.

[C184]. O. Ozturk, F. Wang, M. Kandemir, Yuan Xie. "Optimal Topology Exploration for Application-Specific 3D Architectures." *Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 390-395, Jan. 2006. *(135*

papers accepted out of 432 submissions. 31% acceptance rate)

[C185]. Ramanarayanan, R., J. S. Kim, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "SEAT-LA: A Soft Error Analysis tool for Combinational Logic." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. (*26.8% acceptance rate for regular papers (88 out of 328 submissions))*

[C186]. T. Richardson, C. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C. R. Das. "A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. *(26.8% acceptance rate for regular papers)*

[C187]. R. Luo, H. Luo, H. Yang, Yuan Xie. "An Instruction Level Analytical Power Model for Designing Low Power SOC." *Proceedings of IEEE International Conference on ASICs*, pp.1070-1073, Oct. 2005.

[C188]. T. Richardson and Yuan Xie. "Evaluation of Thermal-Aware Design Techniques for Microprocessors." *Proceedings of IEEE International Conference on ASICs*, pp.62-65, Oct. 2005.

[C189]. W-L. Hung, G. Link, Yuan Xie, N. Vijaykrishnan, N. Dhanwada, J. Conner. "Temperature-Aware Voltage Islands Architecting in System-on-Chip Design." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 689-696, Oct. 2005. *(101 out of 313 submissions, 32% acceptance rate)*

[C190]. S. K. Narayanan, G. Chen, M. Kandemir, Yuan Xie. "Temperature-Sensitive Loop Parallelization for Chip Multiprocessors." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 677-682, Oct. 2005. *(101 out of 313 submissions, 32% acceptance rate)*

[C191]. Y-F. Tsai, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Three-Dimensional Cache Design Exploration Using 3DCacti." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 519-524, Oct. 2005. *(101 out of 313 submissions, 32% acceptance rate)*

[C192]. D. Hostetler and Yuan Xie. " Adaptive Power Management in Software Radios Using Resolution Adaptive Analog to Digital Converters." *Proceedings of IEEE International Symposium on VLSI (ISVLSI)*, pp. 186-191, May. 2005.

[C193]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin "Thermal-Aware Floorplanning Using Genetic Algorithms." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 634-639, Mar. 2005. *(83 out of 222 submissions, 37% acceptance rate)*

[C194]. S. Tosun, O. Ozturk, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "An ILP Formulation for Reliability-Oriented High-Level Synthesis." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. *(83 out of 222 submissions, 37% acceptance rate)*

[C195]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-Centric Hardware/Software Co-design." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. *(83 out of 222 submissions, 37% acceptance rate)*

[C196]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-centric High-level Synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1258-1263, March 2005. *(176 papers accepted out of 825 submissions. 21% acceptance rate)*

[C197]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Power Attack Resistant Crypto Design: A Dynamic Voltage and Frequency Switching Approach." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 64-69, March 2005. *(21% acceptance rate)*

[C198]. Wei-lun Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 898-899, March 2005. *(21% acceptance rate)*

[C199]. Y-F Tsai, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Leakage-Aware Interconnect for On-Chip Network." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 230-231, March 2005. *(21% acceptance rate)*

[C200]. J.Conner,Yuan Xie, M. Kandemir, R. Dick, G. Link. "FD-HGAC: A Hybrid Heuristic/Genetic Algorithm Hardware/Software Co-synthesis Framework with Fault Detection." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC).*, pp. 709-712, Jan. 2005. *(99 regular papers accepted out of 692 submissions (14.3%))*

[C201]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC).*, pp. 539-544, Jan. 2005. *14.3% acceptance rate for regular papers (99 regular papers accepted out of 692 submissions (14.3%))*

[C202]. Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Yuan Xie. "Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 374-379, Jan. 2005. *(97 regular papers accepted out of 352 submissions (28%)).*

[C203]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100nm Circuits." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2005. *(97 regular papers accepted out of 352 submissions (28%)).*

[C204]. S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Yuan Xie, M. J. Irwin. " Improving Soft-error Tolerance of FPGA Configuration Bits." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 2004. *(24% acceptance rate).*

[C205]. W-L Hung, C. Addo-Quaye, T. Theocharides, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Thermal-Aware IP Virtualization and Placement for Networks-on-Chip Architecture." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 430-437, Oct. 2004. *(84 out of 226 submissions, 37% acceptance rate.)*

[C206]. Yuan Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. "Reliability-aware Cosynthesis for Embedded Systems." *Proceedings of IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP)*, pp. 41-50, Sept. 2004.

[C207]. W-L. Hung,Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Total Power Optimization Through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing With Stack Forcing." *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED 2004)*, pp. 144-149, Aug. 2004. *34% acceptance rate)*

[C208]. W. Xu, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Design of a Nanosensor Array Architecture." *Proceedings of Great Lakes Symposium on VLSI(GLSVLSI)*, pp. 298-303, Apr. 2004. *(23 full papers accepted out of 235 submissions, 10% rate)*

[C209]. V. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "The Effect of Threshold Voltages on the Soft Error Rate." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 503-508, Mar. 2004. *(49 papers accepted out of 148 submissions, 33%)*

[C210]. C-H. Lin, W. Wolf, and Yuan Xie. "LZW-based Code Compression for VLIW Embedded Systems." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Feb. 2004. *(181 papers accepted out of 780 submissions (23%))*

[C211]. Yuan Xie. "Analysis of Two Code Compression Algorithms for Embedded Systems." *Proceedings of International Conference on ASIC (ASICON)*, pp. 773-776. Oct. 2003.

[C212]. Yuan Xie, Wayne Wolf, H. Lekatsas. "Code Compression Using Arithmetic Coding Based Variable-to-fixed Coding." *Proceedings of Data Compression Conference(DCC 2003)*, pp. 382-391, Mar. 2003.

[C213]. Yuan Xie, W. Wolf, and H. Lektasas. "Profile-driven Code Compression." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Mar. 2003. *(152 out of 590 submissions (25%))*

[C214]. Yuan Xie, W. Wolf, and H. Lektasas. "Code Compression for VLIW Using Variable-to-fixed Coding." *Proceedings of Fifteenth International Symposium on System Synthesis (ISSS 2002)*, pp. 138-143, Oct. 2002. *(24 out of 71 submissions (33%))*

[C215]. Yuan Xie, W. Wolf, and H. Lektasas. "A Code Decompression Architecture for VLIW Processors." *Proceedings of the Thirty-Fourth International Symposium on Microarchitecture (MICRO-34). pp. 66-75. (29 out of 144 submissions, 20% acceptance rate)*

[C216]. Yuan Xie, W. Wolf, and H. Lektasas. "Compression Ratio and Decompression Overhead Tradeoffs in Code Compression for VLIW Architectures." *Proceedings of the Fourth International Conference on ASIC (ASICON).* **Best Paper Award**.

[C217]. Yuan Xie, W. Wolf. "ASICosyn: Co-Synthesis of Coditional Task Graphs with Custom ASICs." *Proceedings of the Fourth International Conference on ASIC (ASICON).*

[C218]. Yuan Xie, W. Wolf. "Allocation and Scheduling of Conditional Task Graphs in Co-synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 620-625, Mar. 2001. *(81 full papers out of 300 submissions (27%))*

[C219]. Yuan Xie, Hua Lin, Zhao Wu, W. Wolf. "CAD Techniques for Multimedia System Design." *Proceedings of Synthesis and System Integration of MIxed Technologies (SASIMI)*, Mar. 2000.

[C220]. Yuan Xie and Wayne Wolf. "Co-synthesis with Custom ASICs." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 129-134, Jan. 2000.

Patent

[1]. United States Patent. No. 9,317,448. "Methods and apparatus related to data processors and caches incorporated in data processors." Zhe Wang,Yuan Xie, Junli Gu, Yi Xu, ShuChang Shan, Shuai Mu, Ting Cao Issued on April 19, 2016.

[2]. United States Patent. No. 9,223,716. "Obstruction-Aware Cache Management." Jue Wang and Yuan Xie Issued on Dec. 29, 2015.

[3]. United States Patent. No.7,095,343. "Code Compression Algorithms and Architectures for Embedded Systems." Yuan Xie and Wayne Wolf Issued on August 22, 2006.

Patent Applications

[1]. United States Patent Application. Application No. 14/452058, Filed on 8/05/2014 Junli Gu, Brad Beckmann, and Yuan Xie "Moving Data Between Caches in A Heterogeneous Processor System."

[2]. United States Patent Application. Application No. 14/229404 , Filed on 03/28/2014. Zhe Wang, Yuan Xie, Yi Xu, Junli Gu, Ting Cao "Enhancing Lifetime of Non-Volatile Cache by Injecting Random Replacement Policy".

[3]. United States Patent Application. Application No. 14/229420 , Filed on 03/28/2014. Zhe Wang, Yuan Xie, Yi Xu, Junli Gu, Ting Cao "Enhancing Lifetime of Non-Volatile Cache by Reducing Inter-Block Write Variation".

[4].United States Patent Application. Application No. 14/144920 , Filed on 12/31/2013. Yi Xu, Xing Hu, and Yuan Xie "Voltage Droop Mitigation in 3D Chip System."

[5]. United States Patent Application. Application No. 13/913071 , Filed on 06/07/2013. Hong Su, Jian Yang, Yuan Xie, Jia-Yao Chen "Direct OpenCL Graphics Rendering."

[6]. United States Patent Application. Application No.13/976905, Filed on 5/21/2013 Yuan Xie and Junli Gu "Thermal-Aware Compiler for Parallel Instruction Execution in Processors."

[7]. United States Patent Application. Application No. 14/891523, Filed on 5/16/2013 Yi Xu, Nuwan Jayasena, Yuan Xie "MEMORY SYSTEM WITH REGION-SPECIFIC MEMORY ACCESS SCHEDULING."

[8]. China Patent Application. Application No. 201410062792 , Filed on 02/24/2014. Yuan Xie "Multi-chip System".

Student Supervision

Doctoral Dissertations Supervised

[1]. 2016 **Ping Chi**, Ph.D. in Electrical and Computer Engineering, UCSB
Facilitating Emerging Non-volatile Memories in Next-Generation Memory System Design: Architecture-Level and Application-Level Perspectives
First Employer: Assistant Professor, Chinese University at Hong Kong.

[2]. 2016 **Jia Zhan**, Ph.D. in Electrical and Computer Engineering, UCSB
The Interconnects for Energy Efficient Multicore Architecture
First Employer: Uber Inc.

[3]. 2016 **Hsiang-Yun Cheng**, Ph.D. in Computer Science and Engineering
Exploiting and Accommodating Asymmetries in Memory To Enable Efficient Multi-core Systems
First Employer: Assistant Professor, Academia Sinica, Taiwan.

[4]. 2015 **Matthew Poremba**, Ph.D. in Computer Science and Engineering
Architecture Modeling and Design with Emerging Memory Technologies
Current Job: Researcher at AMD Research Lab.

[5]. 2015 **Qiaosha Zou**, Ph.D. in Computer Science and Engineering
Design Automation and Optimization with Emerging 3D Integration Technologies
Current Job: Assistant Professor at Zhejiang Polytech University.

[6]. 2015 **Jing Xie**, Ph.D. in Computer Science and Engineering
Circuit Designs with Emerging 3D Integration Technologies
First Employer:Qualcomm Research.

[7]. 2014 **Cong Xu**, Ph.D. in Computer Science and Engineering
Modeling, Circuit Design, and Optimization of Resistive Memory
Current Job:Research Scientist at HP Labs.

[8]. 2014 **Jue Wang**, Ph.D. in Computer Science and Engineering
Architecture Level Design Using Emerging Nonvolatile Memory
Current Job: Research Scientist at Google.

[9]. 2014 **Tao Zhang**, Ph.D. in Computer Science and Engineering
High-performance and Low Power Memory Architecture
Current Job: Senior Architect at Nvidia Inc.

[10]. 2014 **Jishen Zhao**, Ph.D. in Computer Science and Engineering
Energy-efficient Memory Hierarchy Design with Emerging Technologies
Current Job: Assistant Professor at UCSC.

[11]. 2013 **Dimin Niu**, Ph.D. in Computer Science and Engineering
Modeling and Circuit Optimization for ReRAM Memory Architecture
Current Job: Senior Architect at Samsung.

[12]. 2012 **Jin Ouyang**, Ph.D. in Computer Science and Engineering
On-Chip Interconnection Network For Future Many-Core Chip-Multiprocessors
Current Job: Researcher at Nvidia Inc.

[13]. 2011 **Guangyu Sun**, Ph.D. in Computer Science and Engineering
Memory Hierarchy Design using Emerging Non-volatile Memories
Current Job: Assistant Professor at Peking University, China.

[14]. 2011 **Xiangyu Dong**, Ph.D. in Computer Science and Engineering
Modeling and Leveraging Emerging Non-Volatile Memories for Future Computer Designs
Current Employer: Google.

[15]. 2011 **Yibo Chen**, Ph.D. in Computer Science and Engineering
Variation-aware Behavioral Synthesis for Nanometer VLSI circuits
Current Employer: Google Inc.

[16]. 2011 **Mike Debole**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
Configurable Accelerators for Video Analytics
Current Employer: IBM.

[17]. 2010 **Soumya Eachempati**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
Influence of Emerging Technologies on Interconnect Architectures
Current Employer: Intel.

[18]. 2010 **Prasanth Mangalagiri**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
A Reliability and Process Variation Aware Design flow for Platform FPGAS
Current Employer: Intel.

[19]. 2010 **Xiaoxia Wu**, Ph.D. in Computer Science and Engineering
Design Space Exploration for 3D ICs
Current Employer: Qualcomm.

[20]. 2009 **Balaji Vaidyanthan**, Ph.D. in Computer Science and Engineering
Reliability Analysis and Optimization for Nanoscale System-on-Chip Design
Current Employer: Micron Inc.

[21]. 2008 **Feng Wang**, Ph.D. in Computer Science and Engineering
Design Automation Techniques to Mitigate Process Variations
Current Employer: Qualcomm.

[22]. 2007 **Yu Wang**, Ph.D. in Electronic Engineering, Tsinghua University (co-advised with Prof. Huazhong Yang)
Optimization for the Leakage Current and Reliability in Digital Integrated Circuits
Current Job: Assistant Professor in Tsinghua University.

[23]. 2006 **Wei-lun Hung**, Ph.D. in Computer Science and Engineering
Designing Cool Chips: Low Power and Thermal-Aware Design Methodologies
Current Employer: Sun Microsystems.

Postdoctor/Visiting Scholar Supervised

Visiting Scholar **Yuanqing Cheng**, Now Associate Professor at Beihang University, China.

Visiting Scholar **Chao Wang**, Now Associate Professor at University of Science and Technology in China(USTC), China.

Visiting Scholar — **Fen Ge**, Now Associate Professor at Nanjing University, China.

Visiting Scholar — **Chun-Yao Wang**, Now Associate Professor at National Tsing Hua University, Taiwan.

Post-Doc — **Yongsoo Joo**, Now Assistant Professor at Ewha University, Korea.

Post-Doc — **Lian Duan**, Ph.D. from Peking University, China.

Master Thesis Supervised

2016 — **Ziyang Qi**, M.S. in Electrical and Computer and Engineering, UCSB
First job: TBD

2015 — **Ivan Stalev**, M.S. in Computer Science and Engineering
Dark Silicon in Die-stacking Architecture
First job: Google

2015 — **Yang Zheng**, M.S. in Computer Science and Engineering
Design Automation for Emerging Resistive RAM
First job: Google

2008 — **Paul Falkenstern**, M.S. in Computer Science and Engineering
Design Automation Tools for 3D ICs
First job: Lockheed Martin Inc.

2007 — **Han-wei Chen**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Impact of Circuit Degradation on Design Security of Field Programmable Devices
Now graduate student at University of Texas at Austin.

2007 — **Charles Addo-Quaye**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Thermal-Aware Placement and Virtualization for Three Dimensional Network-on-Chip Designs
Now Ph.D. student at PennState.

2007 — **Melvin Eze**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Delay and Energy Efficient Data Transmission for On-Chip Buses
Now Ph.D. student at PennState.

2006 — **Yinkun Xue**, M.S. in Computer Science and Engineering
Providing Energy-Aware Map Services to Mobile Devices
First job: Siemens Inc.

2005 — **Thomas Richardson**, M.S. in Computer Science and Engineering
Analysis and Design of Scalable SoC Interconnects
First job: Availink Inc.

Current Students

[1]. Ph.D. — **Kaisheng Ma**(co-advise with Vijay Narayanan), Ph.D. in Computer Science and Engineering, Penn State

[2]. Ph.D. — **Shuangchen Li**, Ph.D. in Electrical and Computer Engineering, UCSB, 2014-

[3]. Ph.D. — **Itir Akgun**, Ph.D. in Electrical and Computer Engineering, UCSB, 2014-

[4]. Ph.D. — **Peng Gu**, Ph.D. in Electrical and Computer Engineering, UCSB, 2015-

[5]. Ph.D. — **Maohua Zhu**, Ph.D. in Electrical and Computer Engineering, UCSB, 2015-

[6]. Ph.D. — **Dylan Stow**, Ph.D. in Electrical and Computer Engineering, UCSB, 2015-

[7]. Ph.D. — **Liu Liu**, Ph.D. in Computer Science, UCSB, 2016-

[8]. Ph.D. — **Abanti Basak**, Ph.D. in Electrical and Computer Engineering, UCSB, 2016-

[9]. Ph.D. — **Wenqin Huangfu**, Ph.D. in Electrical and Computer Engineering, UCSB, 2016-

[10]. Ph.D. — **Alvin Oliver Glova**, Ph.D. in Electrical and Computer Engineering, UCSB, 2016-

[11]. M.S. — **Linuo Xue**, M.S. in Electrical and Computer Engineering, UCSB, 2014-

[12]. M.S. — **Russell Barnes**, M.S. in Electrical and Computer Engineering, UCSB, 2015-

Tutorials

06/2014 Semicon China [1]. **Full-day Tutorial: "Modeling and Architecture for Emerging Memory Technologies" ISCA, 2014**

03/2013 Semicon China [2]. **Full-day Tutorial: "Design and Tools for 3D ICs" SemiCon China, 2013**

03/2011 DATE-11 [3]. **Full-day Tutorial: "Manufacturing, CAD and Thermal-Aware Design for 3-D MPSoCs"** *with David Atienza (EPFL), Ruchir Puri (IBM), Tanay Karnik (Intel), Patrick Leduc (CEA-LETI)* **IEEE/ACM Design Automation and Test in Europe, 2011**

11/2010 ICCAD-10 [4]. **Half-day Tutorial: "Manufacturing, CAD and Thermal-Aware Design for 3-D MPSoCs"** *with David Atienza (EPFL), Sani Nassif (IBM), Ayse K. Coskun (Boston University)* **IEEE/ACM Intl. Conf. on CAD**

6/2010 DAC-10 [5]. **Full-day Tutorial: "3D IC: New Dimensions in IC Design"** *with Ruchir Puri (IBM), Tanay Karnik (Intel), David Atienza (EPFL), Paul Marchal (IMEC)* **IEEE/ACM Design Automation Conference**

3/2010 SC-09 [6]. **Half-day Tutorial: "The Impact of Emerging Technology on Computer System Design"** *Norm Jouppi (HP Labs) and Yuan Xie* **Architecture Support for Programming Language and Operating Systems (ASPLOS) 2010**

1/2010 ASPDAC-10 [7]. **Full-day Tutorial: "3D Integrated Circuit Design"** *with Ruchir Puri (IBM), Paul Franzon (NCSU) and Sachin Sapatnekar (UMN)* **ACM Asia and South-Pacific Design Automation Conference**

1/2010 VLSI Design-10 [8]. **Embedded Tutorial: "Processor Design using 3D Integrations" IEEE Symopsium on VLSI Design Conference**

12/2009 MICRO-2009 [9]. **Half-day Tutorial: "Integrated Multi-core Modeling"** *with Pradip Bose (IBM) and Eren Kursun (IBM)* **42nd International Symposium on Microarchitecture**

11/2009 SC-09 [10]. **Half-day Tutorial: "The Impact of Emerging Technology on Computer System Design"** *Norm Jouppi (HP Labs) and Yuan Xie* **Supercomputing 2009**

04/2009 VLSI/DAT-09 [11]. **Half-day Tutorial: "3D Integration"** *Yuan Xie* **International Symposium on VLSI/DAT**

06/2008 ISCA-08 [12]. **Half-day Tutorial: "3D Integration for Microarchitectures"** *organized with G. Loh (Gatech)* **International Symposium on Computer Architecture**

5/2006 GLSVLSI-08 [13]. **Half-day Tutorial: "Technology, EDA, and Architecture for Emerging 3D Integration"** *with Syed Alam (Freescale), Mike Ignatowski (IBM)* **Greatlake Symposium on VLSI (GLSVLSI), 2008**

12/2006 MICRO-06 [14]. **Half-day Tutorial: "3D Integration for Microarchitectures"** *with K.Bernstein (IBM), B. Black (Intel), and G. Loh (Gatech)* **International Symposium on Microarchitecture (MICRO-39)**

8/2006 VLSI06 [15]. **Half-day Tutorial: "Thermal-Aware Design Techniques for Nanometer VLSI Chips" The 17th VLSI Design/CAD Symposium**

10/2005 ASICON05 [16]. **Half-day Tutorial: "Thermal-Aware Design Techniques for Nanometer VLSI Chips" The 6th International Conference on ASIC (ASICON)**

06/2005 ISCA05 [17]. **Half-day Tutorial: "Robust Systems Design from Unreliable Components"** *with S. Mitra (Intel), L. Spainhower (IBM), and N. Vijaykrishnan (PSU)* **International Symposium on Computer Architecture (ISCA)**

01/2005 ASPDAC05 [18]. **Half-day Tutorial: "Designing Reliable Circuit in the Presence of Soft Errors" Asia-South-Pasific Design Automation Conference (ASP-DAC)**

10/2004 ASPLOS04 [19]. **Full-day Tutorial: "Computing in the Presence of Soft Errors "** *with N. Vijaykrishnan (PSU)* **Intl. Conf. on Architectural Support for Programming Languages and Operating Systems**

Invited Talks

10/2013	[1]. Invited talk, **Boston University** "MAAEMO: Modeling, Architecture, and Application for Emerging Memories"	**Boston, MA**
1/2013	[2]. Invited talk, **University of Illinois at Urbane Champain** "MAAEMO: Modeling, Architecture, and Application for Emerging Memories"	**Urbana Champain, IL**
1/2013	[3]. Invited talk, **Nortwestern University** "TSV-based 3D IC Design"	**Chicago, IL**
1/2013	[4]. Invited talk, **Semiconductor Manufacturing Intl. Corp. (SMIC)** "Design, Architecture, and Tools for 3D ICs"	**Shanghai, China**
11/2012	[5]. Invited talk, **Nanjing University** "3D IC Design and Tools"	**Nanjing, China**
4/2012	[6]. Invited talk, **University of California at San Diego (UCSD)** "Design and Architecture for 3D ICs"	**San Diego, USA**
4/2012	[7]. Invited talk, **University of Science and Technology of China (USTC)** "Design and Architecture for 3D ICs"	**Hefei, China**
3/2012	[8]. Invited talk, **Xi'an Polytech University** "Design and Architecture for 3D ICs"	**Xi'an, China**
3/2012	[9]. Invited talk, **Xi'an Jiaotong University** "Design and Architecture for 3D ICs"	**Xi'an, China**
12/2011	[10]. Invited talk, **Rice University** "Design and Architecture for 3D ICs"	**Houston, TX**
6/2011	[11]. Invited talk, **Intel China Labs** "3D IC Design and Architecture"	**Beijing, China**
6/2011	[12]. Invited talk, **Samsung** "3D IC Design and Architecture"	**Seoul, Korea**
6/2011	[13]. Invited talk, **IMAPS Northern California Chapter** "3D IC Design and Cost Implication"	**San Jose, CA**
5/2011	[14]. Invited talk, **Chinese Academy of Science** "Emerging NVM technologies for Exascale Computing"	**Beijing, China**
3/2011	[15]. Invited talk, **University of Illinois at Urbane Champain** "Design and Architecture for 3D ICs"	**Urbana Champain, IL**
3/2011	[16]. Invited talk, **AMD Research Labs** "3D Architecture and Application"	**Seattle, WA**
3/2011	[17]. Invited talk, **Global Semiconductor Alliances (GSA)** "Cost, Architecture, and Applications for 3D Integration"	**San Jose, CA**
12/2010	[18]. Invited talk, **National Tsing Hua University** "3D IC EDA and Architecture and Application"	**Hsinchu, Taiwan**
11/2010	[19]. Invited talk, **Yuan Ze University** "3D IC EDA and Architecture"	**Taipei, Taiwan**
11/2010	[20]. Invited talk, **National Chiao-Tung University** "Emerging Memory Technologies and the Impact on Computer System Design"	**Hsinchu, Taiwan**
10/2010	[21]. Invited talk, **National Cheng Kung University** "Emerging Memory Technologies and the Impact on Computer System Design"	**Tainan, Taiwan**
10/2010	[22]. Invited talk, **National Cheng Kung University** "Design Challenges for 3D ICs"	**Tainan, Taiwan**
09/2010	[23]. Invited talk, **Global Semiconductor Alliance (GSA)** " System Level Cost Analysis and Design Exploration for 3D ICs"	**San Jose, CA**
9/2010	[24]. Invited talk, **Industrial Technology Research Institute(ITRI)** "Design Challenges for 3D ICs"	**Hsinchu, Taiwan**
9/2010	[25]. Invited talk, **Korea Advanced Institute of Science and Technology (KAIST) UiversityDaejeon, Korea** "Design Challenges for 3D ICs"	

7/2010	[26]. Invited talk, **China Computer Federation** "Emerging Technologies and the Impact on Computer System Design"	**Beijing, China**
6/2010	[27]. Invited talk, **Qualcomm** "Emerging Memory Technologies and the Impact on Computer System Design"	**San Diego, CA**
5/2010	[28]. Invited talk, **IMEC (Interuniversity Microelectronic Centre** "Emerging Memory Technologies and the Impact on Computer System Design"	**Leuven, Belgium**
5/2010	[29]. Invited talk, **ETH Zurich** "3D IC Design, EDA, and Architecture"	**Zurich, Switzerland**
4/2010	[30]. Invited talk, **Carnegie Mellon University** "Emerging Memory Technologies and the Impact on Computer System Design"	**Pittsburgh, PA**
4/2010	[31]. Invited talk, **Princeton University** "Emerging 3D and NVM Technologies and the Impact on Computer System Design"	**Princeton, NJ**
1/2010	[32]. Invited talk, **Intel** "Modeling, Architecture, and Application for Emerging Memory Technologies"	**Hiilsboro, Oregon**
1/2010	[33]. Invited talk, **Tsinghua University** "Modeling, Architecture, and Application for Emerging Memory Technologies"	**Beijing, China**
1/2010	[34]. Invited talk, **Intel** "Modeling, Architecture, and Application for Emerging Memory Technologies"	**Bengalore, India**
11/2009	[35]. Invited talk, **Intel** "Design Methodologies and Architecture for 3D ICs"	**Hiilsboro, Oregon**
10/2009	[36]. Invited talk, **IBM T.J. Watson Research Lab** "Design Methodologies and Architecture for 3D ICs"	**Yorktown, NY**
8/2009	[37]. Invited talk, **9th International Forum on Embedded MPSoC and Multicore** "Enabling Many-Core Design via 3D Stacking"	**Savannah, GA**
6/2009	[38]. Invited talk, **National Chiao-Tung University (NCTU)** "Design Methodologies and Architecture for 3D ICs"	**HsinChu, Taiwan**
04/2009	[39]. Invited talk, **COOLCHIPS XII** "3D Microarchitecture"	**Yokohama, Japan**
04/2009	[40]. Invited talk, **Industrial Technology Research Institute(ITRI)** "3D IC Design"	**Hsinchu, Taiwan**
02/2009	[41]. Invited talk, **Semiconductor Research Corporation** "3D IC Design and Architecture"	**Raleigh, NC**
02/2009	[42]. Invited talk, **ECE Department, Duke University** "New Dimensions in 3D IC Design"	**Durham, NC**
09/2008	[43]. Invited talk, **ECE Department, Univ. of Texas in Austin** "Potential and Challenges in 3D IC Design"	**Austin, TX**
09/2008	[44]. Invited talk, **IBM Austin Research Lab** "Potential and Challenges in 3D IC Design"	**Austin, TX**
09/2008	[45]. Invited talk, **Freescale** "Potential and Challenges in 3D IC Design"	**Austin, TX**
09/2008	[46]. Invited talk, **National Tsinghua University** "Reliable Circuits Design on Top of Unreliable Hardware"	**Taiwan**
07/2008	[47]. Invited talk, **National Taiwan University** "Design Challenges in Three-dimensional IC Design"	**Taiwan**
07/2008	[48]. Invited talk, **National Tsinghua University** "Design Challenges in Three-dimensional IC Design"	**Taiwan**
06/2008	[49]. Invited talk, **Beijing BeiHang University** "Potential and Challenges in 3D IC Design"	**Beijing, China**
06/2008	[50]. Invited talk, **Harbin Institute of Technology.** "Design Challenges in Three-dimensional IC Design"	**China**
11/2007	[51]. Invited talk, **Qualcomm Inc.**	**San Diego, CA**

"Three-dimensional IC Design"

11/2007 [52]. Invited talk, **MetaRAM Inc.** **San Jose, CA**
"Three-dimensional IC Design"

10/2007 [53]. Invited talk, **Georgia Institute of Technology.** **Atlanta, GA**
"Variation-aware Multi-Processor System-on-Chip (MPSOC) Design"

10/2007 [54]. Invited tutorial, **Seagate Technology LLC.** **Bloomington, MN**
"3D IC Design Tutorial"

10/2007 [55]. Invited talk, **SEMATECH 3D workshop .** **Albany, New York**
"3D Archtecture Design"

09/2007 [56]. Invited talk, **KAIST University.** **Daejeon, Republic of Korea**
"Design Space Explorations for 3D ICs"

05/2007 [57]. Invited talk, **Honda Research Institute.** **Tokyo, Japan**
"Design Automation for Three-dimensional ICs"

05/2007 [58]. Invited talk, **Peking University.** **Beijing, China**
"New Dimension for High Performance"

04/2007 [59]. Invited talk, **IMEC (Interuniversity Microelectronics Centre).** **Leuven, Belgium**
"The Challenges of Designing 3D Microarchitectures"

01/2007 [60]. Invited talk, **Dagstuhl Seminar on Power-Aware Computing Systems.** **Dagstuhl, Germany**
"Thermal Challenges in 3D Microarchitecture Design"

11/2006 [61]. Invited talk, **The 3rd Annual 3-D Architectures Conference.** **San Francisco, CA**
"Design Space Exploration for 3D IC Design"

10/2006 [62]. Invited talk, **University of Pittsburgh.** **Pittsburgh, PA**
"The Challenges of Designing 3D Microarchitectures"

08/2006 [63]. Invited talk, **Hongkong University of Science and Technology.** **Hong Kong, China**
"3D Microarchitecture Design"

08/2006 [64]. Invited talk, **Intel China Research Center.** **Beijing, China**
"3D Microarchitecture Design"

03/2006 [65]. Invited talk, **IBM T.J.Watson Research Center.** **Yorktown, NY**
"The Challenges of Designing 3D Microarchitectures"

10/2005 [66]. Invited talk, **IBM China Research Lab.** **Shanghai, China**
"Thermal-Aware Design Techniques for Nanometer VLSI Chip"

10/2005 [67]. Invited talk, **Peking University.** **Beijing, China**
"Thermal-Aware Design Techniques for Nanometer VLSI Chip"

10/2005 [68]. Invited talk, **Shanghai Jiaotong University.** **Shanghai, China**
"Thermal-Aware Design Techniques for Nanometer VLSI Chip"

05/2005 [69]. Invited talk, **Syracuse University.** **Syracuse, NY**
"Thermal-Aware Design Techniques for Nanometer VLSI Chip"

10/2005 [70]. Invited talk, **University of South Florida.** **Tempa, FL**
"Thermal-Aware Design Techniques for Nanometer VLSI Chip"

10/2004 [71]. Invited talk, **IBM Circuit Education Seminar.**
"Soft Errors: Interactions with Power Optimizations"

Service and Activities

Professional Community

2016-now ACMSIGDA Executive Committee Member.
2009-2012 Committee Member, IEEE Design Automation Technical Committee (DATC).
2007-2010 Chair of Student Technical Activities on the Technical Activitites Board, IEEE Computer Society.
2010- ACM Distinguished Speaker.
2011-2013 IEEE Computer Society Distinghused Visitor.

Editorial

2016-	Editor-in-Chief, ACM Journal of Emerging Technologies in Computer Systems (JETC)
2016-	Associate Editor, IEEE Embedded System Letters (ESL)
2015-	Associate Editor, IEEE Transactions on Computers (TC).
2014-	Senior Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES)
2010-2015	Associate Editor, ACM Journal of Emerging Technologies in Computer Systems (JETC)
2008-	Associate Editor, Journal of Computer Science and Technologies (JCST)
2008-	Associate Editor, IET Computers and Digital Techniques (IET CDT).
2010-2013	Associate Editor, IEEE Transactions on CAD (TCAD).
2010-2012	Associate Editor, IEEE Design and Test of Computers.
2007-2014	Associate Editor, IEEE Transactions on VLSI Systems (TVLSI).

Guest Editorial

2009	Guest Co-Editor, IEEE Design and Test of Computers, Special Issues on 3D ICs.
2009	Guest co-Editor, IET Computers and Digital Techniques (IET CDT), Special Issues on 3D ICs.
2007	Guest co-Editor, ACM Journal of Emerging Technologies for Computer Systems (JETC), Special Issues on 3D ICs.

TPC Chair/Co-Chair in Conferences/Workshops:

2017	Technical Program Co-Chair for IEEE 17th International Forum on MPSoC for Software-defined Hardware, France
2017	Technical Program Vice Chair for 24th IEEE International Conference on High Performance Computing, Data, and Analytics, India
2015	General Chair for MPSOC Forum, USA
2015	Track co-Chair in System Architectures: VLSI-SOC 2015
2015	Track Chair in Internet of Things Symposium, VLSI System Track
2014	General Co-Chair for MPSOC Forum, Grenoble, France
2014	General Co-Chair for International Symposium on Low Power Electronic Devices (ISLPED)
2013	Technical Program Co-Chair for International Symposium on Low Power Electronic Devices (ISLPED)
2013	Technical Program Chair for Asia and South Pacific Design Automation Conference(ASP-DAC)
2012	Technical Program Vice Chair for Asia and South Pacific Design Automation Conference
2012	Technical Program Co-Chair for MPSOC Forum, Montreal, Canada
2011	General Co-Chair for Greatlake Symposium on VLSI (GSVLSI), Laussane, Switzerland
2011	Technical Program Co-Chair for MPSOC Forum, Grenoble, France
2010	General Co-Chair for Workshop on Design for 3D Integration, Laussane, Switzerland
2009	Program Co-Chair for International Symposium on VLSI (ISVLSI), Orlando, Florida
2009	Program Co-chair, First workshop for Three-dimensional Architectures, in conjunction with High Performance Computer Architectures(HPCA)
2008	Program Chair for 3D IC and Architecture Workshop, Hsin Chu, Taiwan.
2009	Program Subcommittee Chair for Emerging Technology Track, and TPC member, Design Automation and Test in Europe(DATE)

Program Committee Member in Conferences:

2016-2017	External Review Committee Member, IEEE International Symposium on Computer Architecture (ISCA)
2017	Program Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2016	External Review Committee Member, International Symposium on Microarchitecture(MICRO)
2016	Program Committee Member, International Conference on Parallel Architecture and Compilation Techniques (PACT)
2016	Program Committee Member, International Conference on Computer-Aided Design(ICCAD)
2016	External Review Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2015-16	Program Committee Member and Subcommittee Chair, IEEE/ACM Design Automation Conference (DAC)
2015-16	Program Committee Member, Design Automation and Test in Europe(DATE)
2015	Program Committee Member, International Symposium on Microarchitecture(MICRO)
2015	Program Committee Member, International Symposium on Low Power Electronics and Design
2014-16	Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
2014-16	Program Committee Member, IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)
2015	Program Committee Member and Subcommittee Chair, IEEE/ACM Design Automation Conference (DAC)
2015,14,12	Program Committee Member, International Symposium on Computer Architecture (ISCA)
2015	External Review Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2014	External Review Committee Member, IEEE International Symposium on Microarchitectre (MICRO),
2014	Program Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2013	Program Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2013	Program Committee Member, and Subcommittee Chair, IEEE/ACM Design Automation Conference (DAC)
2009-12	Program Committee Member, International Conference on Computer-Aided Design(ICCAD)
2012	Program Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
2012	Program Committee Member, IEEE MICRO Top-pick
2012	Program Committee Member, and Subcommittee Chair, IEEE/ACM Design Automation Conference (DAC)
2011	Program Committee Member, and Subcommittee Chair, IEEE/ACM Design Automation Conference (DAC)
2008	Program Committee Member, IEEE/ACM Design Automation Conference (DAC)
2008-2012	Sub-Committee Chair on Eemerging Technology, Design Automation and Test in Europe(DATE)
2008-2012	Program Committee Member, Asia and South Pacific Design Automation Conference (ASP-DAC)
2010	Program Committee Member, IFIP/ACM VLSI-SOC Conference
2010	Student Award Committee Co-Chair, High Performance Computer Architecture (HPCA)
2009,2006	Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
2009-2010	Program Committee Member, IEEE/ACM International Conference on Computer Design (ICCD)
2008-2011	Program Committee Member, IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)
2008	Program Committee Member, ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2008)
2008	Program Committee Member, Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-12)

2008	Program Committee Member, International Conference on VLSI Design (VLSID 2008)
2007	Program Committee Member, International Workshop on Trustworthiness, Reliability and Services in Ubiquitous and Sensor Networks (TRUST 2007)
2006-2007	Program Committee Member, International Conference on Communications, Circuits, and Systems
2007-2008	Program Committee Member, Financial Chair (2008), International Symposium on Low Power Electronics and Design
2007-2008	Program Committee Member, IEEE International Symposium on Circuits and Systems (ISCAS 2007, 2008)
2007	Program Committee Member, ACM International Conference on Computing Frontiers (CF 2007)
2007-2008	Program Committee Member, EDAA/PhD Forum, in conjunction with DATE 2007/2008
2006-2009	Program Committee Member, Finance Chair (2008,2009), Greatlake Symposium on VLSI (GLSVLSI)
2006	Program Committee Member, International Conference on Nano-networks (Nano-Net 2006)
2006	Program Committee Member, IFIP International Conference on Embedded and Ubiquitous Computing
2005	Program Committee Member, International Conference on Embedded Software and System (ICESS'05)
2005	Tutorial Chair, ACM Conference on Embedded Software (EMSOFT 2005)
2004-2005	Session Chair, International Conference on Computer Design
2003	Session Chair, International Conference on ASICs