Variation-aware Modeling of Integrated Capacitors based on Floating Random Walk Extraction

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Abstract—This paper presents an effective approach to variability analysis of integrated capacitors due to manufacturing process uncertainty. The proposed approach combines the generalized Polynomial Chaos method for uncertainty quantification with the efficient Floating Random Walk algorithm for capacitance extraction. For applications where detailed statistical descriptions are required, the method allows achieving a $1000\times$ acceleration compared to standard Monte Carlo analysis. Application to variability analysis in Digital to Analog Converters is illustrated.

Index Terms—floating random walk algorithm, stochastic models, uncertainty quantification.

I. Introduction

Capacitor devices manufactured in ultra-scaled integration technologies suffer from significant capacitance variability due to fabrication process uncertainty. Device variability reverberates on the performance of several Analog Mixed-Signal (AMS) electronic circuits where capacitors are embedded [1]. For given *nominal* electrodes geometry, dielectric thickness and material properties of the capacitor, the determination of the static electrical capacitance implies solving the Laplace's equation for the electrical potential. Indeed, for capacitors integrated in complicated 3D industrial layouts, the solution of such a static problem with standard finite-element or fine-difference techniques remains challenging in terms of simulation time and memory requirements. For these reasons, specialized techniques based on Floating Random Walk (FRW) have been developed and implemented in capacitance extraction tools [2]–[5]. FRW-based capacitance extraction can be used in connection with standard iterative Monte Carlo (MC) method to evaluate capacitance variability. However, MC method tends to be very time consuming since many iterations (e.g. ten of thousands) are commonly needed to calculate the capacitance statistical distribution with the stringent precision needed by AMS applications. In this paper, we explore a much more efficient approach to uncertainty quantification that relies on generalized polynomial chaos expansion (gPC) [6] and stochastic collocation [7] or stochastic testing (ST) method [8]. Such a method provides detailed statistical descriptions of the capacitance distribution, i.e. the complete Probability Density Function (PDF) (and not only mean and standard deviation),

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and it can handle both Gaussian and non-Gaussian distributed parameters. Furthermore, the gPC compact model, i.e. the surrogate model, can be used hierarchically to propagate capacitance variability to circuit level [12]. However, in the standard implementation of gPC with ST method, it is assumed that the samples of the physical quantity of interest are ideally exact and thus exact interpolation conditions are enforced at the test points. By contrast, the capacitance values extracted with the FRW algorithm are affected by numerical uncertainty and this can deteriorate the accuracy of gPC interpolation. In this paper, we show how the test points selection and interpolation condition can be modified so as to obtain a smooth (or regular) approximation of the relationship between capacitance value and uncertainty parameters. The method is based on least-squares approximation and is able to filter out the numerical uncertainty of FRW extraction. The contributions of this paper are: 1) we show how standard implementation gPC with ST method should be modified so as to deal with the uncertainty of capacitance extraction/evaluation; 2) we use the proposed method to deduce the detailed capacitance PDF in the presence of metal wire width and spacing variability; 3) we illustrate how the calculated PDF can be exploited to evaluate the differential nonlinearity (DNL) figure of merit for charge redistribution Digital to Analog Converters (DACs).

II. UNCERTAINTY QUANTIFICATION OF PHYSICAL QUANTITIES WITH GENERALIZED POLYNOMIAL CHAOS

In this section, we refer to a generic set of M physical quantities X^i , with $i=1,\ldots,M$, associated to an integrated electron device (e.g. the total and coupling capacitances among the electrodes of a capacitor device). These physical quantities all depend on the same set of l manufacturing parameters p_1,p_2,\ldots,p_l (e.g. the geometrical dimensions of electrodes, the oxide thickness) that have a certain degree of uncertainty. The nth parameter can thus be written as

$$p_n = p_n^0 + \xi_n, \tag{1}$$

where p_n^0 is the nominal value and ξ_n is the parameter uncertainty associated to a given manufacturing process. Mathematically, ξ_n is a zero-mean stochastic variable described by a given Probability Density Function (PDF) $\rho_n(\xi_n)$.

As a result, the physical quantities of interest can be seen as multi-valued functions of the parameter uncertainties, i.e.

$$X^i = X^i(\vec{\xi}),\tag{2}$$

where $\vec{\xi} = [\xi_1, \xi_2, \dots, \xi_l]$ is the parameter uncertainties vector.

An effective stochastic description of each X^i can be achieved by means of the generalized polynomial chaos expansion (gPC). In fact, under the hypothesis that X^i is a second-order stochastic process (i.e., it has finite variance), it can be approximated by an order-O truncated series

$$X^{i}(\vec{\xi}) \approx \sum_{j=1}^{N_b} x_j^i H_j(\vec{\xi}), \tag{3}$$

formed by N_b multi-variate basis functions $H_j(\vec{\xi})$ weighted by unknown polynomial chaos coefficients x_i^i [6]–[9].

Each multi-variate basis function is given by the product

$$H_j(\vec{\xi}) = \prod_{n=1}^l \phi_{j_n}(\xi_n) \tag{4}$$

where $\phi_{j_n}(\xi_n)$ is a univariate orthogonal polynomial of degree j_n whose form depends on the density function of the nth parameter ξ_n . For instance, $\phi_{j_n}(\xi_n)$ are Hermite polynomials if ξ_n is a Gaussian-distributed variable, while $\phi_{j_n}(\xi_n)$ are Legendre polynomials if ξ_n is a uniformly distributed variable [6]. For a given number of parameters l and series expansion truncation order O, the degrees j_n of univariate polynomials in (4) forming $H_j(\vec{\xi})$, for $n=1,\ldots,l$, are such that $\sum_{n=1}^l j_n \leq O$. For truncation order O and number of stochastic parameters l, the number of gPC basis functions is given by [7]

$$N_b = \frac{(O+l)!}{O! \, l!} \tag{5}$$

independently of the number ${\cal M}$ of physical quantities being described.

According to collocation-based Stochastic Testing (ST) method [8], the N_b unknown coefficients x_j^i in the series expansion (3) of $X^i(\vec{\xi})$ are calculated by properly selecting $N_s = N_b$ testing points $\vec{\xi}^k$, for $k = 1, \ldots, N_s$ in the stochastic space where the physical quantity $V_k^i = X^i(\vec{\xi}^k)$ is evaluated/extracted. The same set of testing points $\vec{\xi}$ is used for all of the M physical quantities X^i being approximated. At each testing point, the series expansions (3) are enforced to fit exactly (i.e., the polynomials interpolate the samples) the values V_k^i .

Mathematically, this results in the following linear systems

$$\mathbf{A}\,\vec{x}^{\,i} = \vec{V}^{\,i},\tag{6}$$

for $i=1,\ldots,M$, where $\vec{x}^i=[x_1^i,\ldots,x_{N_b}^i]^T$ and $\vec{V}^i=[V_1^i,\ldots,V_{N_s}^i]^T$ are the column vectors collecting the unknown coefficients and physical quantities values, respectively. The linear systems in (6) are among them decoupled but share the same $N_b\times N_b$ square matrix $\mathbf{A}=\{a_{k,j}\}=\{H_j(\vec{\xi}^k)\}$. Such a matrix collects the gPC basis functions evaluated at the testing points, i.e.

$$\mathbf{A} = \begin{bmatrix} H_1(\vec{\xi}^{\dot{1}}) & \dots & H_{N_b}(\vec{\xi}^{\dot{1}}) \\ \vdots & \ddots & \vdots \\ H_1(\vec{\xi}^{N_s}) & \dots & H_{N_b}(\vec{\xi}^{N_s}) \end{bmatrix}. \tag{7}$$

The selection of the testing points $\vec{\xi}^k$ in the stochastic space is done so as to ensure the highest numerical accuracy

of the gPC-based interpolation scheme and of the associated statistical description. This is achieved by considering the highest order O univariate polynomial $\phi(\xi_n)$ describing the nth parameter ξ_n with PDF $\rho_n(\xi_n)$. The associated stochastic integral is best approximated by a Gauss quadrature formula

$$\int_{\Omega_n} \phi(\xi_n) \rho_n(\xi_n) d\xi_n \approx \sum_{k=1}^{O+1} \phi(\xi_n^k) w_n^k, \tag{8}$$

where ξ_n^k is the kth quadrature node and w_n^k the corresponding weight. The O+1 quadrature nodes ξ_n^k are thus good testing points for the single uncertainty parameter ξ_n . Passing to the multivariate case with l parameters, the testing points vectors $\vec{\xi}^k = [\xi_1^k, \xi_2^k, \dots, \xi_l^k]$ are determined by considering the multi-dimensional grid of all the possible combinations (i.e. the tensor product) of the univariate quadrature nodes.

It is worth noting that the number $(O+1)^l$ of nodes in the multi-dimensional grid is greater than the number N_b of basis functions defined in (5). For instance, in the case of two parameters (i.e. l=2) and expansion order O=3, the number of nodes is 16 while the number of basis is only $N_b=10$. To make problem (6) well posed, a subset formed by $N_s=N_b$ quadrature nodes has to be selected as testing points. A proper method for selecting the subset of testing points among the quadrature nodes is presented in [8]. It relies on the criteria of preferring those quadrature nodes with largest associated weights w_n^k and that lead to well conditioned matrix $\bf A$.

Finally, once (6) has been solved and coefficients x_j^i computed, the compact models (3) allow deriving in a very efficient way the detailed PDF for all of the X^i quantities as well as their mean values and standard deviations [8].

III. DEALING WITH THE UNCERTAINTY OF FRW-BASED CAPACITANCE EXTRACTION

In this section, we investigate uncertainty quantification for capacitor devices employed in electronic applications, e.g. in DAC circuits. For a given electrodes geometry and physical property, the capacitance values (i.e. the coupling capacitance and total capacitances) can be efficiently extracted via the iterative Floating Random Walk (FRW) algorithm [2]-[5]. In the remainder of this paper, we specifically focus on coupling capacitance since this is the relevant quantity for DAC circuits [10]. Compared to other efficient techniques for capacitance extraction, FRW does not need any space/geometry discretization and this enables handling complex 3D layouts that are otherwise intractable. However, FRW methods provide an approximate capacitance estimation with an error that reduces only as the inverse of the square root of the number of walks N_{FRW} . This fact can be critical when FRW is used in connection with the gPC and ST methods presented in Sec. II. In this case, in fact for each testing point described by the uncertainty vector ξ^k , the FRW extractor supplies a capacitance estimation of the type

$$C(\vec{\xi}^k) = X(\vec{\xi}^k) = V_k(\vec{\xi}^k) + e_k, \tag{9}$$

where $V_k(\vec{\xi}^k)$ is the (unknown) exact capacitance value and e_k is the error introduced by the FRW algorithm. Such an error is a random variable symmetrically distributed around its zero

mean value [3]. Furthermore, due to the great number of walks N_{FRW} performed in each extraction of the capacitance value (9), it follows that the FRW errors e_k at different testing points $\vec{\xi}^k$ in the parameter space Ω are among them independent. As a consequence, for any continuous deterministic function $H(\vec{\xi})$ of the uncertainty parameters and any set of N_s test points $\vec{\xi}^k$, the following relation

$$\lim_{N_s \to \infty} \frac{1}{N_s} \sum_{k=1}^{N_s} H(\vec{\xi}^k) e_k = 0$$
 (10)

holds [3].

The presence of an error in the physical variable estimation $X(\vec{\xi}^k)$ makes the scheme (6) inaccurate. To overcome this drawback, we propose the following enhanced method. First, among the $(O+1)^l$ quadrature nodes in the l-dimensional space, we select a number of testing points $N_s > N_b$ greater than the number of basis. At limit, all of the quadrature nodes may be used as testing points. In this way, when the gPC expansion (3) is imposed to fit the capacitance values (9) at testing points, the following over-determined linear system is obtained

$$\mathbf{A}_{auq}\,\vec{x} = \vec{V} + \vec{e},\tag{11}$$

where the $N_s \times 1$ column vectors \vec{V} and \vec{e} contains the exact capacitance values and FRW errors respectively. The augmented $N_s \times N_b$ rectangular matrix $\mathbf{A}_{aug} = \{a_{k,j}\} = \{H_j(\vec{\xi}^k)\}$ collects the N_b basis functions evaluated at the N_s testing points.

Second, the over-determined system (11) is solved in the least-squares sense by multiplying both sides of (11) by the augmented transposed matrix, i.e.

$$\left(\mathbf{A}_{aug}^{T} \cdot \mathbf{A}_{aug}\right) \vec{x} = \mathbf{A}_{aug}^{T} \left(\vec{V} + \vec{e}\right), \tag{12}$$

and then solving the resulting well posed system (12). In the remainder of this paper, we will refer to the gPC with method (12) as Least-Squares Stochastic Testing (LS-ST). The good feature of the LS-ST method can be seen by dividing both members of (12) by N_s and then looking at the form of the jth element in the right-hand side. It reads

$$\frac{1}{N_s} \sum_{k=1}^{N_s} H_j(\vec{\xi}^k) V(\vec{\xi}^k) + \frac{1}{N_s} \sum_{k=1}^{N_s} H_j(\vec{\xi}^k) e_k. \tag{13}$$

When N_s grows, the first term in (13) remains finite while, in view of (10), the second term tends to vanish. As a consequence, the random errors introduced by the FRW method tend to be filtered out by the LS-ST formulation (12). In this way, the coefficients x_j derived by solving (12) are such that the associated gPC expansion (3) provides an accurate global approximation of the $X=X(\xi)$ relationship through a smooth multi-dimensional surface. The surrogate model provided by the gPC expansion (3) can then be used to evaluate the detailed PDF of the capacitance as well as its mean value $\mu_c = \text{mean}(C)$ and standard deviation $\sigma_c = \text{std}(C)$. The statistical variability of capacitor device can be propagated hierarchically in the circuits and systems where it is embedded [12].

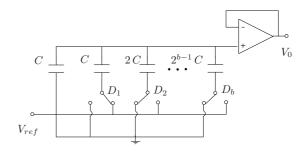


Fig. 1. The circuit of the charge redistribution DAC.

IV. VARIABILITY ANALYSIS OF DIGITAL TO ANALOG CONVERTERS (DAC)

As an example, we consider the charge redistribution DAC shown in Fig. 1. This circuit is made of a bank of b+1 capacitors whose values are multiple of the unit capacitance C, i.e. $C_0=C$ and $C_i=2^{i-1}C$ for $i=1,\ldots b$. Given a digital word described by b digits D_1,\ldots,D_b , the circuit converts it into the analog output voltage

$$V_0 = V_{ref} \cdot \left(\sum_{i=1}^b D_i C_i\right) / \left(C_0 + \sum_{i=1}^b C_i\right), \tag{14}$$

where V_{ref} is a reference voltage level. The statistical fluctuations of the unit capacitance C, produce statistical fluctuations in the bank capacitor value C_i and eventually in the analog values V_0 . The values of capacitors C_i are distributed with the same PDF as C but with the mean value $\operatorname{mean}(C_i) = (2^{i-1})\,\mu_c$ and standard deviation $\operatorname{std}(C_i) = (\sqrt{2^{i-1}})\,\sigma_c$. As a result, from the detailed PDF of C provided by the gPC model we are able to evaluate the statistical distribution of each output voltage level V_0 by using (14) and MC method. Finally, considering two consecutive values $V_0^L < V_0^H$ taken by the output voltage and the associated analog interval (V_0^L, V_0^H) , the statistical distribution of the differential nonlinearity (DNL) is calculated as $\operatorname{DNL} = (V_0^H - V_0^L)/\operatorname{LSB} - 1$, where $\operatorname{LSB} = V_{ref}/2^b$ denotes the nominal interval width corresponding to the least significant bit.

V. NUMERICAL RESULTS

In this section, the gPC method is applied to the lateral-field fringing capacitor whose layout is shown in Fig. 2 [10].

It is made of two interdigitated electrodes realized on the same Metal layer (i.e one-layer MOM capacitor) whose layout is defined by: the metal finger width W, finger spacing S and overlap length L. A metal thickness $T_m=0.5\,\mu\mathrm{m}$ is assumed. Finger spacing and width are taken as the uncertain manufacturing parameters $p_1=S$ and $p_2=W$ while overlap length is fixed to $L=10\,\mu\mathrm{m}$. Stochastic parameters are assumed to be mutually-independent and Gaussian distributed around the mean values $p_1^0=p_2^0=0.3\,\mu\mathrm{m}$. In order to calculate the gPC coefficients x_j of the surrogate model (3), we assume 10% standard deviations $\sigma_1=\sigma_2=0.03\mu\mathrm{m}$. This makes the model valid over a sufficiently wide range of parameter variations.

First, we use the gPC expansion (3) truncated to order O = 3 in connection with standard interpolation-based ST

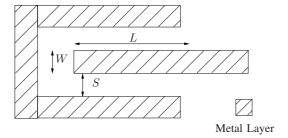


Fig. 2. Top view of the capacitor layout.

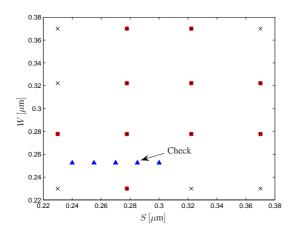


Fig. 3. (Black Cross Marker) The 2-dimensional grid of quadrature nodes. (Red Circle Marker) Subset of nodes used as testing points in ST interpolation. (Blue Triangle Marker) Points used as a check.

method (6). Fig. 3 shows all the sixteen quadrature nodes in the stochastic space of parameters and the subset of ten nodes selected with the algorithm in [8] and used as testing points. At testing points, the corresponding capacitance values are extracted with the FRW algorithm. For each extraction, we run $N_{FRW}=80,000$ random walks (which corresponds to an estimated extraction uncertainty of ≈ 0.06 fF). With the gPC coefficients x_j derived by solving ST system (6), we then use the compact gPC model (3) to predict the capacitance values at some new points (i.e. not employed in interpolation) used for accuracy check.

Second, for the same gPC order O=3, we compute the expansion coefficients with the enhanced LS-ST method (12) presented in this paper. With the LS-ST method, all of the sixteen quadrature nodes in Fig. 3 are employed as testing points. For a fair comparison with ST, when using the LS-ST method the capacitance value at each testing point is extracted by running a smaller number $N_{FRW}=50,000$ of random walks. In this way, the total computational time (e.g. the product $N_s \times N_{FRW}$) is kept the same for LS-ST and ST methods. Fig. 4 reports the capacitance values predicted by gPC ST and LS-ST methods at considered check points along with the values extracted with the FRW method by running 2,000,000 walks 1 . It is seen how ST interpolation exhibits a significant discrepancy compared to the reference FRW with a

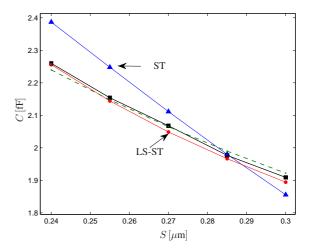


Fig. 4. Capacitance values at check points: (Black Square Marker) Reference values provided by FRW (2,000,000 of walks/per point). (Blue Triangle Marker) Capacitance values predicted by ST. (Red Circle Marker) Capacitance values predicted by enhanced LS-ST. (Green Dashed Marker) Capacitance values predicted by ST when trained by expensive FRW (2,000,000 of walks/per point).

maximum error of $\approx 0.14 fF$ near the border of the stochastic space. By contrast, the LS-ST smooth approximation closely follows the reference curve with a smaller approximation error (always smaller than $\approx 0.02\, fF)$ that keeps almost constant along the curve.

As a further verification, we recalculate the gPC coefficients for the conventional ST system (6) but now we use the accurate capacitance values extracted by running 2,000,000 walks at each sample point. The interpolation provided by the ST method trained by the expensive FRW, reported in Fig. 4 with a dashed line, moves closely to the reference and LS-ST curves. We can conclude that, for the same computational time and noisy samples extracted by efficient FRWs (< 100,000 walks per point), the LS-ST method provides more accurate gPC expansions than conventional ST method. The accuracy of ST method can be recovered by running a large number of walks per sample ($\approx 2,000,000$ walks), however this requires computational times that are $\approx 25 \times$ greater compared to LS-ST.

The compact model (3), with the extracted coefficients, is then used to efficiently evaluate the capacitance PDF. Fig. 5 shows the PDF derived with the LS-ST method when 5% standard deviations of the finger spacing and width parameters, i.e. $\sigma_1 = \sigma_2 = 0.015\mu\text{m}$, are assumed. In this case, the computed mean value and standard deviation are $\text{mean}(C) = 1.95\,\text{fF}$ and $\text{std}(C) = 0.072\,\text{fF}$, respectively. These values are in agreement with the experimental values reported in the literature [11] (Table-I in this reference) for custom-fabricated one-layer MOM capacitors. By a comparison with the Gaussian distribution of equal mean value and variance reported in Fig. 5, we also observe how the capacitance PDF is not strictly Gaussian and exhibits a non symmetric shape around the mean value. This is due to the nonlinearity of capacitance dependence on geometry parameters. Such a non-

 $^{^{1}}$ This corresponds to a FRW extraction uncertainty of $\approx 0.008 \, \text{fF}$ and thus it is considered as accurate reference.

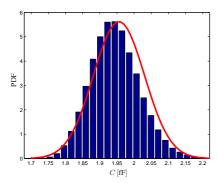


Fig. 5. (Histogram) PDF of capacitance values derived with LS-ST: ${\rm mean}(C)=1.95\,{\rm fF},\,{\rm std}(C)=0.072\,{\rm fF}.$ (Red Continuous Line) Gaussian distribution of equal mean value and variance.

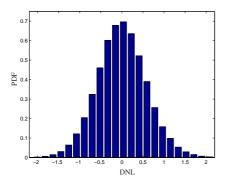


Fig. 6. (Histogram) PDF of the mid-code DNL for a 8-bit DAC.

Gaussian capacitance distribution should be considered when investigating variability at circuit level.

We check these results by using standard MC method and FRW. In order to estimate the $\operatorname{std}(C)$ with a relative accuracy of 2% (as needed by application to DACs) we have to perform more than 10,000 capacitance extractions (i.e. Monte Carlo iterations) each one requiring running more than 80,000 walks. Such an accurate MC analysis requires a computational time which is about $1000\times$ greater than that of the LS-ST method. The PDF provided by the accurate MC method is very close to that shown in Fig. 5 and has mean value and standard deviation $\operatorname{mean}(C) = 1.95 \, \operatorname{fF}$ and $\operatorname{std}(C) = 0.071 \, \operatorname{fF}$, respectively. By contrast, the PDF provided by the standard ST method (with extraction based on 80,000 walks) predicts a 14% greater standard deviation $\operatorname{std}(C) = 0.082 \, \operatorname{fF}$ and a more pronounced non-symmetric distribution.

Finally, the gPC expansion derived with the LS-ST method is employed to evaluate the critical mid-code DNL, determined by the consecutive codes $2^{b-1}-1$ and 2^{b-1} , in charge redistribution DAC, as explained in Sec. IV. Fig. 6 shows the distribution of the DNL for a 8-bit DAC: 90% of the realizations are such that -1 < DNL < 1 and thus no missing code occurs. We verified that the percentage of successful realizations increases to 100% for b=6.

VI. CONCLUSION

In this paper, we have described an effective approach for modeling the statistical uncertainty of integrated capacitors. The proposed model relies on state-of-the-art uncertainty quantification techniques based on polynomial chaos expansion and stochastic testing method. In this paper, we have extended the available method to the case where the extraction of capacitance values is done with the efficient FRW algorithm and thus is itself affected by a degree of uncertainty. The method has been employed to evaluate the effect of metal wire width and spacing uncertainty on capacitance distribution. We have shown how the method can provide detailed statistical descriptions in the presence of relatively large parameter variations and nonlinearities. For applications where accurate detailed statistical descriptions are required, the method can achieve a 1000× acceleration compared to Monte Carlo analysis, for the same accuracy. An application example to variability analysis of charge redistribution DACs has been provided.

REFERENCES

- [1] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26 W 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585-1595, Jul. 2011.
- [2] Y. L. Le Coz, R. B. Iverson, "A stochastic algorithm for high speed capacitance extraction in integrated circuits," *Solid-State Electron.*, vol. 35, no. 7, pp. 1005-1012, Jul. 1992.
- [3] A. Brambilla, P. Maffezzoni, "Statistical Method for the Analysis of Interconnects Delay in Sub-micron Layouts," *IEEE Trans. on Computer-Aided-Design of Integrated Circuits and Systems*, vol. 20, no. 8, pp. 957-966, Aug. 2001.
- [4] Tarek A. El-Moselhy, Ibrahim M. Elfadel, and Luca Daniel, "A capacitance solver for incremental variation-aware extraction" Proc. of the 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD '08), San Jose, CA, Nov. 2008, pp. 662-669.
- [5] Wenjian Yu, H. Zhuang, C. Zhang, G. Hu and Z. Liu, "RWCap: A Floating Random Walk Solver for 3-D Capacitance Extraction of Very-Large-Scale Integration Interconnects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 3, pp. 353-366, March 2013.
- [6] D. Xiu and G. E. Karniadakis, "The Wiener-Askey polynomial chaos for stochastic differential equations," SIAM Journal on Scientific Computing, vol. 24, no. 2, pp. 619-644, Feb 2002.
- [7] A. Sandu, C. Sandu, and M. Ahmadian, "Modeling multibody systems with uncertainties. part I: Theoretical and computational aspects," *Multibody Syst. Dyn.*, vol. 15, no. 9, pp. 373-395, Sept. 2006.
- [8] Z. Zhang, T. A. El-Moselhy, I. M. Elfadel, and L. Daniel, "Stochastic testing method for transistor-level uncertainty quantification based on generalized polynomial chaos," *IEEE Trans. Computer-Aided-Design* of Integrated Circuits and Systems, vol. 32, no. 10, pp. 1533-1545, Oct. 2013.
- [9] Wenjian Yu, Chao Hu, and Wangyang Zhang, "Variational capacitance extraction of on-chip interconnects based on continuous surface model," *Proc. Design Automation Conference*, San Francisco, CA, USA, Jul. 2009, pp. 758-763.
- [10] H. Omran, H. Alahmadi and K. N. Salama, "Matching Properties of Femtofarad and Sub-Femtofarad MOM Capacitors," *IEEE Transactions* on Circuits and Systems I: Regular Papers, vol. 63, no. 6, pp. 763-772, June 2016.
- [11] A. Abusleme, A. Dragone, G. Haller and B. Murmann, "Mismatch of lateral field metal-oxide-metal capacitors in 180 nm CMOS process," *Electronics Letters*, vol. 48, no. 5, pp. 286-287, March 2012.
- [12] Z. Zhang, T. A. El-Moselhy, I. M. Elfadel and L. Daniel, "Calculation of Generalized Polynomial-Chaos Basis Functions and Gauss Quadrature Rules in Hierarchical Uncertainty Quantification," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 5, pp. 728-740, May 2014.